THE DESIGN OF A MULTI-LOOP, LOW-POWER LOW DROPOUT VOLTAGE REGULATOR WITH ZERO-POLE TRACKING TECHNIQUE

by

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ABSTRACT

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The Design of a Multi-Loop, Low-Power Low Dropout Voltage Regulator With Zero-Pole Tracking Technique

Bachelor of Engineering, Electrical and Computer Engineering, Lakehead University, 2023

This thesis describes the theoretical background, design, simulation, implementation and measurements of an analog low-dropout voltage regulator intended for wide load applications requiring low power consumption. Due to the modern requirements for systems on chip to be operable over long periods and over wide conditions, circuits have become more efficient to meet such demands. Typically as a regulator design is optimized for low power consumption, the performance is worsened. This tradeoff produces the need for a low-dropout regulator which is capable of wide, stable operation while consuming little current. This work contributes to the state of the art of low power low-dropout regulators, further contributing to the literature by testing and measuring the fabricated design. Finally deepening this research with a comparison of the past decades of research in low-dropout technologies.

The proposed work in this thesis is comprised of a low-dropout regulator which utilizes a multi-loop compensation network to increase this stability while consuming very little current. The design introduces Ahuja compensation, which removes the feed-forward path which is common in Miller compensation. Furthermore, a zero-tracking network is proposed, which extends stability by inserting a zero capable of tracking the frequency of the dominant output pole. This multi-loop technique provides a phase margin of 60° at the lowest, demonstrating stable operation through the full current range of 0 mA to 50 mA. A schematic and layout is produced with the design being implemented in the TSMC 180 nm standard CMOS process. The measured quiescent current is 486.67 nA with the ability to reduce this further by disabling the circuit operation, allowing for a static current draw of 2.06nA. At its

peak, the circuit performs with a current efficiency of 99.96%. With a stepped load transient performance of 418 μs with an overshoot of 52.5 mV between full and no load. With the positive step response being 36.5 μs with a change in output of 81.25mV.

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List of Abbreviations

ADC	Analog to Digital Converters
$ASIC$	Application Specific Integrated Circuit
BJT	Bipolar Junction Transistor
$CMOS$	Complementary Metal-Oxide Semiconductor
CMP	Chemical-Mechanical Polishing
DRC	Design Rule Check
DUT	Device Under Test
ESD	Electro Static Discharge
ESR	Equivalent Series Resistance
FF	(nMOS)Fast-(pMOS)Fast
FS	(nMOS)Fast-(pMOS)Slow
IoT	Internet of Things
I_Q	Quiescent Current:
LDO	Low-Dropout Voltage Regulator
LVS	Layout V. Schematic
MIM	Metal-Insulator-Metal (Capacitor)
$MOSFET$	Metal Oxide Semiconductor Field Effect Transistor
$nMOS$	n-channel Metal-Oxide Semiconductor

OTA	Operational Transconductance Amplifier
$PMIC$	Power Management Integrated Circuit
$pMOS$	p-channel Metal-Oxide Semiconductor
$RFIC$	Radio Frequency Integrated Circuit
RHP	Right-Half-Plane
SF	(nMOS)Slow-(pMOS)Fast
SS	(nMOS)Slow-(pMOS)Slow
SoC	System on Chip
TT	(nMOS)Typical-(pMOS)Typical
UGF	Unity Gain Frequency
ZT	Zero Tracking
ϕ_M	Phase Margin

Chapter 1

INTRODUCTION

In the realm of electronics, a major keystone of all designs is power regulation. Given a device, one must ensure that the specifications for operation described by the designing engineer must be met within tolerances to ensure long, stable operation. No electronics are immune to noise, small changes in supply voltage and even catastrophic changes resulting in premature failure of the device. Voltage regulators specifically low-dropout regulators [1], are therefore necessary in mitigating and minimizing these potential risks and are a primary tool towards protecting integrated circuits. Each circuit handles fluctuations in supply differently and have different specifications, as mentioned, therefore, a balance must be made when approached with such challenges, which means that no one regulator can suit all applications. There are a number of specific applications for power regulation circuits and available optimizations for which we can explore. This chapter will give a clear reasoning behind the motivation for this work, carrying into the objectives for this voltage regulator.

1.1 Motivation

In today's system on chip (SoC) devices the demand for space efficient, low power consuming components is quickly becoming the norm. Frequently, the applications for these devices are for use in portable electronics requiring lasting battery life, internet of things (IoT) devices, or low-power circuits such as wireless receivers, analog to digital converters

(ADCs) [2–4], ect. The demands of these devices in critical situations as well as harsh environments gave rise to multitude of techniques to have long lasting performance. Some devices have the ability to enter a "sleep-mode" and the importance of low quiescent current (I_Q) draw is becoming a forefront target in the mind of a designer. If the power management of an SoC doesn't meet these requirements, rarely will down stream components be able to make up for these regulation losses, and so the importance of these primary actors is paramount.

The modern power management unit or (PMIC) is designed to supply multiple output voltages, potentially with multiple load capabilities associated to each. This is accomplished by housing varying arrays of DC-DC converters which are typically buck converters, along with multiple linear regulators typically being low-dropout voltage regulators. A large factor in power efficiency is dropout voltage, which is determined by the difference between the input voltage to a regulator, and the maximum output voltage that can be achieved while still being able to regulate changes in line or load characteristics.

With current embedded systems and application specific integrated circuit (ASIC) technologies trending towards advanced processes, the gate voltages required to drive these transistors has dropped. LDOs are now required to have lower output voltage capabilities to meet the demand of these technology nodes. With this, the ability to curate a design for efficiency at voltages ranging from 1.8 V down to 0.8 V for "safe" SoC applications is important. This reduces overall power consumption, however has the tradeoff of increasing the difficulty a designer faces in creating a low-dropout device which can be utilized in wide-load applications. Although it is customary to parallelize power management and have many different LDOs feedings portions of an IC architecture, the need for a single, wide-load device still arises. Therefore a device, capable of low I_Q with a "sleep-mode" section is proposed, able to drive a low-voltage, wide-load device.

One of the most utilized building blocks in radio frequency ICs (RFIC) is the oscillator, whose phase noise plays a pivotal role in meeting the stringent requirements for data rate in wireless communication systems. The design and analysis of low phase noise oscillators have been extensively developed [5–12]. It is noted that noise from LDOs, which provide regulated voltage to the oscillators, is detrimental to their performance. Therefore, minimizing the noise contributed by LDOs is often preferable.

1.2 Objectives

The objective of this paper is to explore solutions to these common problems. The design must be a low power consuming device, this will be achieved through having a small I_Q over as full a range as possible. Furthermore, the dropout voltage must be minimized; this, in tandem with a low quiescent current will allow for low overall power consumption. The circuit must drive a wide load range, with a stable operation through that full range, allowing for quick, accurate regulation of line and load changes. The important figure to determine the effectiveness of this circuit's stability is if phase margin, $\phi M \geq 60°$.

With these design considerations in mind, we propose a solution to stability issues in low I_Q LDOs by making use of a Zero-Tracking (ZT) compensation network. The tracking network functions by adding internal feedback compensation which follows the current at the load to control the position of the zero in the LDO, thereby increasing ϕ_M focusing on performance at low currents. Further improving the response accuracy as well as load range a current amplification buffering stage is proposed. The design improves upon common LDO typologies for both ϕ_M and I_Q by increasing the loop phase around the unity gain frequency (UGF). By tracking the output pole, the design is also able to maintain this phase increase over the full load range of 0 - 50 mA.

Chapter 2

BACKGROUND

The purpose of voltage regulation circuits is to isolate a device from any changes in supply while providing constant voltage with changes in load. These line and load variations act as undesirable non-ideal characteristics of typical running conditions for circuits in operation. The fundamentals of designing a low-dropout voltage regulator is presented in this chapter. First, exploring the challenges in keeping a supply purely DC. Then, breaking apart what a voltage regulation circuit is and typical topologies. Finally, an introduction into feedback and control theory will form an understanding of how these circuits are implemented.

2.1 Importance of Supply Voltage

When engineering any product, we must deeply consider the applications that the design must operate within. Civil engineers must specify load conditions for a beam, mechanical engineers, how much boost an engine is capable of. In electrical engineering, every device has operable qualities that determine the cases for which a design will maintain operation to a good degree. The supply of a device is a large source of these operable conditions. An ideal DC supply is a perfectly consistent invariable voltage rail. However, a device can experience many changes to its supply voltage and will react differently to each of them. In [13] a

Table 2.1: Effects of Supply Voltage Changes on Circuits

No.	Supply Voltage Error	Description of Occurrence	Effect on Circuit
1.	**Overvoltage**	Voltage supply greater than nominal by a large margin.	Component overstress, possible breakdown, reduced lifespan, excessive heat dissipation.
2.	**Undervoltage (Brownout)**	Voltage supply much lower than nominal.	Inadequate performance, higher current draw, failure to operate.
3.	**Outage (Blackout)**	Commonly described in AC device operation as loss of voltage for multiple cycles, less common in DC.	Device ceases operation, device failure on restart.
4.	**Voltage Sag**	A slight decrease in supplied voltage over a short duration.	Temporary undervoltage, decreased efficiency, malfunction during transient events.
5.	**Voltage Spike**	A slight increase from nominal supply voltage for a short duration.	Short-term overvoltage, potential damage to components, data corruption, circuit reset or latch-up.
6.	**Voltage Ripple**	The result of AC-DC and DC-DC conversion, caused by rectification or switching.	Variability in power consumption, compounds other voltage changes, unreliable operation.
7.	**Voltage Drift**	Slow changes in voltage level over a long-period.	Long-term instability, calibration issues, parameter shifts in analog circuits, including nonlinearity.
8.	**Noise**	Distortion of the nominal supply voltage caused by noise.	Signal distortion, unreliable operation, potential interference with sensitive components.

description of these power management considerations of given and summarized in Table 2.1.

In ideal conditions, a voltage regulator would consistently give a single specified output with complete rejections of any variations such as line changes or noise. What we must do, is attempt to match reality with the closest approximation of the ideal. Therefore, voltage regulators attempt to be invariant to a wide variety of stimuli. The key to this regulation is feedback. Feedback is a pivotal technique in delivering sustained nominal voltage to devices and this is the purpose of this thesis. Let's now focus solely on electronics with this analogous understanding in place. With a circuits performance heavily dependent on it's supply voltage there must be systems in place to remove as much variability and aim towards

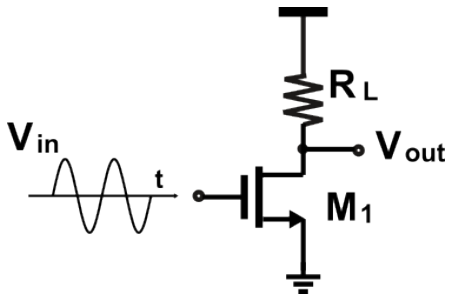


Figure 2.1: Simple common source amplifier.

as much of a theoretical ideal DC source as possible.

Let's consider a simple common-source, metal oxide semiconductor field-effect transistor (MOSFET) amplifier with a resistive load as shown in Fig. 2.1. We know that to effectively amplify the input AC small signal, the NMOS transistor, M_1 must be biased to operate in the saturation region. This achieves the maximum voltage gain. To meet this requirement, the voltage between gate and source V_{gs} must be greater than the threshold voltage V_{th} of M_1, furthermore, for headroom requirements to be met, the output voltage must be greater than the saturation voltage of M_1, $V_{out} \geq V_{dsat}$. It's important to recognize that V_{out} is heavily dependent of V_{DD}, meaning large variations in V_{DD} creates large variations on V_{out}. The worst case is if M_1 exits saturation causing gain of the amplifier to be reduced and performance to be poor. Maintaining constant supply voltage is highly desirable, however challenging.

In addition to analog circuits, the effects of supply voltage variations must also be considered in digital circuits, particularly in a CMOS inverter such as that in Fig. 2.2 comprised of a PMOS transistor, M_1, and an NMOS transistor, M_2. The inverter operates by switching M_1 and M_2 between their respective on and off states, thereby toggling the output between high and low logic levels. However, variations in the supply voltage V_{DD} can significantly affect the operation of these transistors. For instance, if V_{DD} increases, the threshold voltage of M_1 may decrease slightly, causing M_1 to turn on more easily. Conversely, M_2

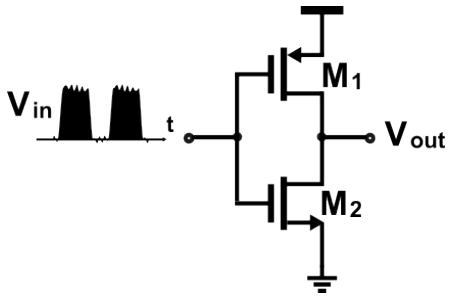


Figure 2.2: Simple inverter.

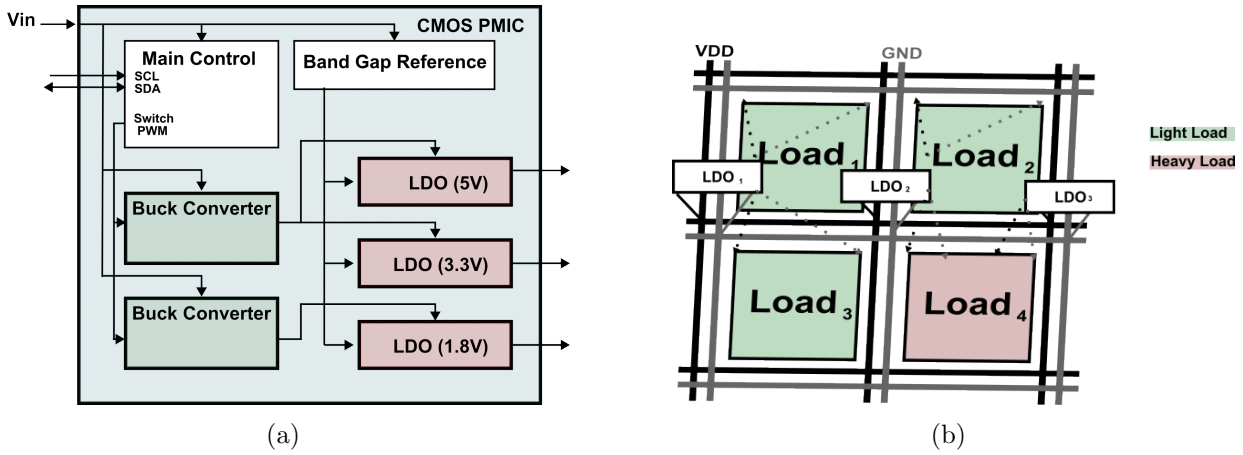
might require a higher gate-to-source voltage to turn on, altering the balance between the transistors. This imbalance can shift the inverter's switching threshold, where the output transitions from high to low, potentially causing incorrect logic levels. On the other hand, a decrease in V_{DD} can result in M_1 turning off prematurely or M_2 failing to turn on fully, leading to incomplete switching and slower operation. In both scenarios, the inverter's ability to accurately distinguish between logic '0' and logic '1' is compromised, increasing the susceptibility to noise. This can push the input signal above or below its threshold, potentially resulting in erroneous logic levels being interpreted, which jeopardizes the integrity of data transmission in digital circuits.

2.2 Voltage Regulation

Voltage regulator's ideally ensure constant voltage supplied to a load, regardless of changes at the input or output of the system. As a key building block of all power management devices, voltage regulators are a common topic in literature, specifically for their applications in SoC devices. Since we are in the era of battery powered portable devices, the need for small fully-integrated CMOS circuits is constantly growing. Therefore, the introduction of CMOS linear regulators was an important step in SoC fabrication. The demands of such SoCs is that of efficiency, reliability and protection. This section explains the functions of such devices, the essential starting point of a design, and specifically how a CMOS

linear regulator functions.

An SoC device operates by use of many different power management techniques being combined to feed each of its internal circuits. For example, an SoC could have three operating voltages, a 5 V, 3.3 V and 1.8 V rail all for different applications within the device. Furthermore, having the ability to enable and disable each of these lines is becoming a standard as wearable and portable devices require highly optimized PMICs. For this same reason, low I_Q devices are more in demand. Modern systems now utilize a more sophisticated power grid, demonstrated in Fig. 2.3, along the nodes of the grid is a power regulator, feeding to many devices within the interior of the grid array. The benefit of this is minimization of travel distance, along with added parallelization. This does increase the space utilization however and so designers must be aware of their layout optimization. SoCs benefit from the advancements that have been made in the state of the art for power management and it continues to be a relevant topic of research discussions today.



(a) (b)

Figure 2.3: (a) Implementation of LDO on a CMOS PMIC device, and (b) an ASIC power-grid.

The available topologies for electrical voltage regulation vary widely. A primitive voltage regulator can be achieved using the reverse biasing characteristics of a diode's PN junction. Commonly referred to as zener diodes, these diodes leverage breakdown voltage

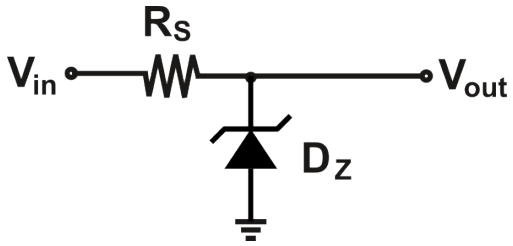
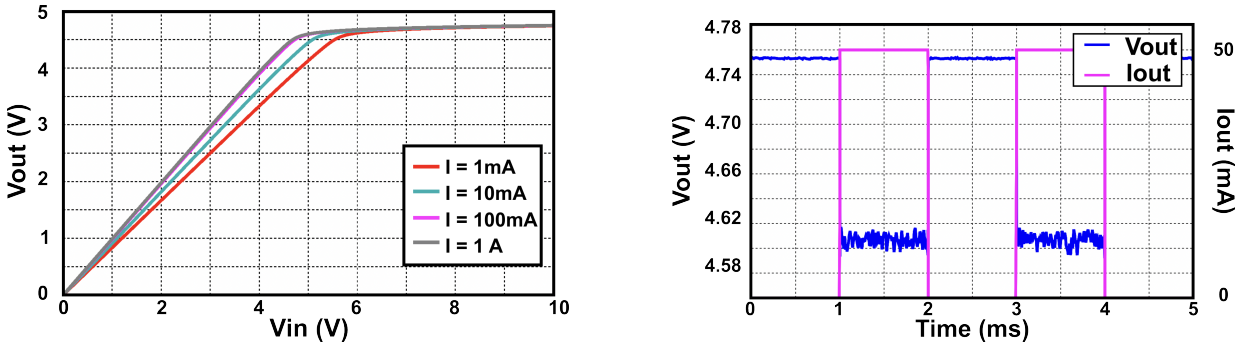


Figure 2.4: Zener regulator.

which when applied produces the so called avalanche current, conducting in reverse bias of a standard diode. This avalanche current has a non-linear relationship between output current and applied voltage, effectively allowing for a basic regulated voltage ideally independent to load. This voltage regulator has disadvantages however, since the physical properties of the PN junction dictate operational qualities such as the biasing voltage, these regulators are critically dependent on the material properties, such as doping, of the PN junctions. Noise suppression is minimal, as noise can pass directly to the output without isolation, or rejection. Furthermore the diode has to be reversed biased, held at a certain breakdown voltage, increasing the headroom required to operate the device. Finally diode circuits are susceptible to small changes such as changes in temperature, and changes in load current producing changes in output voltage.

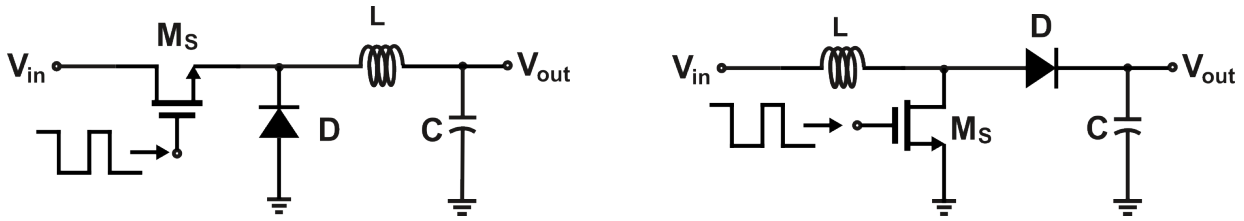
Figure 2.4, gives an example of how this simple circuit is created and 2.5 (a) shows the DC sweep of the input voltage, with varied loads. This gives us an idea of how much headroom is required for stable operation. There is a clear voltage dropout, being the difference between operating input and output, which is higher at larger loads. Finally figure 2.5 (b) shows the transient operation of this circuit swinging from 0 to 50 mA with noise and voltage fluctuations present at the input voltage. It is clear that the device, although capable of fast transient responses, has relatively large voltage swing and is not suited for all applications. This introduces the need for more complex regulators.

The logical next step in need is a circuit which can be more easily adjusted. By introducing passive components in conjunction with more active switching circuitry, an out-



(a) (b)

Figure 2.5: The (a) DC characteristics of a zener regulator and (b) its transient response including noise.



(a) (b)

Figure 2.6: (a) Buck and (b) boost switching regulators.

put voltage can effectively be held above, below, or inverted to that of the input. These circuits function by using a capacitor in parallel with the output of adequate size that, once initially charged, it will hold more or less the desired output voltage independent to load. A switch configured transistor, generally a field effect transistor (FET) is used to control the charge on and off time. A diode controls the direction of current flow and allows for current circulation into the cap. Inductors are added for use of their high current discharge, which is attributed to the collapse in EM field that the component attempts to maintain. This property means the inductor has the ability to produce voltages higher (Boost) and substantially lower (Fly-back) than that of the input. The typical circuit topology for the commonly used buck and boost switching configurations is presented in Fig. 2.6.

These devices are adjustable with the duty cycle and frequency of the switching, surpassing the functionality of the diode regulator with the added circuitry required. It is

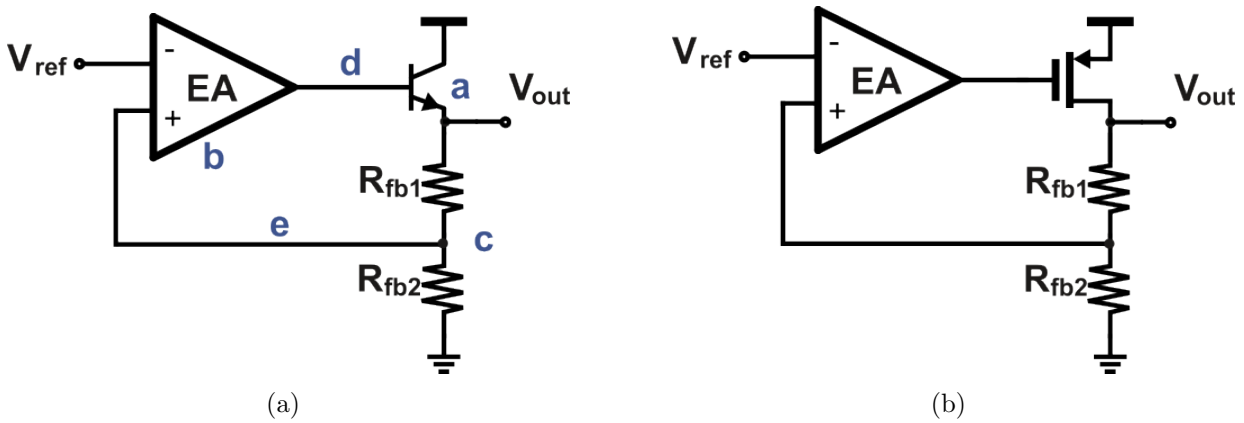
also not uncommon to see further functionality with these circuits with the introduction of negative feedback management ICs. These ICs will compare the output voltage to that of a reference and alter the switching for a more accurate output with changes in input and load. These devices benefit from high efficiency with a minimal number of components and less resistances, energy transfer and thermal loss is reduced. However these devices suffer from poor noise performance since nearby switching circuitry will interfere with stable output voltages, along with the addition of the ripple from the charge and discharge of the capacitor at the output. Finally, as mentioned ICs are needed to convert a compared voltage into a duty-cycle feedback to the switch which is added complexity and further design to the engineer. For applications of low I_Q this circuitry means a DC-DC converter will struggle to perform to the specifications of wearable devices, further, the need for large passive components means these devices cannot be easily produced in a CMOS IC technology.

2.3 Linear Regulators

Voltage regulators, such as those presented in Fig. 2.7, solve many of the issues tabulated in table 2.1. By utilizing a differential amplifier with a reference voltage input, the differential pair effectively reduces the amount of common mode noise, often associated with supply ripple, present at the output. With the introduction of negative feedback, voltage regulators can also sense changes between the referenced voltage, and the voltage present in the current sensing network. Regardless of where a voltage fluctuation is presented, the device should be capable of reducing variations even when transient events occur. Drift is easily prevented with adequate headroom for proper operation, as slow changes in voltage require the least amount of circuit performance to reduce. While sharp transitions, perhaps caused by a sudden load change, can be countered by a well compensated feedback network.

Typically there are two solutions for voltage regulation, linear regulators Fig. 2.7 (a), and low-dropout (LDO) linear regulators, Fig. 2.7 (b). Essentially formed from the same internal blocks, however with the alteration of the *a.* pass-element in an LDO the headroom

required is much lower than a basic bipolar junction transistor (BJT) regulator. The rest however is shared, being *b.* an error amplifier *c.* a resistive current sensing network, and where the *d.* gate or base-driving circuitry and *e.* compensatory circuitry would be inserted in a design.



(a) (b)

Figure 2.7: Two typical topologies, (a) linear regulator, and (b) LDO.

The subtle difference between the typical linear regulator, and a low-dropout regulator as mentioned is the so called pass element, named so for passing the current to the load. The pass element can be comprised of many different elements, NMOS cascode configuration and a single PMOS commonly are the elements used in a proper LDO. The benefit of using a MOS device is such that the headroom of the device can be much smaller than a typical linear regulator utilizing a BJT or other method. The reason for this being that a MOS field effect transistor (MOSFET) operates with a smaller voltage drop when on (R_{ds}) than an equivalent BJT device. With this drop being smaller, less current is consumed and overall the performance in terms of efficiency is increased. Furthermore a benefit of utilizing a MOSFET is that these components are voltage driven, as compared to a BJT which is current driven. This causes a larger amount of current to constantly need to flow through the pass element of a linear regulator which uses a BJT as compared to an LDO utilizing a MOSFET. Once the gate capacitor is charged, there is little to no current which flows into

the device as waste energy.

2.3.1 Pass Elements

An essential component in linear regulators, is the pass element, with the common topologies demonstrated in Fig. 2.8. As mentioned, the component which dictates the nomenclature used to describe the regulator is the pass element. A device which uses a MOSFET has a much lower dropout voltage than BJT equivalents and therefore is considered a low-dropout regulator. The pass element can be either a MOS or BJT device of differing designs. A simple PMOS can be used, with a single transistor being the device which passes current to the load. With the voltage-current characteristics of a PMOS being inverse to that of an NMOS a simpler topology can be used whereas to utilize an NMOS, a cascaded configuration is required. NPN configurations are the same in that they require a PNP feeder transistor to operate, however these topologies have strong current carrying capabilities and with use of a super-beta transistor or darlington configuration can have improved speed to that of even MOS devices.

The pass element also dictates key characteristics of the regulator with table 2.2 tabulating the common performance metrics of each pass shown in Fig. 2.8. The threshold voltage (V_{th}) of the pass element determines the V_{DO} of the regulator which is difficult to adjust as it is dependent on many factors including the C_{ox} or gate oxide capacitance, as well as the depletion region charge or Q_{dep}, which are both intrinsic to the material properties of the doped silicon. Furthermore the I_Q is given by the gate leakage of the pass element as this is the largest transistor in a linear regulator design. As the device size increase the stability is also effected since the output pole is directly proportional to the R_{on} and C_{par}, this will be discussed further in Section 2.4.

In power electronics and specifically linear regulator design the material science of the structure has a large part to play in the operation of a device. Recently, researchers

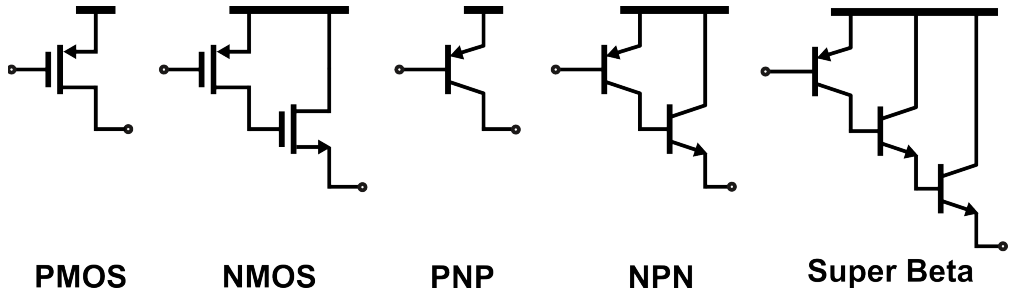


Figure 2.8: Typical linear regulator pass elements.

Table 2.2: Comparison of Pass Element Structures

Parameter	PMOS	NMOS	PNP	NPN	Super Beta (NPN)	NMOS (SiC)
Transient Performance	Medium	Medium	Slow	Fast	Fast	Fast
Accuracy	High	High	Medium	Medium	Medium	Medium
$\boldsymbol{V_{DO}}$	V_{dsat}	V_{dsat}	V_{ecsat}	V_{cesat}	$V_{cesat} + 2V_{be}$	$V_{gs} + V_{th_{SiC}}$
$\boldsymbol{I_Q}$	Low	Low	High	Medium	High	Medium
$\boldsymbol{I_{max}}$	Medium	Medium	High	High	High	High
PSRR	Medium	Medium	Low	Medium	High	High
Noise	Low	Low	High	Medium	Medium	Low
Thermal Performance	Good	Good	Moderate	Good	Good	Excellent

have been experimenting with the emerging technology of silicon carbonate (SiC) NMOS technologies [14–16]. With the advantage of high thermal capabilities and high switching speeds, these devices have strong performance in 100°+ environments where high output voltage and current is also required. These advancements are few to explore, specifically for linear regulator research. The voltage threshold in standard operation is higher than that of Si devices [17] ranging from 2 V - 6 V, however as temperature increases this threshold drops substantially. Another property of SiC devices is that they have much higher gate leakage than Si MOSFETs, reducing their low quiescent current capabilities.

2.3.2 Low-Dropout Regulators

LDO regulators are catagorized by their use of an output capacitor. This is indicated by the notation of being a cap-less, or a design without use of an off-chip capacitor, and

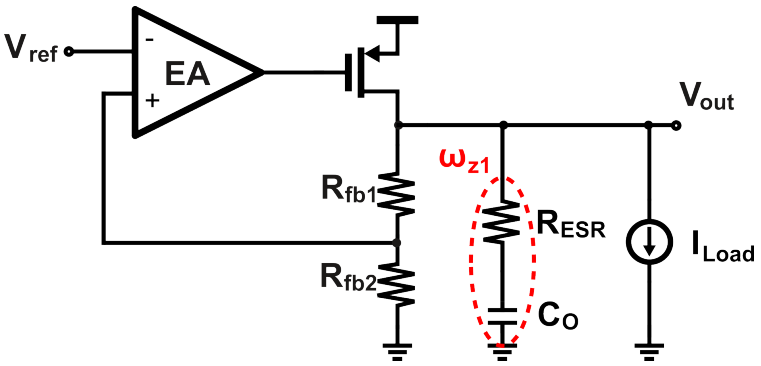


Figure 2.9: Typical ESR LDO schematic.

a typical LDO which uses an off-chip capacitor to extend stability by introducing another zero. When observing the transfer-function associated with an ESR LDO such as that in figure 2.9 there is an added zero and pole created by the output capacitor,

$$H(j\omega) = \frac{V_{out}}{V_{in}}(s) = \frac{A_{ol}}{\beta} \cdot \frac{(C_O R_{ESR} s + 1)}{\left(C_{G_p} R_{out_{EA}} s + 1\right)\left(C_O \left(R_{ESR} + r_{op}\right) s + 1\right)}, \tag{2.1}$$

with the transfer-function demonstrating the following poles and zeros,

$$\omega_{p0} \approx \frac{1}{C_O r_{op}}, \tag{2.2}$$

$$\omega_{p1} = \frac{1}{\mathrm{C_{G_p}\, R_{out_{EA}}}}, \tag{2.3}$$

and

$$\omega_{z1} = \frac{1}{\mathrm{C_O\, R_{ESR}}}. \tag{2.4}$$

The zero is produced by having an equivalent series resistance (ESR), generally ranging from 10Ω to 0.01Ω. In conjunction with the capacitance, this ESR produces a frequency-dependent path to ground and therefore a zero, which alters the frequency response of the LDO, generally improving stability.

To fully understand the role of ESR in Low Dropout Regulators (LDOs), it's essential to recognize its impact on the stability and performance of the regulator. The ESR of the output capacitor directly influences the placement of the zero and additional poles in the LDO's frequency response. A proper selection of ESR can enhance the phase margin by creating a zero at a frequency where the phase lag introduced by the internal poles of the LDO is significant, thus improving stability. Conversely, if the ESR is too low, typically below 0.01Ω, the zero might occur at a very high frequency, providing insufficient phase boost where needed, leading to potential instability. On the other hand, if the ESR is too high, exceeding 10Ω, it can introduce an additional low-frequency pole which can dampen the response excessively and degrade transient performance.

Furthermore, the interaction between the ESR and the LDO's internal compensation network is crucial for optimal performance. One must balance the ESR with the LDO's compensation to achieve the desired frequency response, particularly in applications with varying load conditions. This balance is particularly significant in applications with varying load conditions, where the dynamic behaviour of the regulator is critical. Therefore, selecting the appropriate output capacitor with the right ESR value is a key design consideration in ensuring the LDO operates reliably across different operating conditions. The correct ESR helps in shaping the frequency response to mitigate the adverse effects of load transients and input noise, thereby maintaining a stable and robust power supply.

2.3.3 Performance Metrics

Linear regulators have many key metrics to display their performance. A primary parameter especially in LDO design is the voltage dropout, measured by the minimum difference between the input voltage (V_{IN}) and the output voltage (V_{OUT}) for which the LDO can still regulate the output voltage. The dropout defines the headroom required for operation and is dictated by the pass element. As the pass element exits saturation and

enters the triode region the MOSFET begins to act as a resistive element, given by R_{ds} or R_{on}. Demonstrated thorugh this equation,

$$V_{DO} = I_{out} \cdot R_{on} \tag{2.5}$$

the dropout definition which can further be expanded knowing the triode resistance model as given by [18]. Equation 2.6 shows that as the aspect ratio, or $\frac{W}{L}$ is increased, the dropout will decrease. This however leads into a key compromise where the size of the output pass element affects the stability as well as the quiescent current of the device. This is expressed in the "on" resistance equation as follows,

$$R_{on} = \frac{1}{\left(\mu_p C_{ox} \frac{W}{L}(V_{SG} - V_{th})\right)} \tag{2.6}$$

where, μ_p is the mobility of holes, C_{ox} is the oxide capacitance per unit area, $\frac{W}{L}$ is the aspect ratio of the transistor, V_{SG} is the source-gate voltage, V_{th} is the threshold voltage.

Furthermore, especially in the case of this design, quiescent current is a key metric. Defined as the current utilized by the LDO and not passed to the load, quiescent current is expressed as

$$I_Q = I_{IN} - I_{LOAD}. \tag{2.7}$$

Since LDOs are voltage driven devices, they do not suffer from proportional current draw to that of the output, unlike traditional BJT linear regulators. This however is less true in a fast switching situation, as the gate capacitor needs to be charged and discharged for each swing in load current. This, in combination with all of the other gate capacitances (C_g), leakage currents from wide transistors, and the current draw from the current sensing resistive feedback network as well as all biasing needed, causes the quiescent current to increase quickly unless specifically targeted as an important metric. A design can perform

well, however can draw much more current than other topologies because it has not been optimized.

Stability of an LDO is also critical, as this will show a designer essentially an expected ability of the circuit to not oscillate, and to respond effectively to transients experienced by the device. Be it load or line changes. There are many figure to show this stability, however in the literature it is common to see this expressed by the phase margin, or ϕ_M of the LDO,

$$\phi_M = 180^\circ + \angle H(\omega) \tag{2.8}$$

where $\angle H(\omega)$ is the phase of the open-loop transfer function of the LDO given by,

$$\angle H(j\omega) = tan^{-1}\left(\frac{\Im\left(H(\omega)\right)}{\Re\left(H(\omega)\right)}\right) \tag{2.9}$$

using the transfer function of the open loop to express the amount of phase a signal can change before the feedback signal phase is 180° or 0°. A deeper exploration into the reason this feedback is important and will be in chapter 2.4. Moving forward, let's express the typical transfer function in an ESR LDO. The transfer function is expressed in (2.1) and shows us the parameters that can increase ϕ_M. Importantly, the A_0 of the AC gain of our system is inversely proportional to the base ϕ_M. The drawback to altering the AC gain in attempt to increase stability is that the system operates slower, is less accurate, and will reject noise poorly.

The small signal model is an important starting point when analyzing performance of an LDO. The small signal transfer function is utilized in understanding how the LDO will perform with varied AC inputs. A Bode plot can be produced with use of these functions, giving us the locations where frequency response will drop, the bandwidth of the system, the DC and AC gain, and the margins for operation. However, in application device data sheets will not show the transfer function, or the phase margin or stability figures. Stability is a

metric used for designers and researchers to quantify contributions to a topology, generally this is not used in practice as transient responses will depict performance visually.

For example, line regulation is a measure of an LDOs ability to maintain a constant output voltage despite variations in the input voltage. When a voltage sag, spike or drift occurs the LDO must quickly adapt and resume nominal voltage at the output. In the case of a transient event, any overshoot or undershoot experienced at the output is the measure of performance. The less deviation from nominal an LDO produces the better for devices it is regulating. This performance is often expressed in $\frac{mV}{V}$ and is calculated in,

$$\text{Line Regulation} = \frac{\Delta V_{out}}{\Delta V_{in}} \approx \frac{1}{\beta}\left(\frac{g_{mp} r_{op}}{A_{ol}} + \frac{\Delta V_{ref}}{\Delta V_{in}}\right) \tag{2.10}$$

by the change in voltage out over in. Furthermore much like line regulation, another transient event which can occur is changes in load.

The ability for an LDO to regulate changes in output amperage is known as load regulation and is given usually in the units $\frac{mV}{mA}$,

$$\text{Load Regulation} = \frac{\Delta V_{out}}{\Delta I_{load}} \approx \frac{r_{op}}{1 + A_{ol}\beta}. \tag{2.11}$$

Small changes over a long period generally do not tax LDO performance, therefore datasheets will present full-load swing metrics as this is the worst case. Additionally, the faster the event occurs, the more difficult it is for an LDO to adapt to the change, so edge-time as it is known is important in this respect. Both (2.10) and (2.11) demonstrate how the feedback and open loop gain affect the performance of the LDO. These parameters however if increased can negatively affect stability of the system, as presented in (2.1) the transfer function of a typical ESR LDO.

Power Supply Rejection Ratio (PSRR) quantifies the ability of the regulator to suppress variations in the input supply voltage from appearing at the output. High PSRR

indicates effective isolation of the output from input noise, ensuring a stable and clean output voltage. PSRR is primarily controlled by the error amplifier, the pass transistor, and the feedback network. The error amplifier's bandwidth and gain play a significant role in determining the PSRR at different frequencies, with higher gain generally improving low-frequency PSRR. The pass transistor's characteristics, including its intrinsic gain and capacitance, influence the high-frequency PSRR. Furthermore, the output capacitive network helps to filter out high-frequency noise. Given by,

$$PSRR = 20 \log \left(\frac{\Delta V_{IN}}{\Delta V_{OUT}} \right) \tag{2.12}$$

where PSRR is given as a dB ratio.

2.4 Feedback Techniques

In analog systems, feedback is a fundamental concept used to improve the performance of circuits by making them less sensitive to variations in component values, temperature, and other external factors. Feedback works by feeding a portion of the output signal back to the input, either in phase as positive feedback or out of phase as negative feedback. Negative feedback, such as that depicted in Fig. 2.10, is widely used because it stabilizes the gain of the system, reduces distortion, and enhances bandwidth. Mathematically, the closed-loop gain $\frac{V_{out}}{V_{in}}$ of a feedback system can be expressed as,

$$\frac{V_{out}}{V_{in}} = \frac{A_O}{1 + A_O \beta} \tag{2.13}$$

where A_O is the open-loop gain of the system, and β is the feedback factor. The feedback reduces the effective gain of the system but makes it more stable and less sensitive to variations in A_O.

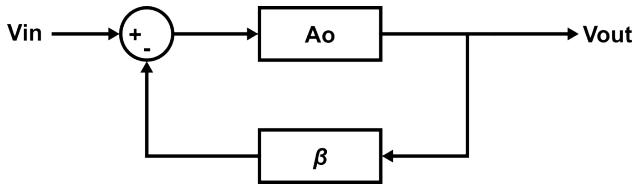


Figure 2.10: Negative feedback system.

However, introducing feedback into a system also raises concerns about stability. Stability is the ability of a system to return to equilibrium after a disturbance. In the context of feedback systems, stability is closely related to the phase shift introduced by the loop. According to the Barkhausen criteria, for a system to oscillate, two conditions must be met. The magnitude of the loop gain $|A_O(\omega)\beta(\omega)|$ must equal 1 (or 0 dB), and the phase shift around the loop must be an integer multiple of 2π radians (360°). This can be mathematically expressed as,

$$|A_O(\omega)\beta(\omega)| = 1 \quad \text{and} \quad \angle A_O(\omega)\beta(\omega) = 2\pi n. \tag{2.14}$$

When these conditions are met, the feedback becomes positive, causing the system to oscillate. This is because, as the feedback signal is in phase with the input it leads to a reinforcement of the input signal and an eventual runaway condition where oscillations build up.

To prevent instability, the phase margin and gain margin of the system must be carefully managed. Phase margin is defined as the difference between the actual phase shift at the unity gain frequency (UGF) and $-180°$. A larger phase margin indicates greater stability, as it implies that the system has a buffer before the phase shift reaches the critical $-180°$ point where oscillation could occur. Gain margin, on the other hand, is the factor by which the gain can increase before the loop gain reaches unity at the frequency where the phase shift is $-180°$. Ensuring adequate phase and gain margins is essential in analog circuit design to maintain stability while achieving the desired performance characteristics.

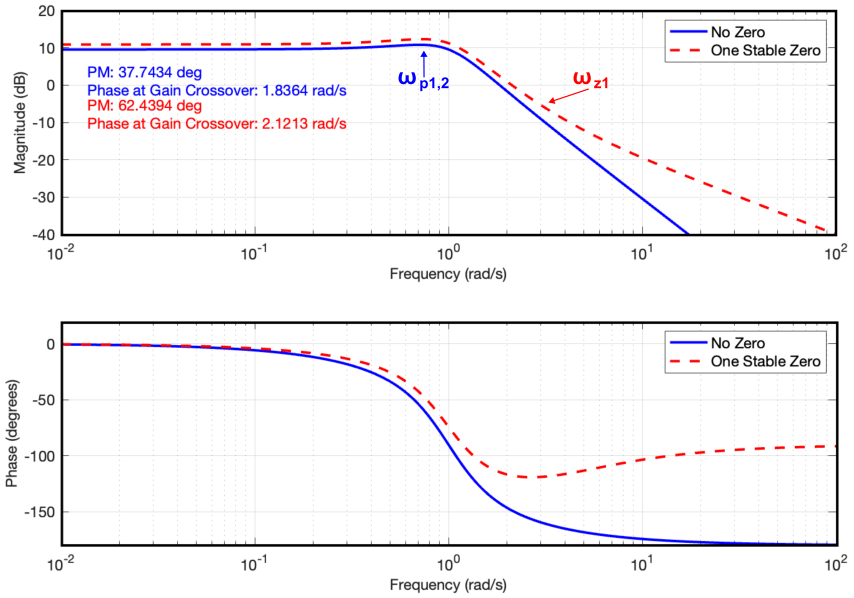


Figure 2.11: Bode diagram comparing a traditional LDO with ESR, shown in red and an LDO without, shown in blue.

There is a large body of work in the modern literature that depicts methods for stabilizing and improving the response an LDO has to stimuli. When a step change in line or load occurs, such as a load step from 0 mA to tens of mA or more which is common in SoC designs, the LDO will respond. The output of a poorly stabilized system will have overshoot, undershoot, drift, and or oscillation in the worst case. To combat these issues, LDOs will have a capacitor at the output, introducing a zero in the control loop, utilizing the capacitance and its equivalent series resistance (ESR), the stability added is clearly visible in Fig. 2.11 where ϕ_M is increased by 24.69° with this technique. This technique will add stability to a two pole LDO, however a two pole system is not suitable for introducing miller compensation. Because the poles are close to DC, pole-splitting cannot be implemented adequately, unless the internal miller capacitor is very large. This is not the case however in a three pole system, where a buffer is inserted before the power transistor's gate. This allows for a design to have many more options available in stabilizing the loop. Therefore, an important consideration in this work is finding a method to increase stability of a feedback

network while generally keeping the circuit efficient.

2.5 Literary Review

Low-Dropout (LDO) voltage regulators with off-chip capacitance (C_O) are widely used, comprehensively studied devices frequently utilized in microelectronic architectures; specifically for battery-powered System on Chip (SoC) applications requiring low power consumption, fast load regulation response time and stability over a wide range of loads. Typically, Analog LDO (ALDO) designs have measurably lower quiescent current (I_Q) as compared to both Hybrid LDOs (HLDO) and Digital LDOs (DLDO) [19]. ALDOs, however, suffer from stability issues at low load currents. Traditionally a zero is added to the control loop by use of a bulky external C_O and its associated Equivalent Series Resistance (ESR) [20]. Fig. 2.9 demonstrates the conventional topology of such LDOs. The zero associated with the ESR increases the Unity Gain Frequency (UGF) while adjusting phase of the loop at that point to increase Phase Margin (ϕ_M) of an LDO.

Frequently, to extend this stable range, compensation networks within the LDO itself are utilized [21–27], Using a Miller capacitor, the frequency response can be shaped to create a loop gain which acts like that of a single pole system above UGF [18]. LDOs utilizing ESR compensation typically operate as a three-pole high-gain loop. However, the zero associated with the C_O and its ESR do not change with load, unlike the pole at the output which is a function of load current. Therefore tracking that pole is required for high ϕ_M over a larger stable range.

An impedance-attenuated buffer stage which employs a current-buffer compensation network to increase the ϕ_M to above 65° is proposed in [25]. By reducing the output resistance of the buffer between the error amplifier and the power stage, the pole associated with the gate of the pass device is moved to high frequencies, which is negligible. The reported

design can support large load changes. However, the inevitable large current during no-load applications limits its application. Fu *et. al.* [26] proposed a multiple loop LDO of which the PM was improved significantly while it suffers from high quiescent current.

To summarize the improvements present in the decades of LDO research, Fig. 2.12 [28–89] tracks the progression of Figures of Merit (FoMs) with adjustments for technology node improvements,

$$(FoM) = \left(\frac{\Delta V_{out} C_{out} I_Q}{{I_{max}}^2}\right) \cdot \left(\frac{1}{L_T}\right) \tag{2.15}$$

where L_T is the technology node used. The data shows a consistent improvement in FoM by approximately an order of magnitude, indicating significant advancements in LDO design and topology optimization. This figure emphasizes the importance of continued innovation in LDO design, and the contributions of this work build on these advancements to push LDO performance further.

2.5.1 Pole Tracking and Substitution

Stability of an LDO changes as current at the load changes. This is due to the dependency the output pole has with the transconductance of the pass element. Generally, this will mean that at lower currents, an LDO looses ϕ_M, therefore reducing stability. There are many unique solutions to this issue. In [21] (Fig. 2.13), a load tracking-zero compensation network is proposed, using a combination of the internal Miller capacitor and a series pMOS which is controlled by a voltage associated with the output pass-transistor. Thereby subverting limitations of ESR compensation. It effectively allowed for a ϕ_M of 44° and 111° under the no-load and full-load while maintaining a low I_Q of 7.5 μA.

In [90] (Fig. 2.14), the authors proposes an improved LDO topology which utilizes a 3-input differential amplifier with signal-current feedforward and amplification which generates a low frequency zero canceling the dominant pole of the system. By doing so the design was able to expand the UGF of the system adjusting the knee point from 9.44 kHz

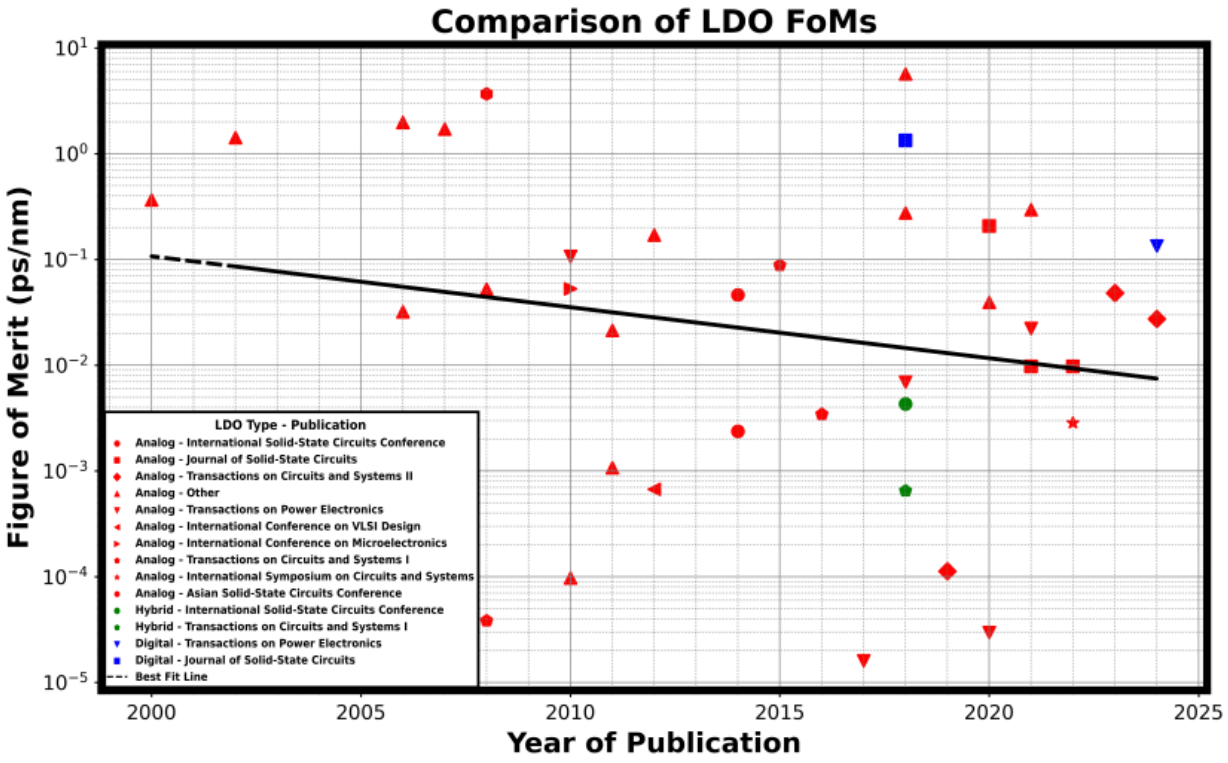


Figure 2.12: Comparing FoMs from two decades of LDO design and their type and publication source.

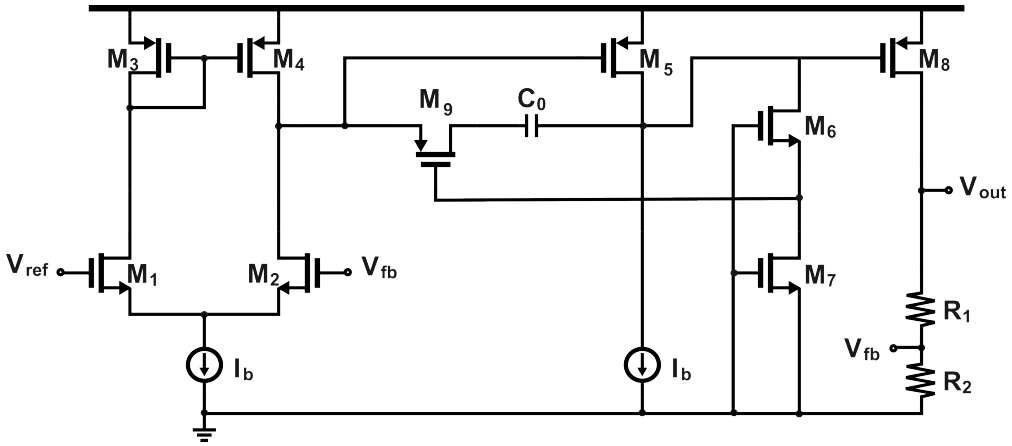


Figure 2.13: Zero Tracking LDO proposed by I. Subbiah *et. al.*

to 16.8 kHz. Overall the design is an intelligent method of extending available frequency response room while remaining simple at the high level. The issue which arrises from this expanded design is that the system has the largest quiescent current draw of all circuits that

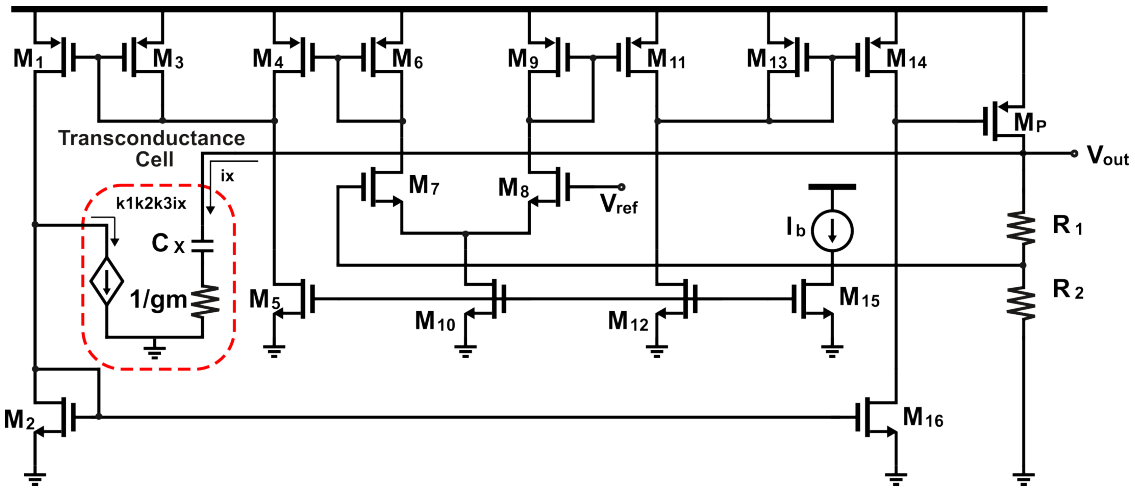


Figure 2.14: Dominant pole substitution LDO proposed by M. Ho *et. al.*

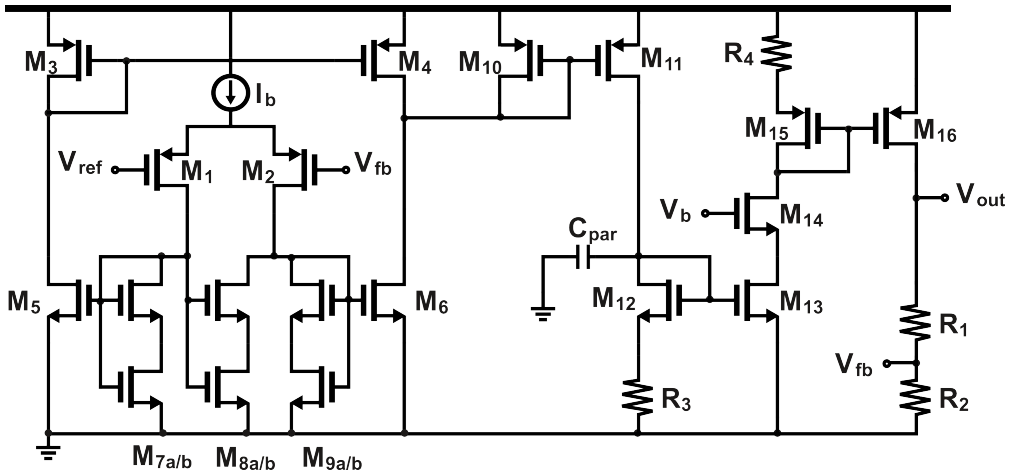


Figure 2.15: Pole tracking LDO proposed by X. Ming *et. al.*

are presented in the report. The extended response means that this design has a very strong ability to react to high current load changes with a drastically reduced settling time and a noticeable reduction on overshoot.

Approaching the state of the art, in [22] (Fig. 2.15), a current-efficient fast-transient LDO with an advanced pole tracking technique achieves good loop stability, without degrading chip area and current efficiency. The design recognizes that the dominant output pole shifts with load current, and proposed a solution which adapts a load resistor controlled

error amplifier to change the output load of the EA to reduce dependence on the ESR at the output. The circuit is state of the art, utilizing many speed increasing techniques including transconductance amplification. However this design suffers from the high demand of no load quiescent current draw, making its applicational uses limited.

2.5.2 Low I_Q

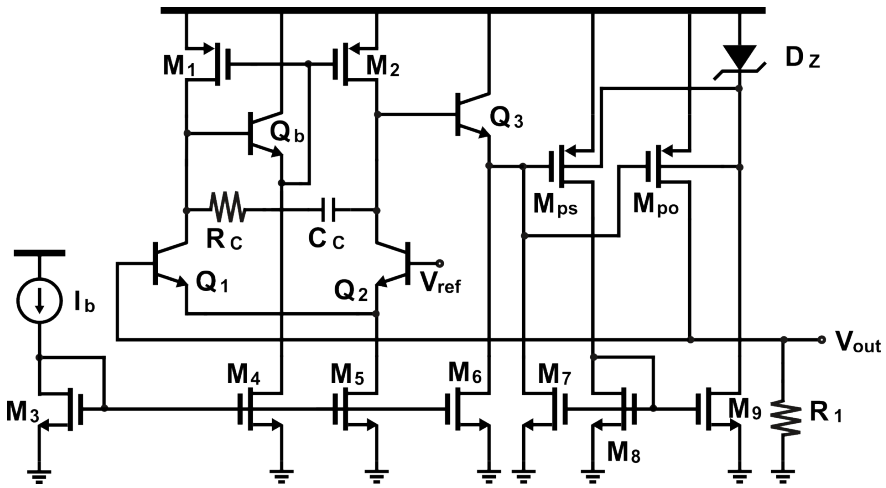


Figure 2.16: Original low I_Q LDO proposed by G. Mora and P. Allen in 1998.

Low I_Q designs for LDOs have been a prominent area of research with Mora and Allen [20] (Fig. 2.16) being one of the first to discuss the topic in an IEEE article. This article, published in 1998, is already bringing up the topic of battery operated cellular phones requiring low power consumption LDOs for their power management. Their solution was to utilize a current efficient buffer and current boosted pass device. With these techniques introduced their current was 23 μA which is about half of that of other LDOs of the era. Further development would be made in the next decade with more experimentation into using solely MOSFETs for implementation in CMOS ASIC devices. As discussed BJTs have to consume current to be active and this reduces current efficiency overall.

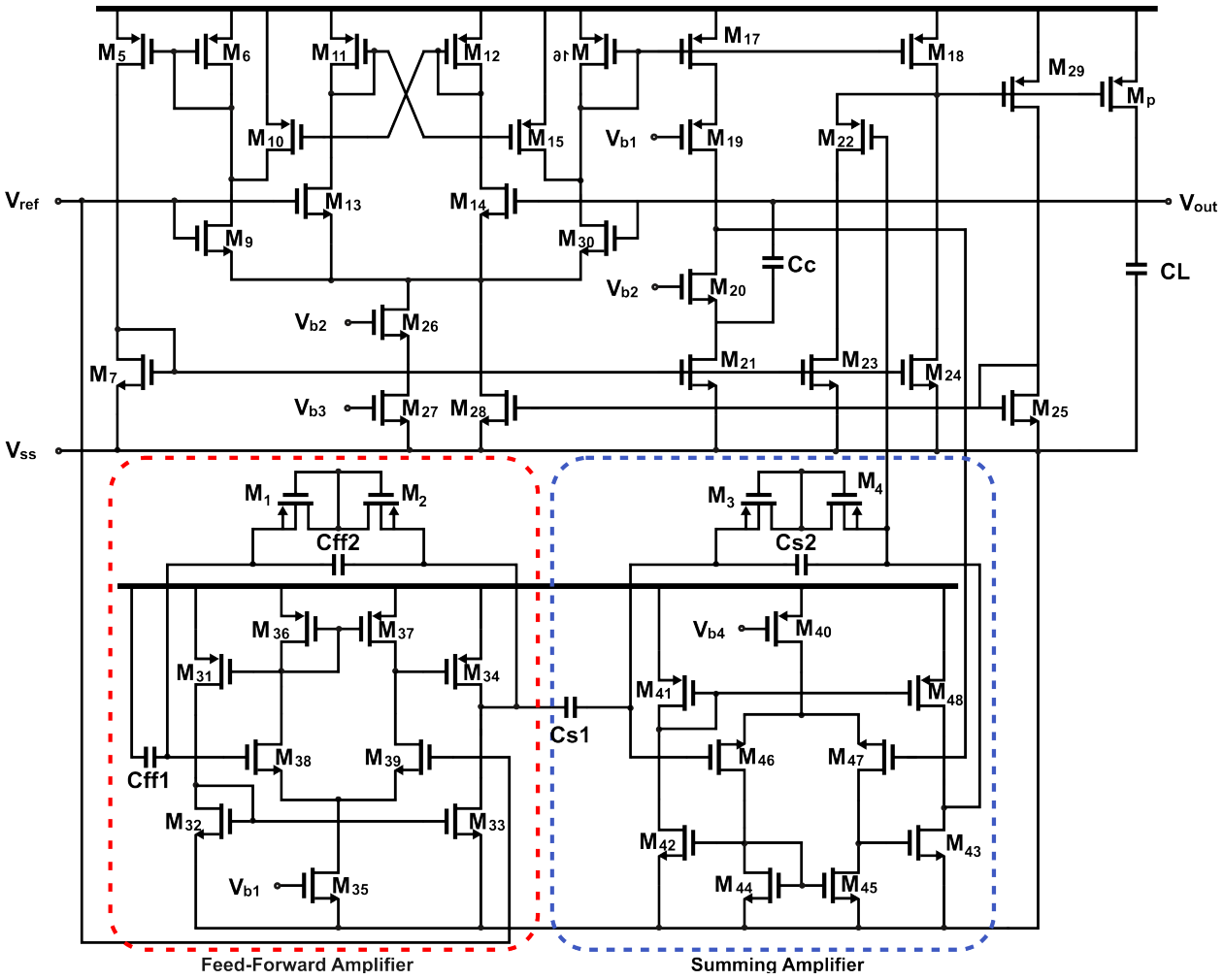


Figure 2.17: High PSRR LDO with a low I_Q presented by T. Guo *et. al.*

In 2022, Guo *et. al* [23] (Fig. 2.17) introduced a high PSRR LDO that achieves a remarkably low quiescent current of 900 nA by implementing a capacitive feed-forward ripple cancellation (CFFRC) technique. This approach leverages capacitors and back-to-back pseudo-resistors to effectively cancel power supply noise without the significant power consumption associated with traditional resistive techniques. The design maintains high performance with a PSRR enhancement of -22 dB at 1 MHz under a 200 mA load. By replacing resistive components with capacitive ones, the quiescent current is minimized while maintaining effective noise cancellation, making this design a significant advancement in

low-power, high-performance LDOs.

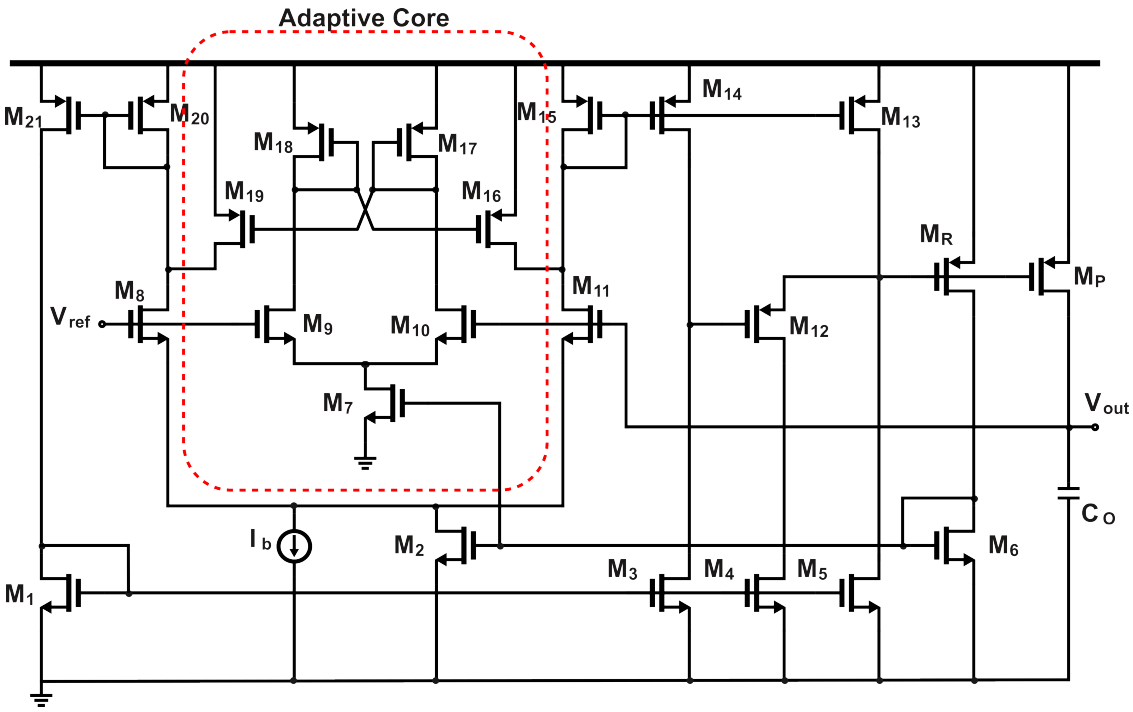


Figure 2.18: Low I_Q adaptable LDO design by J. S. Kim *et. al* representing the state of the art.

Shown in Fig. 2.18, Kim *et. al* [24] propose an adaptive biasing network to detect the amount of load current and disengage faster, more power consuming elements such as gate drivers to reduce current. This is a logical next step in LDO design as enable circuitry is not uncommon, however these enable inputs will require logic units to drive this with load detection being implemented in different circuitry. This design eliminates the need for external circuitry which greatly improves the FoM of the design. This technology can still be improved, as this design was built for smaller loads of 10 mA and lower. This lower I_{max} actually reduces the current efficiency which is 98%. Since the circuit does have a higher I_Q at full loads due to all of the circuits elements being "on" more current is drawn with limited output current.

2.6 Summary

This chapter aims to develop an understanding of where the choices for this proposed design have originated. Expressing many options that are available in the current LDO literature, and their trade-offs. The current space revolves around current efficient devices and hence a large body of work develops the methods necessary to produce an LDO with favourable qualities in this regard. Voltage regulation circuitry has developed extensively over the past decades with the state of the art LDOs of today being highly efficient devices which are capable or operating under a wide range of conditions. With the effective introduction of stabilizing circuitry such as a simple ESR based zero to the more complex pole-zero cancelations techniques used in literature, it is common to have devices reach high phase margins and remain stable from low to high load conditions. Selection of a specific pass element is dependent on the requirements of an LDO with the common PMOS element remaining a highly effective, fast and low quiescent current option, however power supply ripple remains a targeted area of improvement for these LDOs.

Chapter 3

LOW I_Q ZERO TRACKING LDO

This proposed work focuses on development of a low quiescent current wide load range LDO. The proposed topology is fully displayed in Fig. 3.1 with all transistor parameters tabulated in Table 3.1. With the modern requirements of LDOs aimed towards SoC battery powered devices, it has become increasingly important to develop technologies which maximize stability while minimizing current consumption. The examples specified in the literary review provide strong sources for the state of the art in which this research intends to build upon. This solution intends to contribute to the literature available by improving the commonly used Miller compensation technique. Introducing nested compensation loops allows for the required stability without consuming high amounts of current. This chapter intends to explain each of the stages of this improved, novel design. Once the circuit is understood, all simulations utilized to verify the design will be examined, finally measurements and conclusions will be produced.

3.1 Proposed Design

The contributions of this work are primarily focused on the design of stability circuitry that demands very little static and dynamic current consumption. As discussed in 2.3.2, it is critical for performance for a design to accommodate the additional pole and zero which is produced when utilizing an output capacitor and its ESR. Stability is dependent

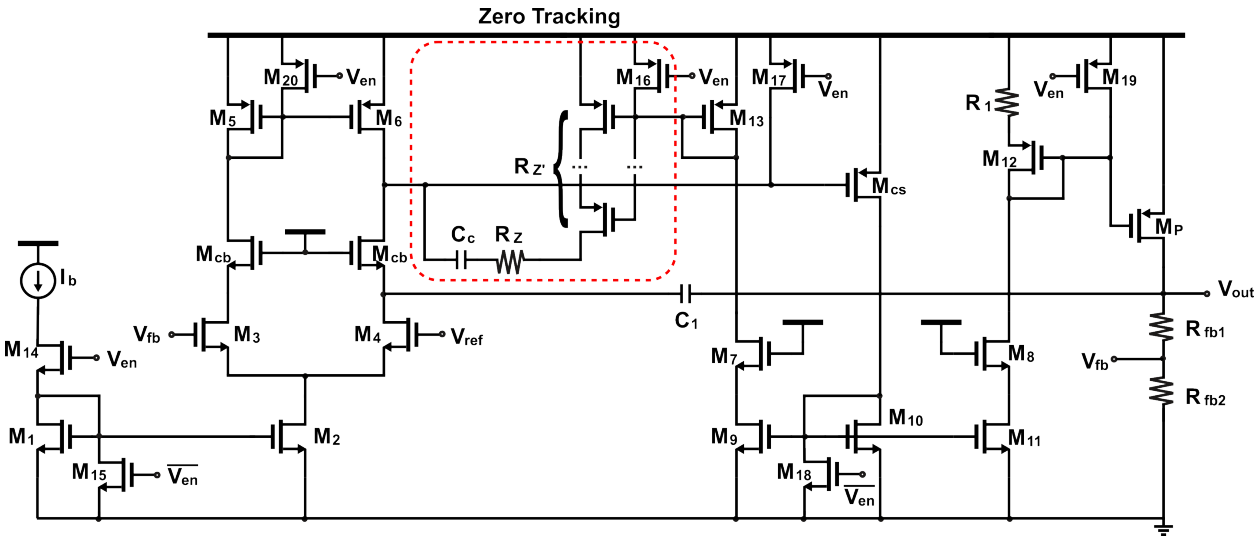


Figure 3.1: Proposed LDO design.

on load conditions, in (2.2) the dominant pole, associated with the output resistance of M_P and the output capacitor, dictates the bandwidth of an LDO. As output current increases the output resistance drops and therefore "pushes" the pole to higher frequencies. This relationship is pivotal in determination of the bandwidth of an LDO, and therefore is a key factor in the contribution this proposed design targets.

With the addition of an internal zero which is not associated with the ESR zero, further performance improvements can be included to an LDO, however without an ability to dynamically alter the position of this zero, the output pole remains a detriment to stability. To track this change in pole position, a dynamic zero is introduced which uses a MOSFET biased in the linear region to affect the impedance of a zero network. Current mirrors are used to sense the changes in I_{load} and send this value through a current attenuation network to bring down the quiescent consumption and keep the zero tracker from over reacting to output changes.

LDOs can be simply analyzed to have a DC output of,

$$V_{out} = V_{ref} \cdot \left(1 + \frac{R_{fb1}}{R_{fb2}}\right) \tag{3.1}$$

where $R_{fb1} = 2.4$ MΩ and $R_{fb2} = 4.8$ MΩ. This gives the desired β or feedback ratio of 0.5. The larger valued resistance is beneficial for low frequency PSRR, furthermore, as the current sensing network is also a source of static dissipation. To create resistors in CMOS, polysilicon is deposited above an isolating trench to cause a low parasitic impedance within the IC. These resistors are very common however increase in area as the resistance is increased. A balance must be made between the amount of static current that flows to the current sensing feedback network, and how much area is available within a design. With the values that were selected for this proposed design, the current through the current sensing network at typical running conditions of $V_{out} = 1.8$ V will have $I_{fb} = 250$ nA. Essentially, without any leakage current, with no load, the absolute minimum current that this device will consume, is 250 nA. This is where most designs in low I_Q systems must sacrifice area.

3.1.1 Error Amplifier

The error amplifier, shown in it's entirety in Fig. 3.2, is the point at which the difference between V_{ref} and V_{fb} is determined in the circuit, however the EA is also critical to the overall performance of the LDO, being a contributor to the PSRR, accuracy as well as regulation of line and load changes. Error amplifiers, to be optimally integrated into an LDO design, must have their internal poles at a much higher frequency than those contributed by the pass element. Without this, the poles would contribute a phase shift which lowers ϕ_M while also lowing UGF overall. Furthermore, an effective error amplifier must contribute little current consumption while being able to support the demands for current draw of the subsequent stages gate draw.

To combat this, a modified operational transconductance amplifier (OTA) design topology is employed, with an added cascode current buffer allowing for improved Miller

Table 3.1: Transistor Parameters

Parameter	**Device Values**					
Transistor	M_1	M_2	$M_{3,4}$	M_5	M_6	M_7
Element	NMOS	NMOS	NMOS	PMOS	PMOS	NMOS_{3V}
Length	8 μm	8 μm	2 μm	8 μm	8 μm	800 nm
Width	2 μm	2 μm	4 μm	2 μm	2 μm	2 μm
Fingers	1	1	2	1	1	1
Multiplier	2	4	2	2	2	2
Transistor	M_8	M_9	M_{10}	M_{11}	M_{12}	M_{13}
Element	NMOS_{3V}	NMOS	NMOS	NMOS	PMOS_{3V}	PMOS
Length	800 nm	10 μm	2 μm	2 μm	800 nm	2 μm
Width	2 μm	2 μm	2 μm	2 μm	2 μm	500 nm
Fingers	1	1	1	2	1	1
Multiplier	2	2	2	2	2	4
Transistor	$M_{14,15,18}$	$M_{16,17,19,20}$	M_{cb}	M_{cs}	M_P	R'_z
Element	NMOS	PMOS	NMOS_{3V}	PMOS	PMOS_{3V}	PMOS
Length	500 nm	500 nm	800 nm	800 nm	800 nm	2 μm
Width	2 μm	2 μm	2 μm	2 μm	50 μm	4 μm
Fingers	1	1	1	1	10	1
Multiplier	1	1	2	2	4	1

compensation, known as Ahuja compensation [91]. Due to the high output resistance, this device "pulls" the output pole associated with its output resistance and the input capacitance of the subsequent stage to lower frequencies. This introduces the need to move these high impedance poles away from each other, hence the introduction of multiple zeros. The benefit of such a design however, is that the gain of an OTA is high relative to its current consumption.

A primary trade-off when designing such a stable high efficiency device is the balance between the error amplifiers gain, and its current consumption. In large technology sizes such as the 180 nm process used here, gate-induced drain leakage, sub-threshold leakage and junction reverse-bias leakage are large contributors to the static consumption of a design. Included in static consumption is biasing current, being a large contributor to overall device consumption. Because the gain of an amplifier is largely related to how much power the

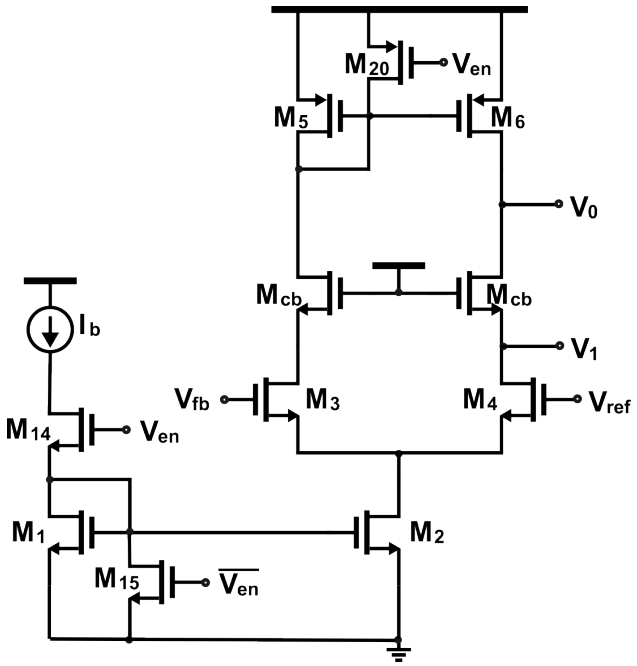


Figure 3.2: Error amplifier of the proposed design.

device consumes, a balance must be made to keep performance high and current low. When analyzing a simple operational transconductance amplifier the gain equation is equal to,

$$AV_{OTA} = gm_3(ro_6||ro_4) \tag{3.2}$$

where the transconductance (gm_3) is equal to,

$$gm = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D} \tag{3.3}$$

when examining this relationship, we can see that the length of a transistor has a detrimental effect on the transconductance. However, leakage current is lowered by an increase in L_{eff}. Therefore performance must be balanced in this case to keep consumption low while still allowing for accurate response and the ability to reject noise.

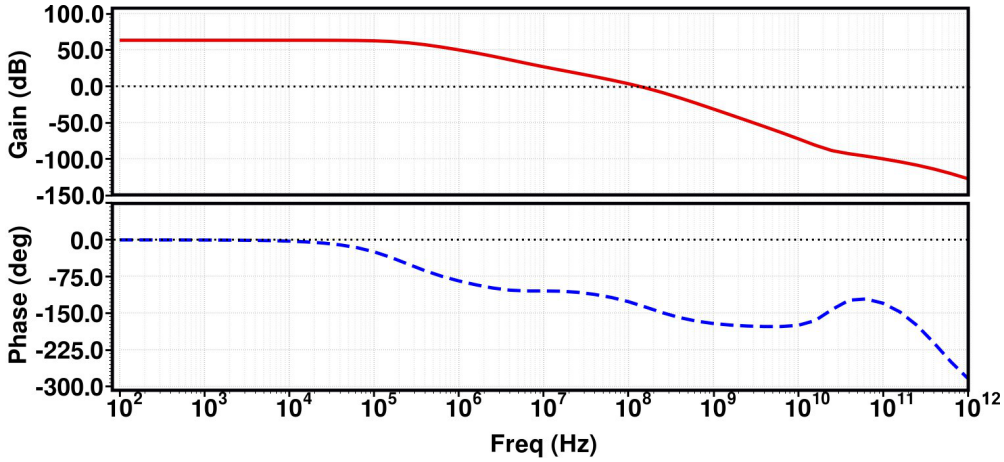


Figure 3.3: Gain and phase of the error amplifier for a typical speed at $T = 27°$.

The error amplifier performed with a DC gain of 62.5 dB, with a biasing current (I_b) of 100 nA making it highly efficient. When analyzing the design, the transfer function derived was found to be,

$$\frac{V_{out}}{V_{in}}(s) \approx \frac{-gm_6\left(gm_5 + C_{gd6}s\right)}{\left(R_{in3}C_{g3}s + 1\right)\left(\frac{C_{gs6}s}{gm_5} + 1\right)} \tag{3.4}$$

showing that it is considered approximate to a two pole single zero system which is demonstrated in Fig. 3.3 below the UGF or roughly 100 MHz. With this high UGF we have a sufficiently large bandwidth for satisfactory slew rates and settling time.

3.1.2 Ahuja Compensation and Output Stage

The output, in Fig. 3.4 is comprised a three elements, the driving stage, the pass element, and an Ahuja compensation capacitor. The current driving stage is a PMOS, common source gain stage which acts as a second stage amplifier feeding into a current network. The network utilizes ratioed current mirrors acting as current amplifiers to allow for proportional control of the current driven devices, the pass element, who's parameters are in table 3.2, and the zero tracking unit. This essentially allows for a known ratio of output current to

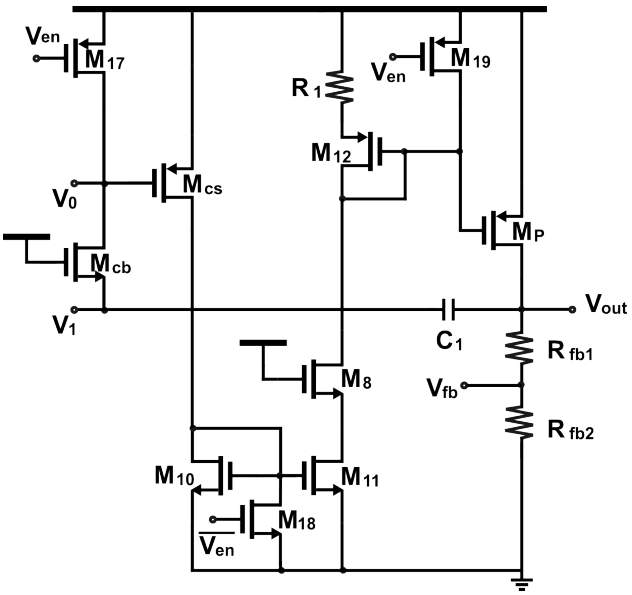


Figure 3.4: Current amplification network and pass transistor.

control the zero tracking network based upon the demand experienced at the load. The network also must be capable of meeting the current demands of the gate capacitance of the pass element. Without sufficient current amplification, there is the potential for reduced stability and slew rate at the output.

To properly size the output pass element it is important to consider the effect that sizing has on the transistor performance. Larger transistors have better performance in terms of their channel length modulation coefficient, however suffer from larger gate capacitance, requiring stronger driving circuitry. Furthermore, if the channel length is sized too small, leakage will be increased, drive will be insufficient and impedance will be too low at high loads to keep the pole positions manageable for high stability, however too large a channel length rapidly decreases the speed of the output. The impedance of a transistor is related to the current flowing through the device I_{DS}. As the position of the output pole is related to the pass devices impedance we can express the dominant pole as follows,

$$\omega_{p1} \approx \frac{1}{C_O(r_{op}||R_L||(R_{fb1}+R_{fb2}))} \approx \frac{\lambda \cdot I_{load}}{C_O} \tag{3.5}$$

Table 3.2: Pass Element Parameters

Parameter	Device Value
Element	PMOS
Length	800 nm
Width	50 μm
Fingers	10
Multiplier	4

where λ is the channel length modulation coefficient of the pass element. As this pole dominantly affects the UGF and ϕ_M it is critical to stability, hence solutions must be made to offset these effects. The decision to increase speed of the output element was critical so the PMOS was decided to have the following characteristics.

The capacitor C_1 is used for two functions. One function of this capacitor is to reduce the peak voltage on startup by acting as a "soft-startup" capacitor. To show this functionality, the startup sequence of the proposed LDO has been analyzed and displayed in Fig. 3.5 where an implementation with and without C_1 is enabled. The transient is viewed to have a reduced voltage peak with a faster return to nominal output voltage. When the LDO is first turned on the output voltage will be 0 V, therefore the feedback voltage will be much smaller than that of V_{ref}. When the voltage difference is sensed by the differential gain stage, M_{cs} will enter saturation, M_{10} (diode connected load) will mirror this current to the output pass transistor M_P while also amplifying the signal by k_x. M_P will also enter saturation. This sudden rush of current could damage the pass transistor unless V_{out} is damped by a capacitor C_1.

Another function of this capacitor is to act as an Ahuja [91] compensation capacitor. The capacitor is connected in negative feedback from the output of the pass transistor to the output of the differential amplifier. A current buffer, added to the differential amplifier by cascode M_{cb}, is included in the loop to eliminate the feed forward path and increase the output resistance. This feedback loop alters the pole associated with the output resistance of the pass element, going from dominant (lowest frequency pole) to non-dominant, pushing

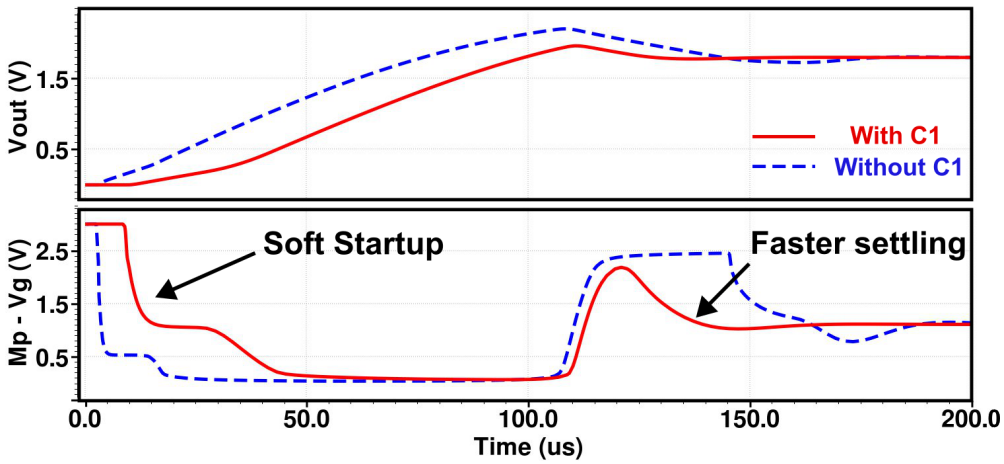


Figure 3.5: Proposed LDO startup, with C1, shown in red and without, shown in blue.

the now non-dominant pole further away from the UGF while shifting a zero and producing a new pole at lower frequencies. By doing so this pulls the phase up at the UGF which increases ϕ_M.

When designing a compensation network, the exact parameters of each component can have large effects on the performance of a device, not simply the topology alone. A method utilized to select the size of these components is to perform parametric sweeps. Figure. 3.6 shows such an analysis being performed, with the swept parameter being the length and width of each capacitive cell. When developing capacitors in CMOS, cells are made from metal layers separated by insulation. These metal insulator metal (MIM) capacitors are required to be square devices when fabricated therefore the parameter that is adjusted is the size in μm. C_1 was selected to be $40\mu m$ x $40\mu m$ to minimize area used while having good ϕ_M at both high and low I_{load}.

3.1.3 Zero Tracking Network

The zero-tracking network, comprised in Fig. 3.7, operates as a filter connected to the output of the error amplifier. By adding this compensation filter, a zero is introduced,

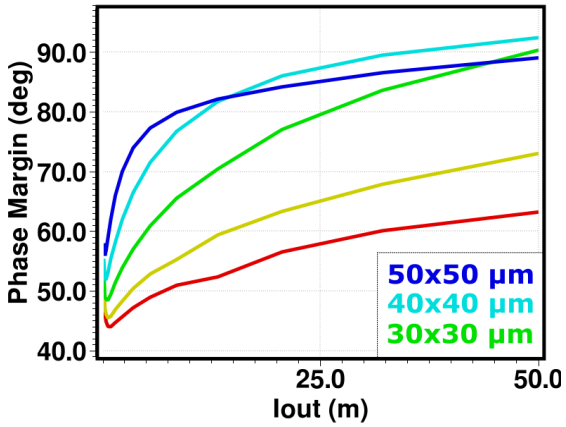


Figure 3.6: Sweeping the Ahuja compensation capacitor C_1.

whose resonant frequency position is controlled by the output current I_{load}. The variable left half plane zero is stated as being,

$$\omega_{z1} = \frac{1}{(R_Z + R_{Z'}) \cdot C_C}. \tag{3.6}$$

This compensation network is made of essentially three components, C_C, R_Z and a transistor network which varies in resistance based on output current,

$$R_{Z'} = \frac{1}{\lambda \cdot I_P k_y \cdot k_z}. \tag{3.7}$$

where λ is the channel length modulation coefficient and k_z is the ratio between $R_{z'}$ and M_{13} which can be written as,

$$k_z = \left[\frac{(W/L)_{R_{Z'}}}{(W/L)_{M_{13}}} \right]. \tag{3.8}$$

The time coefficient, τ, of the filter determines the position of the low frequency zero which increases ϕ_M by reducing the loop gain slope near UGF by $+20\ dB$ and introducing a phase shift. It is important that this network be tracked to the output current since the out-

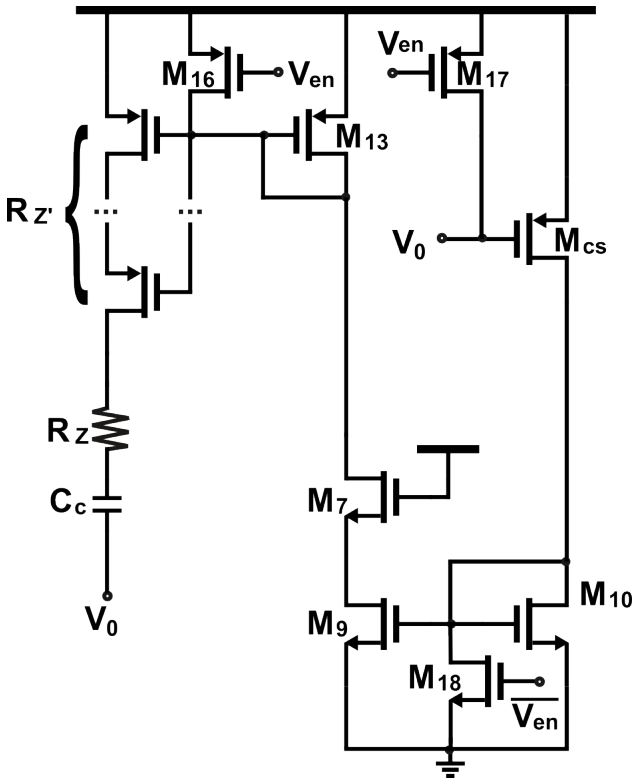


Figure 3.7: Zero-tracking compensation network proposed.

put pole is proportional to I_{load}. By adjusting the frequency by which a short to ground will be created we can track our compensation network to $p1$. $R_{z'}$ was calculated to span 654.48 $k\Omega$ at $I_{load} = 50\ mA$ to 4.68 $M\Omega$ at $I_{load} = 500\ \mu A$ which means that as current at the load increases, the zero will adjust to match the output poles location in frequency. Figure 3.8 demonstrates that the zero from (3.6) tracks the changes of the output pole, improving phase margin sufficiently to stabilize the loop. The benefit of this approach is that it does not significantly degrade power consumption performance.

To express how much these low current consuming compensation techniques implemented improve the ϕ_M of the proposed LDO, Fig. 3.9 compares an equivalent ESR compensated LDO, one with the Ahuja capacitor added, and the proposed LDO itself. It's clear how much of an improvement the zero tracking and Ahuja compensation add with the ϕ_M increasing by roughly 1350%, as compared to a conventional design. This could also be

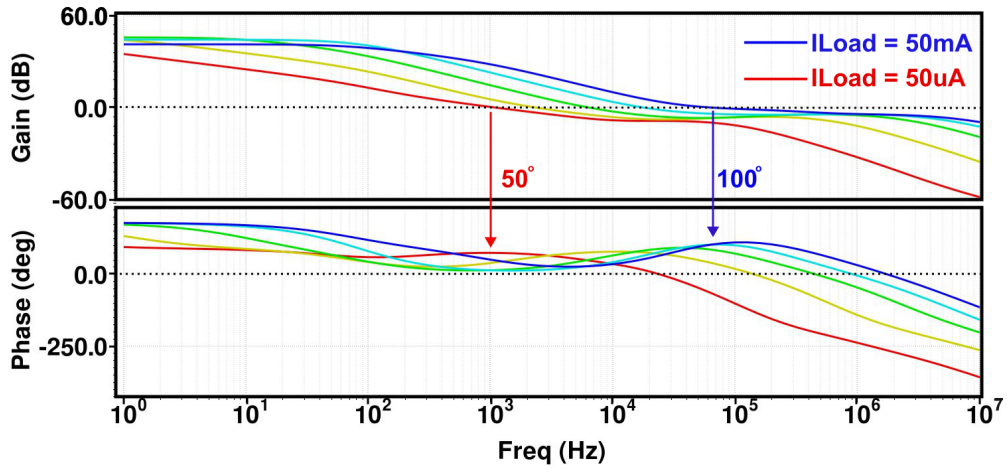


Figure 3.8: Simulated gain and phase response to 10 MHz frequency sweep with I_{load} varied from 50 μA to 50 mA.

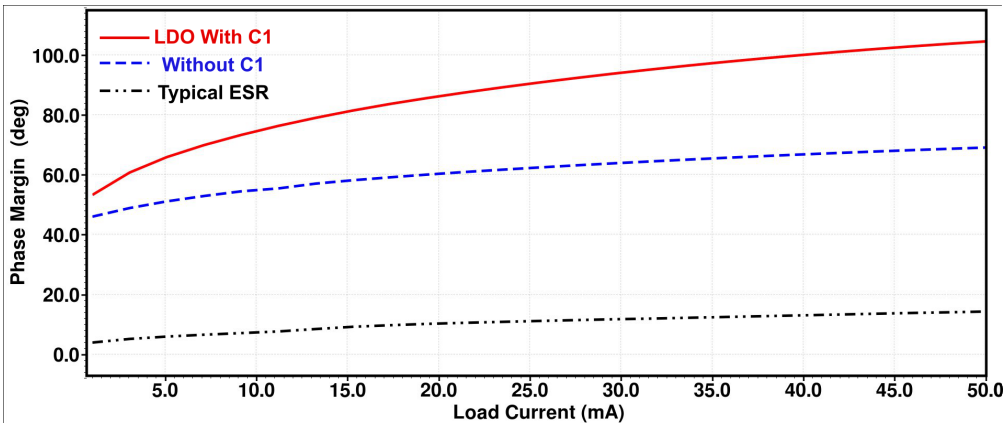


Figure 3.9: Simulated phase margin of the proposed LDO, without Miller compensation (no C1) and an equivalent conventional ESR compensation LDO (no improvements).

improved further by altering the feedback current sent to R'_Z, displayed in Fig. 3.10. If the ratio between M_9, M_{10} and M_{11} is altered to $W_{M_{10}} = 1\ \mu m$ there is a noticeable boost in ϕ_M caused by a more accurate linear relationship between I_{load} and ω_{z1}.

3.1.4 Small Signal Analysis

The proposed design focuses on enhancing stability through increased phase margin (ϕ_M) while minimizing static and dynamic current consumption. As discussed in section 2.4, stabilizing a three-pole LDO presents greater challenges than a simpler two-pole LDO

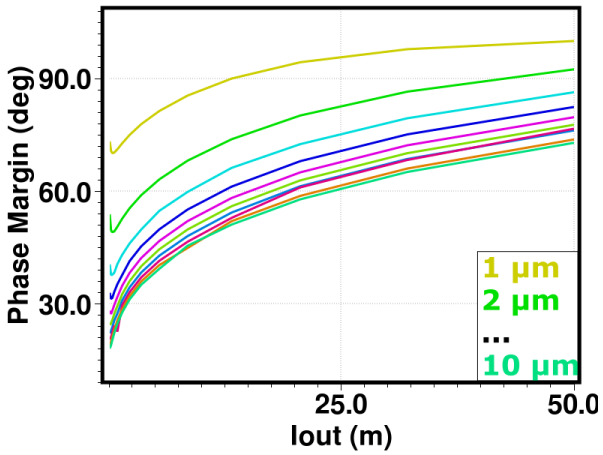


Figure 3.10: Sweeping M_{10} width.

with equivalent series resistance (ESR). Effective compensation requires removing the effect of the output pole, which is commonly achieved through pole-splitting. However, traditional Miller compensation is less effective. Miller compensation involves adding a compensation capacitor C_1 between the output of a gain stage and its input, creating a dominant pole to stabilize the system. This technique, while effective in some LDO designs, is dependent of the load capacitor used, as a larger load capacitor will require a large Miller capacitor which is undesirable. The large Miller capacitor introduces a dominant low frequency pole which results in a phase lag that reduces phase margin and can destabilize the loop. Additionally, the additional capacitor allows for a feedforward path, providing an additional zero to the LDOs transfer function, further increasing the difficulty of stabilizing this system.

To address these issues a technique, similar to that in [91], is used. Where a current buffer M_{cb} is integrated into the error amplifier, utilizing the preexisting I_b current to further minimize power consumption. This buffer increases isolation between the Miller capacitor and the output of the error amplifier, effectively eliminating the feed-forward path and mitigating the adverse effects of the RHP zero. The introduction of the current buffer helps to better manage the frequency response and stability of the LDO. The linearized small signal model, depicted in Figure 3.11, provides a visual representation of these dynamics,

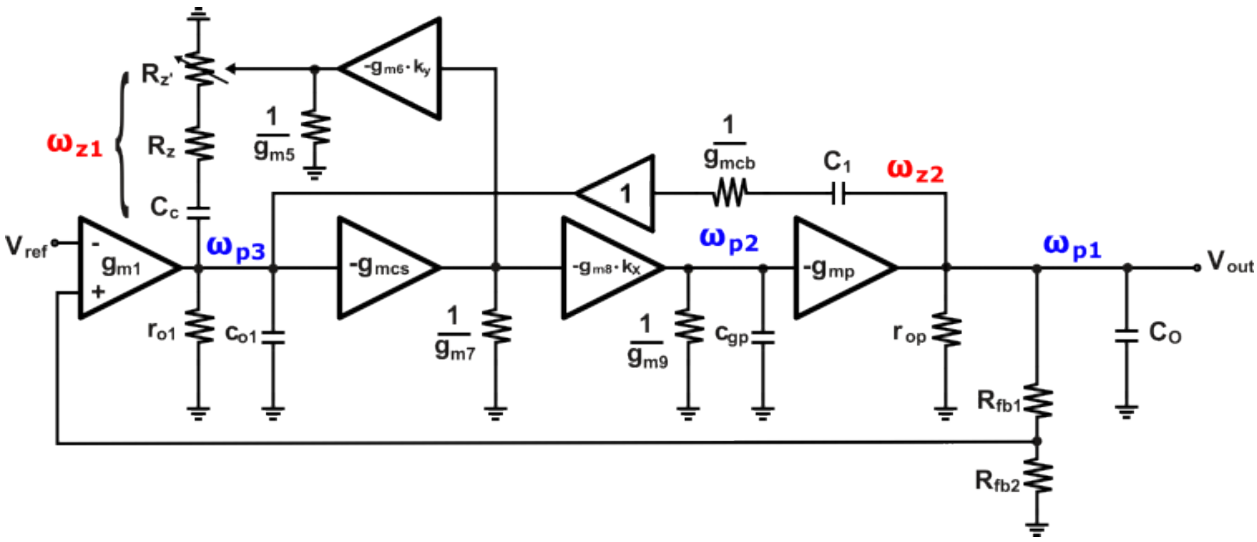


Figure 3.11: Proposed LDO small signal model.

showing the positions of the poles and zeros and their impact on stability. The small signal analysis involves the following pole and zero frequencies:

$$\omega_{p1} \approx \frac{1}{C_O r_{op}} \tag{3.9}$$

$$\omega_{p2} \approx \frac{g_{m9}}{c_{gp}} \tag{3.10}$$

$$\omega_{p3} \approx \frac{1}{r_{o1} c_{o1}} \tag{3.11}$$

$$\omega_{z1} \approx \frac{1}{C_c(R_z + R_{z'})} \tag{3.12}$$

$$\omega_{z2} \approx \frac{g_{mcb}}{C_1} \tag{3.13}$$

Figure. 3.11 illustrates these elements and helps in understanding their influence on the circuit's stability and performance. By optimizing these parameters and incorporating revised compensation techniques, the LDO design achieves a balanced trade-off between stability, performance, and efficiency.

3.1.5 Layout

The layout for the proposed LDO, given in Fig. 3.12, is designed through use of the Cadence Virtuoso development suite. Using the integrated TSMC 180nm production development kit (PDK) a functional CMOS integration of the designed schematic is achieved. When developing a layout, the key considerations are that of functionality first. TSMC provides all needed aspects of their technology. This information is however proprietary, therefore elements of this technology cannot be made public, however, sizing, trace widths, current limitations, ect. are all provided when designing for their foundry.

In designing the layout, several key techniques are employed to ensure the robustness and reliability of the integrated circuit. One of the critical steps was the inclusion of dummy transistors at the edges of active transistor arrays. These dummy transistors are essential for mitigating process variations, particularly during photolithography and chemical-mechanical polishing (CMP). By placing them at the periphery, it ensured that the active transistors within the array were processed under uniform conditions, reducing edge effects and improving overall transistor matching. This approach is important in analog circuits, where precise matching is crucial for maintaining accuracy in differential pairs and current mirrors. Additionally, the dummy transistors helped manage parasitic capacitances and mechanical stress, contributing to more consistent electrical characteristics across the chip.

To further enhance the reliability of the layout, antenna effect diodes and electrostatic discharge (ESD) protection circuitry are incorporated . Antenna effect diodes were added to prevent the accumulation of charge on long metal interconnects during the fabrication process, which could otherwise lead to gate oxide damage due to the antenna effect. These diodes provide a discharge path for the excess charge, protecting the transistors from potential failures. ESD protection circuitry was also integrated at the input and output pads to safeguard the IC against electrostatic discharge events, which are common during handling and operation. This circuitry helps dissipate the high voltage spikes that can occur during an ESD event, preventing catastrophic damage to the chip. Together with careful transis-

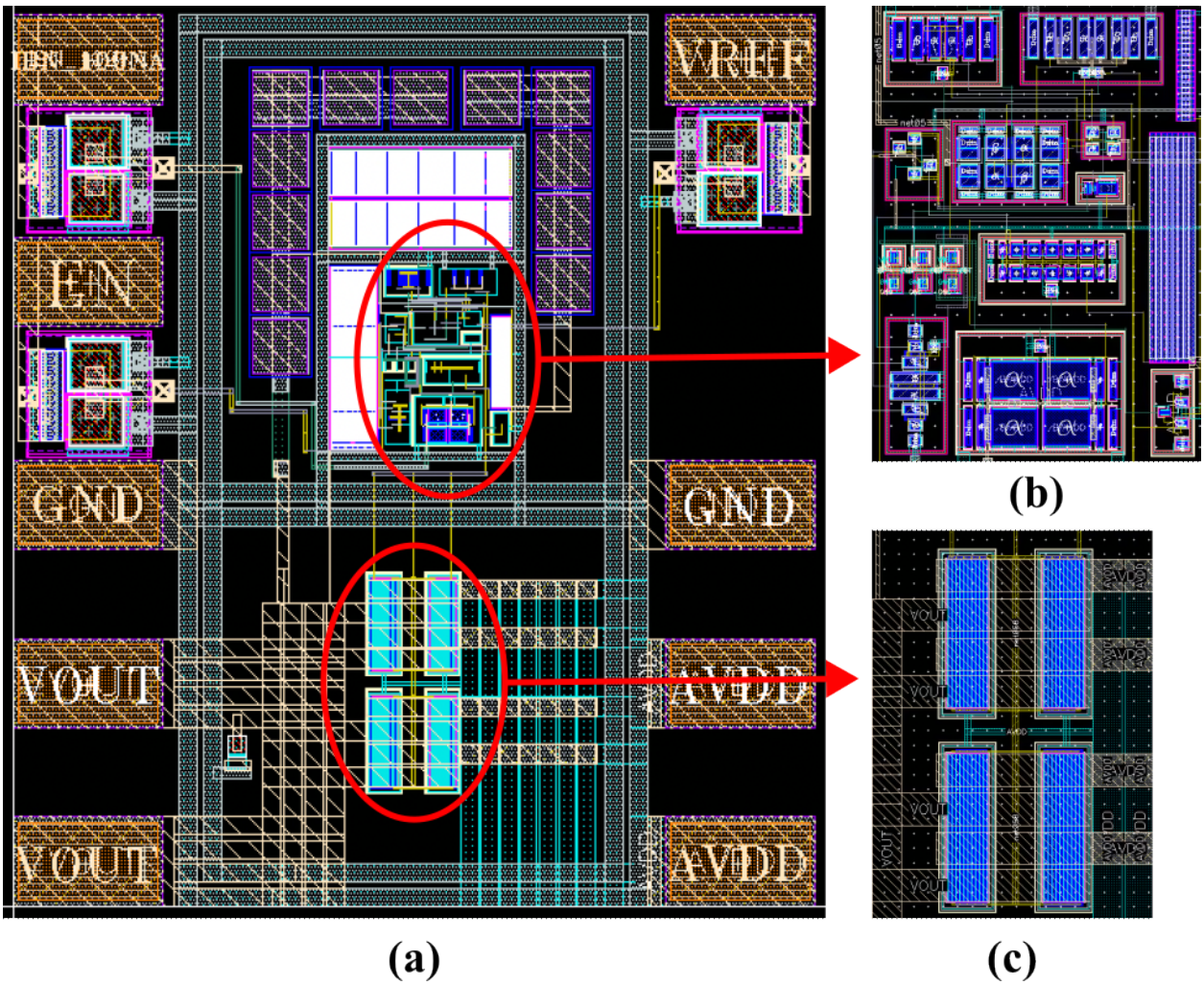


Figure 3.12: (a) Layout of the proposed LDO design, with (b) enlarged control circuitry and (c) pass element.

tor matching and layout optimization, these techniques ensure that the CMOS design not only meets stringent performance specifications but also achieves high yield and reliability in production.

3.2 Simulations

To understand the operation of the circuit, testing began with a focus on stability with alterations of zero-tracking network as well as improvements to the pass element. At

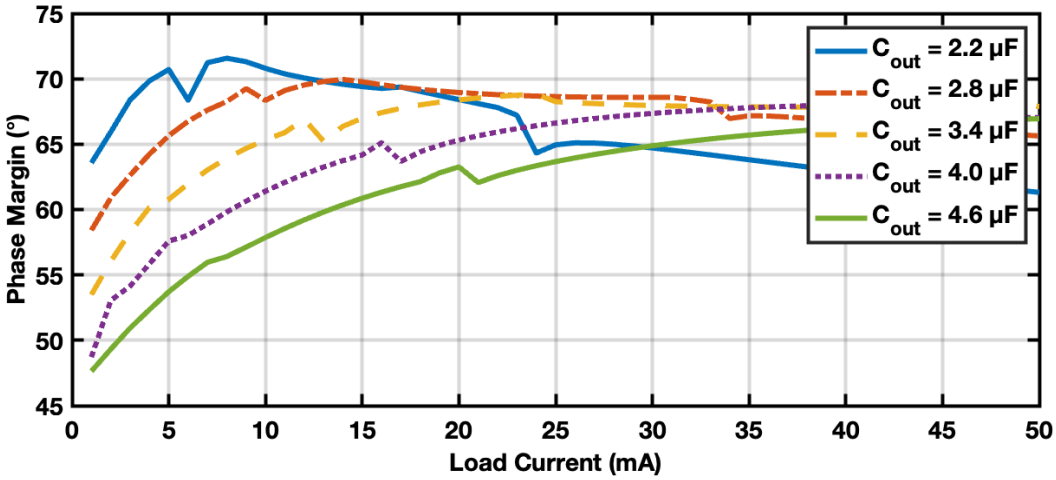


Figure 3.13: Simulated sweep of I_{load} with multiple different C_O values.

this point, schematic testing is conducted, where no layout is produced, therefore layout inaccuracies cannot be accounted for. This is a critical point in testing where any changes to the circuit are made, along with opening of the feed-back loop. Once a layout is created, no wires, inputs or outputs can be altered, therefore phase and gain testing is conducted in this first stage.

3.2.1 Phase Margine

Critically, it is common for LDO design to have poor phase margin at low loads. Utilizing a well tuned zero tracking network, $\phi_M = 50°$ when an I_{load} of less than 1 μA is present. With a full load condition of 50 mA is present, $\phi_M = 100°$ which is quite high. This simulation has been presented in Fig. 3.8 however is drastically altered by the selected C_O, therefore Fig. 3.13 displays the full spectrum of output current with varied output capacitor values. With $C_O = 2.2\ \mu F$ giving the best low current phase margin while not diminishing high load performance substantially.

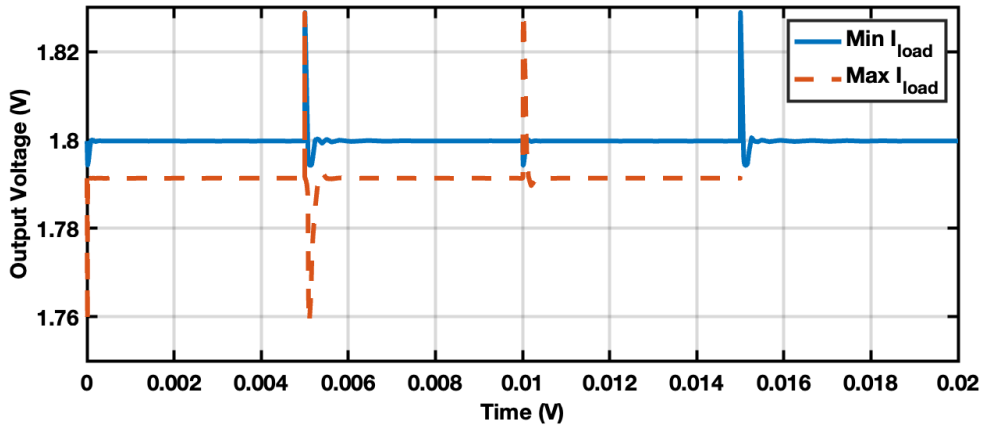


Figure 3.14: Post layout simulation of a 100 mV swing on the input, demonstrating line regulation.

3.2.2 Line Regulation

When the input voltage fluctuates within a range of $\pm 50\ mV$, the output voltage deviation was simulated to be less than 600 $\frac{mV}{V}$ at high loads in the worst case, which is shown in Fig. 3.14. This performance is particularly robust under light load conditions, where conventional designs often struggle. The effectiveness of the line regulation across different load currents and input voltage variations is illustrated in Fig. 3.14. Notably, with an output capacitor of $C_O = 2.2\ \mu F$, the LDO demonstrated the most stable performance across the tested conditions, ensuring minimal output voltage ripple and superior regulation over the entire operating range.

3.2.3 PSRR

Furthermore, testing of the LDOs noise reduction is conducted as PSRR of an LDO is a critical figure. Shown in Fig. 3.15 the LDO is found to have a PSRR of $-38dB$ 1 kHz for the full load range and is between $-40\ dB$ 1 MHz and $-70\ dB$ as load decreases, with an output capacitance of 2.2 μF.

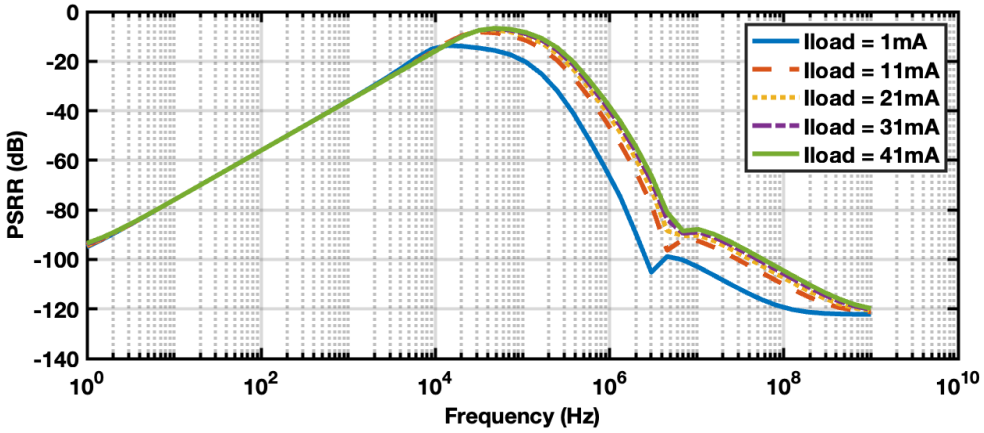


Figure 3.15: The post layout simulated PSRR of the full LDO.

Table 3.3: Simulated Corners

Corner	Process	Temperature (°C)	I_{bias}	ESR ($m\Omega$)
Best	FF	-40	+20 %	0.1
Typical	TT	27	100 nA	10
Worst	SS	150	-20 %	1000

3.2.4 Corner Simulations

The simulation results identify the operable corners of the proposed LDO. Identifying worst and best cases of how the system will react to fabrication with slow PMOS and slow NMOS or conversely, fast PMOS and fast NMOS for each transistor. Using Cadence ® Virtuoso, an analogues test bench was created to simulate real world testing. Simulations are conducted with an extracted render of the layout which bakes into the simulation all parasitics and non-linearities which are produced with the TSMC 180 nm layout shown in Fig. 3.12.

Each simulation is performed with the fully extracted layout incorporating all possible resistance and capacitive parasitics. The transient analysis is performed with a fast edge time of 100 ns with the worst case of a full load transient performance with an I_{max} 50 mA and I_{min} of 1 μ A whose transient is demonstrated in Fig. 3.16. The output capacitor is set

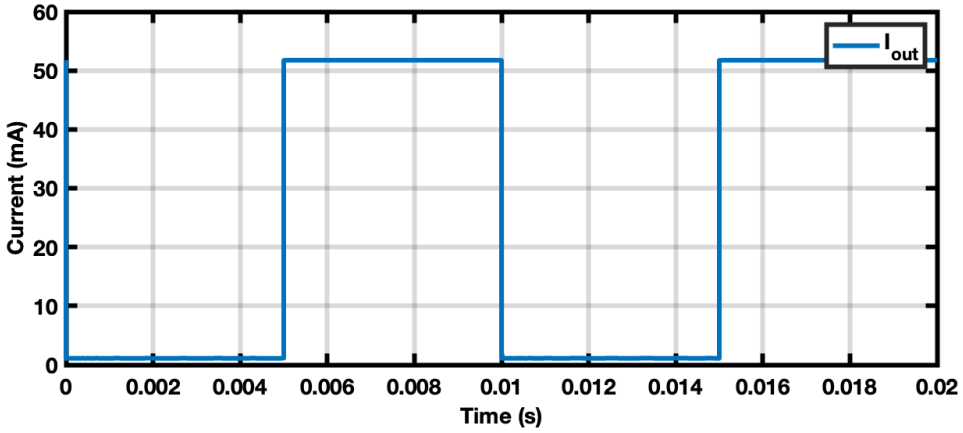


Figure 3.16: Demonstration of the change in I_{load} for each corner simulation.

to 2.2 μ F with an ESR of 100 $\mu\Omega$.

Figure 3.17 compares the LDO performance across different process corners. The slow-slow (SS) corner exhibits the largest voltage deviations, with a peak-to-peak fluctuation of about 60 mV, likely due to slower transistor switching speeds and reduced gain. In contrast, the fast-fast (FF) corner shows the least deviation, under 20 mV, due to faster transistor operation. The typical-typical (TT) and other mixed corners (SF, FS) demonstrate moderate stability, reflecting the balanced performance. These results underscore the importance of process variation analysis in ensuring robust LDO performance across manufacturing conditions.

Temperature performance, shown in Fig. 3.18, displays only minimal deviation from normal operation in the corner conditions. At T = -40° operation is the most stable with a reduction in output oscillations and a very fast response time. Overshoot and undershoot are improved with a deviation of about 10 mV. As temperature increases, CMOS performance is lowered, with threshold voltage and carrier mobility decreasing, leading to reduced switching speed and increased leakage currents. As a result, higher temperatures cause slower circuit operation, higher static power consumption, and decreased noise margins, while also accelerating degradation mechanisms like negative bias temperature instability (NBTI) and hot

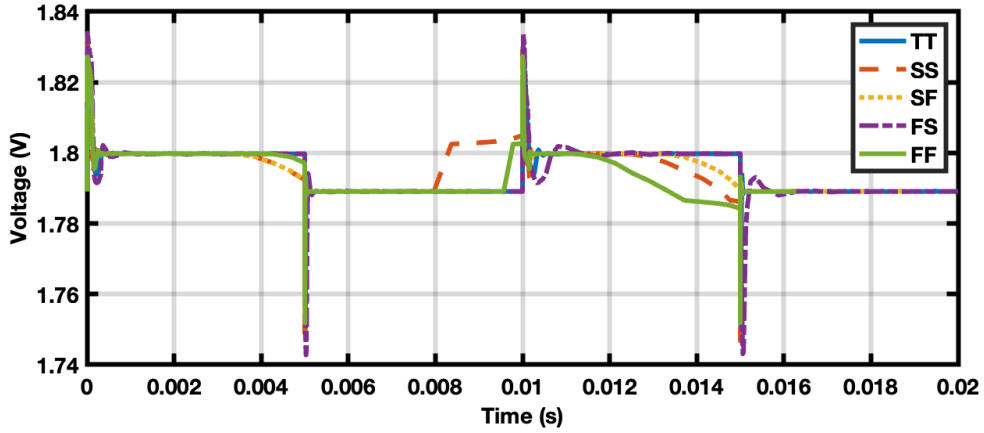


Figure 3.17: Corners simulations of typical, fast and slow PMOS and NMOS devices.

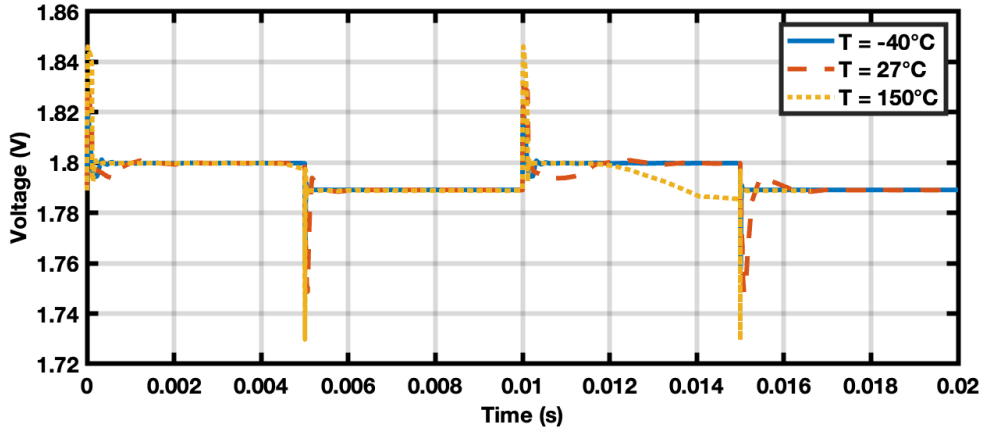


Figure 3.18: Corners simulations of differing operating temperature conditions.

carrier injection (HCI), which can impact long-term reliability. Although the corner simulation shows only a small change in transient performance, long term operation in this state could be damaging.

Studying the effects of bias current variation, Fig. 3.19 shows the effect of varying the bias current (I_{bias}) on the output voltage. At a reduced I_{bias} of 80 nA, the output voltage drops by approximately 20 mV during transient events, indicating insufficient drive strength for the pass transistor. At the nominal I_{bias} of 100 nA, the regulator maintains stability

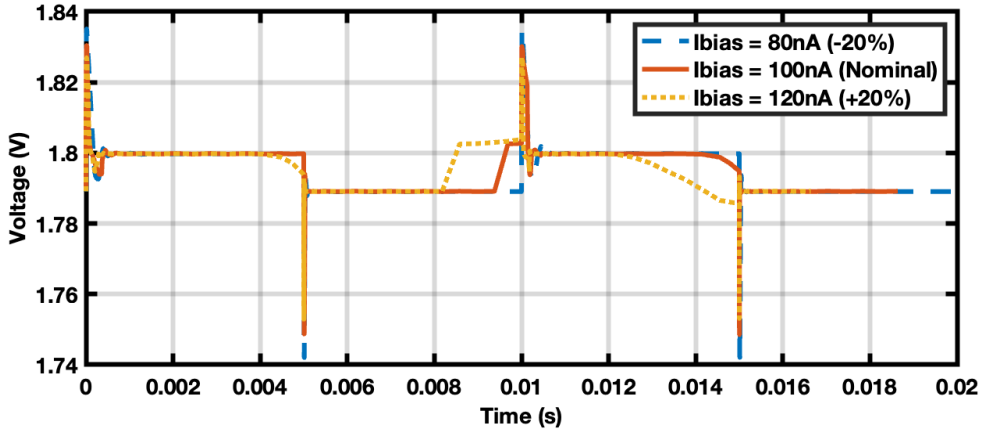


Figure 3.19: Corners simulations of varied I_{bias}.

with minor fluctuations, while increasing I_{bias} to 120 nA improves the response time but also increases power consumption. This analysis highlights the trade-off between power efficiency and transient performance, emphasizing the need for optimal biasing in LDO design.

Finally, the simulation in Fig. 3.20 demonstrates the impact of varying ESR on output voltage stability. With an ESR of 100 $\mu\Omega$, the output voltage exhibits minimal transient fluctuations, maintaining stability with a peak deviation of 10 mV during load transitions. Conversely, a higher ESR of 1 Ω induces significant voltage undershoot and overshoot, with deviations reaching up to 50 mV, likely due to increased phase lag in the feedback loop. The intermediate case with 10 mΩ shows a balanced response, suggesting that ESR must be carefully controlled to optimize both transient response and stability in LDO design.

3.3 Measurements

The LDO was fabricated using the TSMC 180 nm process, whose micrograph is shown in Fig. 3.21, and was tested by use of an external test board. The board consists of three voltage sources for V_{dd}, V_{ref} and an enable voltage. A transistor-driven load section that can switch between I_{max} and I_{min}. A separate voltage summing board was connected to

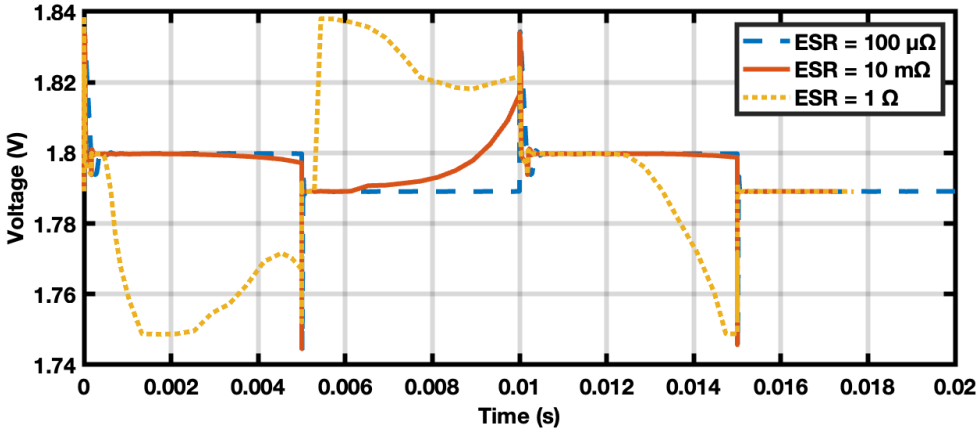


Figure 3.20: Corners simulations of varied ESR values.

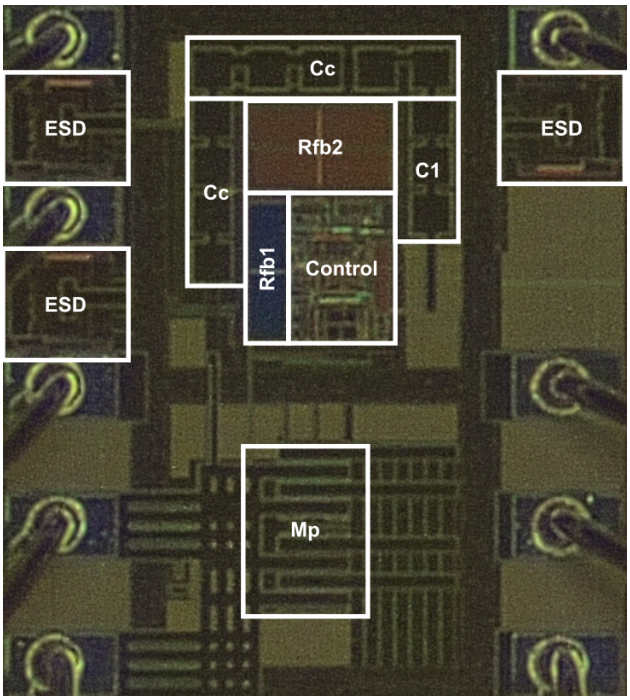


Figure 3.21: Micrograph of die used in measurement testing.

test the power supply rejection ratio (PSRR) via a Keysight MSOX4054A oscilloscope. All waveforms were captured on the MSOX4054A. A Keithley 2602A power source meter was utilized to measure I_Q and inject a biasing current for high-precision biasing.

3.3.1 Quiescent Current

To measure quiescent current a simple breakout board was designed and fabricated. The purposed of the board is to allow for external measurement devices to easily connect with the DUT. In this instance, since quiescent current is so low for the proposed design, the least amount of interconnect resistance should be had, furthermore, the testing device must be extremely well calibrated and capable of low current testing. Therefore the Keithley 2602A source meter was used, being capable of single nA resolution. By having the source meter provide the necessary V_{DD} and V_{en} for chip operation, it simultaneously measures the input current that is experienced during operation. A resistor is used to provide the biasing and the output voltage of the LDO is tested to verify the nominal 1.8 V operation is occurring. Once these conditions were met, differing load resistors were used to simulate DC operation with low to high load conditions. The current was measured over the entire system, and that which is flowing solely through the output resistor. These two figures are then subtracted to find I_Q.

The quiescent current curve presented in Fig. 3.22 offers a detailed characterization of the LDO regulator's performance across a range of load currents, highlighting both its strengths and potential areas for optimization. Notably, the curve demonstrates an initial peak in quiescent current at low load currents, followed by a stabilization and gradual increase as the load current rises. This behaviour aligns well with theoretical expectations and compares favourably with similar figures reported in the literature, where such peaks are often less pronounced or more erratic. With the minimum load, $I_Q = 486.67\ nA$ demonstrating high efficiency. Furthermore, the peak performance of the device is shown to be a 99.96% current efficiency. With the addition of enable circuitry the current in its disabled state, is 2.06nA.

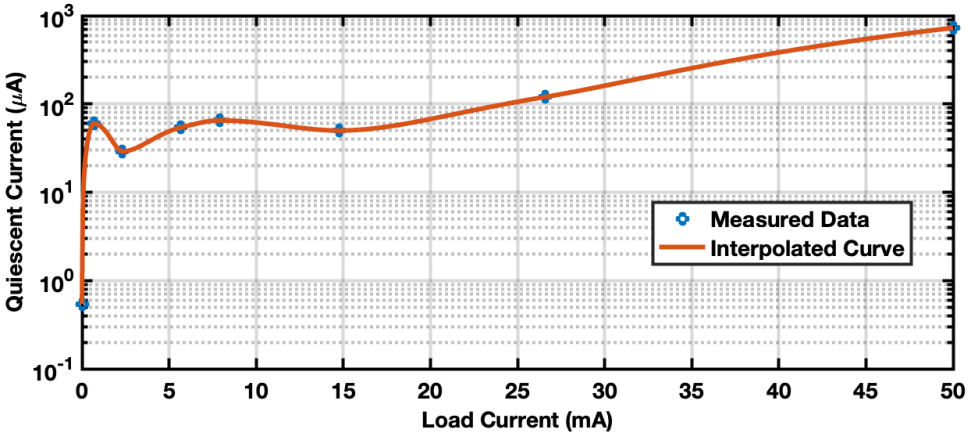


Figure 3.22: Measured no-load and full-load (adjusted) quiescent current.

3.3.2 Voltage Dropout

Voltage dropout was measured utilizing the same breakout board as that used in the quiescent current testing. With a variable DC power supply giving the V_{in} and V_{ref}, V_{in} is swept. An initial test is done with no load resistor applied, and measurements of the output voltage are taken at small input voltage steps. Once this is captured, a load resistor is added to the output to simulate full load operation at 50 mA. The same sweep is conducted and measurements are taken at varying input voltages.

The chip's performance under varying load conditions is demonstrated in the input vs. output voltage characteristics, as shown in Fig. 3.23. The LDO begins regulating in a no load condition with minimal dropout, being less than 100 mV. Under maximum load, the output voltage begins to rise sharply at 1.5V input, stabilizing near 2.5V, illustrating the dropout of 700 mV. This behaviour is typical in CMOS LDOs, indicating efficient regulation under heavy load but highlighting the trade-off in dropout performance.

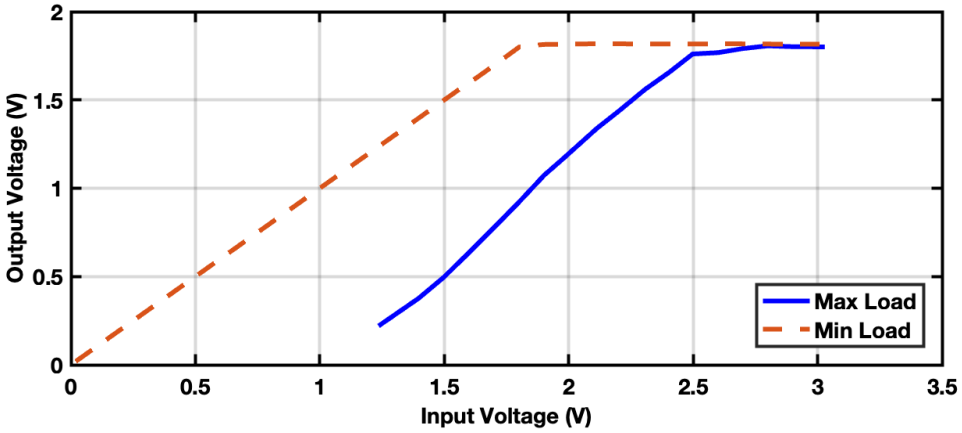


Figure 3.23: Measured $V_{dropout}$ at no load and full load.

3.3.3 Transient Performance

To measure the proposed LDOs operation during transient load events, a sophisticated test board was designed and fabricated. The board is capable of full voltage regulation with each input, V_{DD}, V_{ref}, and V_{en} each having their own ability to be varied for testing of droop situations or operation at different reference voltages. The biasing current is supplied by the Keithly source meter which is capable of precise current regulation. A transient load setup is made up of two current lines, one of which with large resistance capabilities going from 1.8 $k\Omega \rightarrow \infty\ \Omega$. The high load section is design to toggle with a high speed transistor. This transistor is biased to act as a switch and will allow current to flow in either both paths, simulating large load current, or that of just the low load path. This network ranges from 18 $\Omega \rightarrow 190\ \Omega$. Furthermore an array of capacitors are available to test the operation under different C_O and ESR values. Once connected, a function generator is used to produce the signal which toggles the NMOS switch, delivering a load transient to the output of the chip.

The load transient response of the chip, illustrated in Fig. 3.24 & Fig. 3.25, shows distinct performance characteristics. When the load drops from 50mA to 0mA, the LDO exhibits a settling time of 418 μs with an overshoot of 52.5mV. Conversely, when the load increases from 0mA to 50mA, the response is much faster with a 36.5 μs settling time but

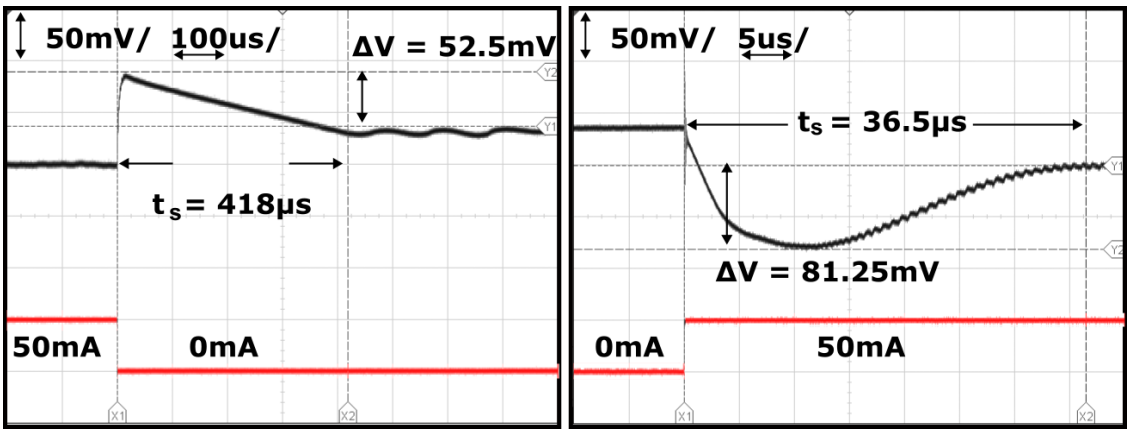


Figure 3.24: Settling of the proposed LDO at full-load.

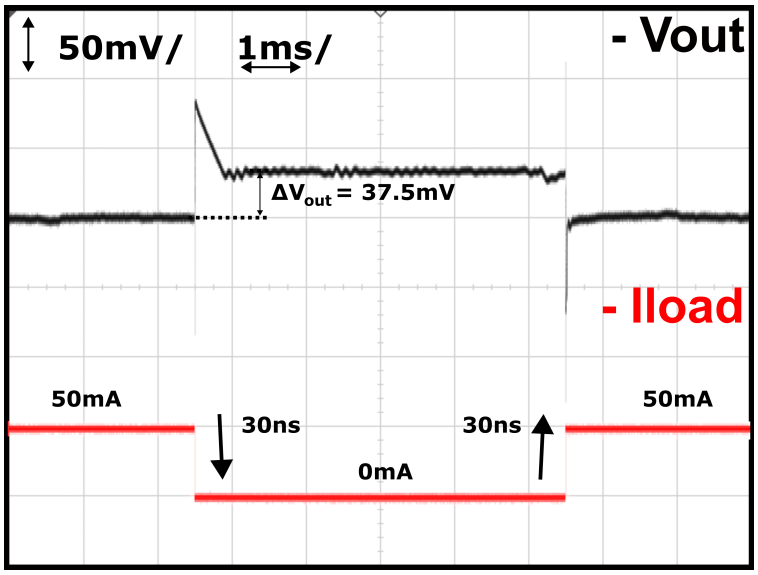


Figure 3.25: Transient response of a full load step measured from the proposed LDO.

with a larger 81.25mV voltage droop. These results reflect the LDO's ability to quickly stabilize after load changes, though the larger droop during load increase indicates potential areas for optimizing voltage regulation under rapid transients.

3.4 Summary

This chapter details the development of a low quiescent current, wide load range LDO, aimed at meeting the stringent demands of SoC battery-powered devices by enhancing stability with a zero-tracking network, while consuming minimal current. Building on existing techniques, this work introduces nested compensation loops to improve Miller compensation, achieving necessary stability without a significant increase in current draw. The design focuses on minimizing both static and dynamic current demands, effectively managing the pole and zero introduced by the output capacitor and its ESR. The LDO, fabricated using the TSMC 180nm process, shows strong quiescent current performance, particularly at low loads where the current stabilizes after an initial peak, outperforming comparable designs in the literature. While the LDO demonstrates effective load transient response, PSRR, and input-output voltage characteristics, further optimization in handling rapid transients and high-frequency noise is noted. This work advances LDO design by offering a more efficient solution for modern low-power applications.

Table 3.4: Comparison With Previously Published Works

	[21] 2015*	[22] 2020	[23] 2022	[24] 2023	This Work
Technology [nm]	130	180	180	28	180
Chip area [mm^2]	0.08**	0.017	0.037	-	0.0145
V_{out} [V]	1.65	1.2	1.6-2.3	0.4	1.8
I_{Load} [mA]	20	150	200	10	50
C_O [μF]	.002	4.7	1	1	4.7
V_{do} [mV]	-	200	200	200	100
ΔV_{out} [mV]	-	36.88	78	10	37.5
I_Q [μA]	7.5	13.5	0.9-160	0.0135	0.486
Undershoot [mV]	310	20	78	10	81.25
Overshoot [mV]	270	17	30	-	52.5
Current efficiency [%]	99.96**	99.0	99.90	98.4	99.96
FoM*** [ps]	-	104	1.76	1.35	40.89

(* Simulated ** Estimated)

$$^{***}\ FoM = \frac{C_O \cdot \Delta V_{out} \cdot I_Q}{I^2_{Load_{(max)}}}\ [19] \tag{3.14}$$

Chapter 4

CONCLUSIONS AND FUTURE WORK

4.1 Conclusions

In this work, the design and analysis of a low quiescent current low dropout regulator is given. Background information on the many available topologies in LDO research is presented, demonstrating the limitations of each. This background allowed for the proposed design to contribute to the state of the art. Demonstrating this contribution, this work was accepted to be published in-proceedings at the 2024 NEWCAS IEEE conference.

- Z. Williams, L. Chen, Y. Zhou, and Z. Bai, "A 580 nA Quiescent Current Low-Dropout Regulator with Zero-Tracking for Wide Load Applications," 2024 Proceedings of the 22nd International NEW Circuits and Systems conference, Sherbrooke, Canada, 2024.

The design proposed uses a novel zero tracking technique to improve stability while maintaining low quiescent current draw. This technique is seen to be new to the literature and is a large contribution that this work provides. The introduction of a zero which is tied to the output impedance of the pass element allows for a wide load range with stability through that whole range. The proposed design has a peak measured current efficiency of 99.6% being very high in the state of the art. This is achievable by including cascode current mirroring stages, a low biasing current error amplifier and a high resistance feedback network. These techniques in conjunction with an increase in transistor sizing provide a

measured quiescent current of 486.67 nA. This can be further diminished when the enable circuitry is utilized, reducing the quiescent current draw when in a disabled state to 2.06 nA.

With the zero tracking unit, ϕ_M is improved over the full range. With a no load condition, ϕ_M is 60° which is a wide margin promoting fast transient performance with small ripple. When the load drops from full to no load, the settling time is measured to be 418 μs with an overshoot of 52.5 mV. Conversely, when the load increases through the full range, the response is much faster with a 36.5 μs settling time but with a larger 81.25mV voltage droop. Overall the proposed LDO exhibits very desirable qualities for use in SoC applications, specifically being those requiring such low current draw.

4.2 Future Work

The goal of future work is to improve the protection of the circuit to ESD and other unwanted damaging stimuli. When testing was conducted, the circuit exhibited difficulty in rejecting noise and was found to be damaged when given inputs outside the intended range. PSRR can be improved, with a low frequency rejection of -30 dB being dissatisfactory in the state of the art. Future improvements to layout are also intended, with superior matching and area optimization being attainable goals. Furthermore, optimization of the exact relationship which the zero tracking network has to the load can better increase ϕ_M.

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