Self-Balancing Five-Level Current Source Inverters

By

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Abstract

Five-level current source inverters (CSIs) inherit the advantages including voltage-boosting capability, absence of dv/dt issues, and reliable short-circuit protection, etc. In addition, they have better harmonic performance compared to traditional three-level CSIs. Many five-level CSI topologies have been proposed for various applications such as wind energy conversion systems and high-power AC drives. However, traditional topologies, using parallel structures of modules or inductors, suffer from a common issue: current imbalance.

The main cause of current imbalance is the unequal on-state voltages of switching devices, along with manufacturing tolerances and variations in the gating signal delays. This imbalance can degrade AC output quality, and potentially lead to overcurrent conditions that may damage components. The existing recommended solutions involve closed-loop control, using additional current sensors to sample DC inductor currents and adjust switching states accordingly. However, even the optimal approaches in the literature have drawbacks, such as increased switching frequency, high computational demands, and higher costs.

To address the issue of current imbalance, three novel topologies: X-, Γ-, and H-type five-level CSIs have been proposed in this work. Unlike traditional five-level topologies, the proposed CSIs achieve self-balance of the inductor currents without using additional balancing control schemes. This reduces the complexity and cost of the system. New SVM-based modulation schemes, designed for the proposed inverters, ensure good harmonic performance and overvoltage clamping. Detailed analysis and calculations are provided for their configurations, operating principles, self-balancing mechanisms, modulation schemes, DC utilization, switch stresses, passive component sizes, and overall efficiency. The performance of the proposed inverters is validated through both simulations and lab-scaled experiments.

Acknowledgments

I would like to express my sincere gratitude to my supervisor, Dr. Qiang Wei for providing his invaluable guidance, comments, and suggestions throughout the course of the project.

To all relatives, friends, and others who in one way or another shared their support morally, financially and physically, thank you.

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List of Symbols

Symbol	Meaning
C_f	filter capacitor
D	duty cycle
D_1-D_4	diodes
G_v	voltage gain
f_{sp}	sampling frequency
f_{sw}	switching frequency
I_{dc}	DC current
I_{ref}	reference current vector
i_L	inductor current
i_w	PWM output current
I_{w1}	RMS value of the fundamental component of i_w
i_s	output sinusoidal current
L_{dc}	DC inductor
L_f	load inductor
m_a	modulation index
R	load resistor
S_1-S_{12}	switches
Δt	dwell times
T_s	sampling period
V_{dc}	DC voltage
V_{LL}	output line to line voltage
V_{in}	input voltage
w	angular frequency
φ	power factor angle
θ	space vector angle

List of Abbreviations

Abbreviation	Meaning
CSI	current source inverter
CSR	current source rectifier
EV	electric vehicle
GCT	gate-commutated thyristor
GTO	gate turn-off thyristor
IGBT	insulated gate bipolar transistor
LCC	line-commutated converter
MFT	medium-frequency transformers
MMC	modular multilevel converter
MOSFET	metal-oxide-semiconductor field-effect transistor
MV	medium voltage
PV	photovoltaic
PWM	pulse width modulation
SCR	silicon-controlled rectifier
SGCT	synchronous gate-commutated thyristor
SHE	selective harmonic elimination
SVM	space vector modulation
SQ	sequence
THD	total harmonic distortion
TPWM	trapezoidal pulse width modulation
VSI	voltage source inverter

Chapter 1

Introduction

The PWM current source inverter (CSI) is favored for its simple converter topology, motor-friendly waveforms, and reliable short-circuit protection, making it a widely discussed and used converter [1]. Unlike the voltage source inverter (VSI), which maintains a constant voltage on the DC link, the CSI is fed by a constant DC current, with AC-side currents being pulse-width modulation (PWM) waveforms. A capacitor filter is required on the CSI output side for device commutation, and a DC inductor is necessary to support the constant DC current. Commonly used for high power applications, such as high-voltage direct current (HVDC) systems [2] and high-power medium-voltage (MV) drives [3], are the line-commutated converter (LCC) using silicon-controlled rectifier (SCR) thyristors, which rely on the load's leading power factor for commutation, and PWM CSIs employing gate-commutated thyristors (GCTs) [4] or gate turn-off thyristors (GTOs) [5]. With the development of commercialized reverse-blocking devices, PWM CSIs are also suitable for low power applications, such as photovoltaic (PV) systems [6] and electric vehicles (EV) [7].

This chapter begins by discussing the conventional configuration of the three-level PWM CSI. It explores various modulation schemes, and reviews common CSI applications. Next, the chapter introduces five-level CSIs, presenting and analyzing different topologies found in the literature. Finally, it addresses the technical challenge of current imbalance in five-level CSIs, discussing its occurrence, causes, consequences, and potential solutions. Based on this introduction, the research objective is identified.

1.1 Conventional three-level current source inverter

This section covers the conventional three-level current source inverter. It introduces the configuration of the CSI, detailing its components and the common modulation schemes, including space vector modulation (SVM) [8], trapezoidal pulse width modulation (TPWM) [9], and selective harmonic elimination (SHE) [10]. Additionally, the section discusses the applications of the CSI such as high-power medium-voltage drives, wind energy conversion systems, and photovoltaic system.

1.1.1 Configuration of current source inverter

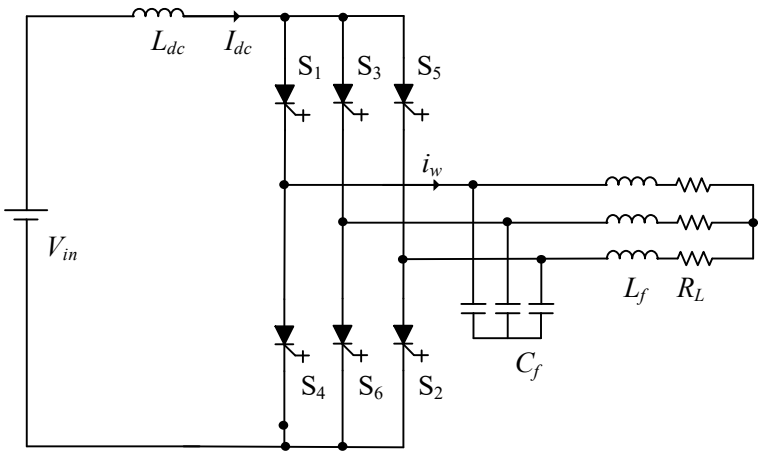


Fig. 1-1 Conventional three-level current source inverter.

The configuration of a conventional three-level PWM CSI is illustrated in Fig. 1-1. This inverter consists of six switching devices, each of which can be replaced by two or more series devices for medium voltage applications. These switching devices are with reverse voltage blocking capabilities. The inverter generates a defined PWM output current i_w. On the DC side, the DC current I_{dc} is generated by the voltage source V_{in} in series with a DC inductor L_{dc}. To facilitate the commutation of the switching devices, the inverter typically requires a three-phase capacitor C_f at its output. For example, when switch S_1 turns off, the inverter's PWM current i_w drops to zero quickly. The capacitor

provides a path for the energy trapped in the phase-A load inductance, preventing high-voltage spikes that could damage the switching devices [11]. Additionally, the capacitor acts as a harmonic filter, enhancing the quality of the load current and voltage waveforms.

The modulation schemes used in CSI mainly includes space vector modulation (SVM), selective harmonic elimination (SHE), and trapezoidal pulse width modulation (TPWM):

SVM:

SVM is an online modulation scheme with superior dynamic performance, the DC current utilization (the ratio of maximum rms fundamental-frequency current $I_{w1,\,max}$ to DC-link current I_{dc}) of which is 0.707 [12]. Fig. 1-2 illustrates the space vector diagram for a CSI, where I_{ref} represents the current reference vector and rotates at a fixed angular velocity in space, θ is the angle I_{ref} turns. Under the switching constraint, the three-phase inverter has a total of 9 switching states listed in Table 1-1, including three zero states and six active states. For example, when S_1 and S_4 in CSI are turned on at the same time, the other four switches are all in the off state and the corresponding space vector is I_0.

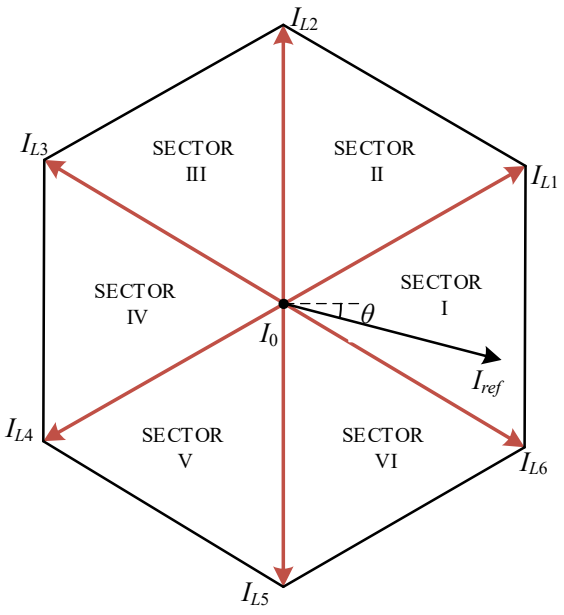


Fig. 1-2 Space vector diagram for CSI.

For a given length and position, I_{ref} can be synthesized from three nearby fixed vectors, and based on these vectors, the switching state of the inverter can be selected. When I_{ref} crosses different sectors, different switches will be turned on or off. The length of I_{ref} determines the magnitude of the output current, and the speed of I_{ref} corresponds to the output frequency of CSC. The dwell time (T_1, T_2, T_0) of the selected vectors in Sector I is calculated as shown in (1-1) [13].

$$\begin{cases} \vec{I}_{ref} T_s = \vec{I}_1 T_1 + \vec{I}_2 T_2 + \vec{I}_0 T_0 \\ T_1 = m_a \sin(\frac{\pi}{3} - \theta) T_s \\ T_2 = m_a \sin(\theta) T_s \\ T_0 = T_s - T_1 - T_2 \end{cases} \tag{1-1}$$

where m_a is the modulation index, θ is the angle of I_{ref}, T_s is the sampling period. I_1 and I_2 are the active space vectors in Sector I, active space vectors will change in other sectors.

Table 1-1 Switching states and space vectors

Type	Space vector	On-state switches
Zero states	$\vec{I}_0$	S_1&S_4
		S_2&S_5
		S_3&S_6
Active States	$\vec{I}_1$	S_6&S_1
	$\vec{I}_2$	S_1&S_2
	$\vec{I}_3$	S_2&S_3
	$\vec{I}_4$	S_3&S_4
	$\vec{I}_5$	S_4&S_5
	$\vec{I}_6$	S_5&S_6

Switching sequence design needs to follow two requirements for the minimization of switching frequencies: 1) Only two switches are involved (one being turned on and one being turned off) when switching between two switching states; and 2) Requiring the

minimum number of switching when I_{ref} traverses different sectors. Fig. 1-3 (a) shows an example of the sequence SQ1 in each sampling period T_s. The sampling frequency f_{sp} is 1080Hz, and there are 3 vectors in each T_s, which occupy dwell time T_1, T_2 and T_0, respectively. The device switching frequency f_{sw} is 540 Hz, corresponding to nine pulses of i_w in Fig. 1-3(b).

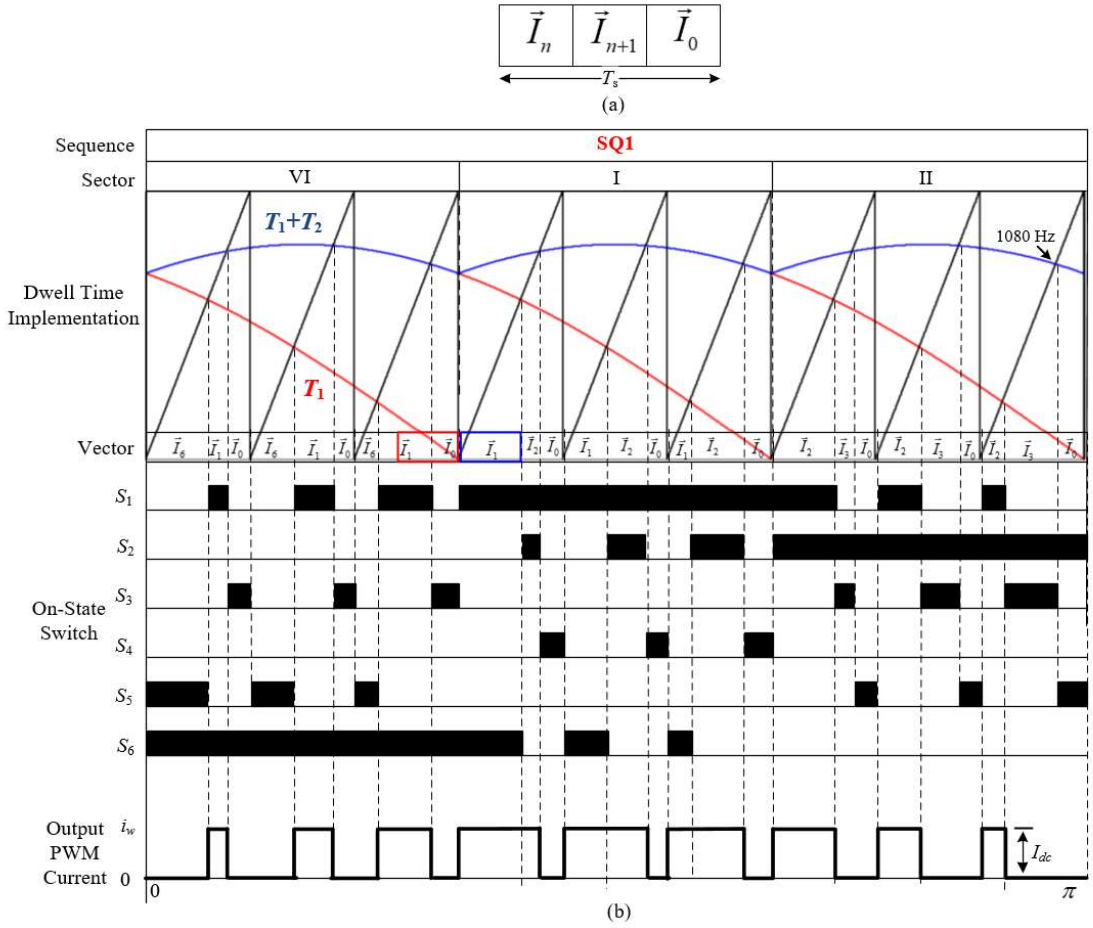


Fig. 1-3 SVM switching sequence SQ1.

SHE:

SHE is an offline modulation scheme that can eliminate a couple of unwanted low-order harmonics in the inverter PWM current i_w [14]. It's implemented by pre-calculating the switching angles and then importing them into the digital controller. Fig. 1-4 shows a 9-pulse SHE waveform (f_{sw} = 540 Hz) that satisfies the switching constraint for the CSI. In the first half cycle (0- π), there are nine pulses (N_p = 540/60 = 9) with 9 switching

angles (different number of switching angles under different f_{sw}) in the first π/2 period. However, only 4 out of 9 angles (θ_1 - θ_4) are independent. Given these 4 angles, all other switching angles can be calculated. These 4 switching angles provide 4 degrees of freedom and can be used to eliminate 4 different harmonics in i_w. Different sets of harmonics can be eliminated by the combination of different switching angles, and the values of these angles can be obtained by solving different equations. By using the Newton–Raphson Iteration Algorithm, the specific values of the switching angles are calculated. When using different combinations of switching angles, the DC current utilization of SHE will float within 0.73-0.78.

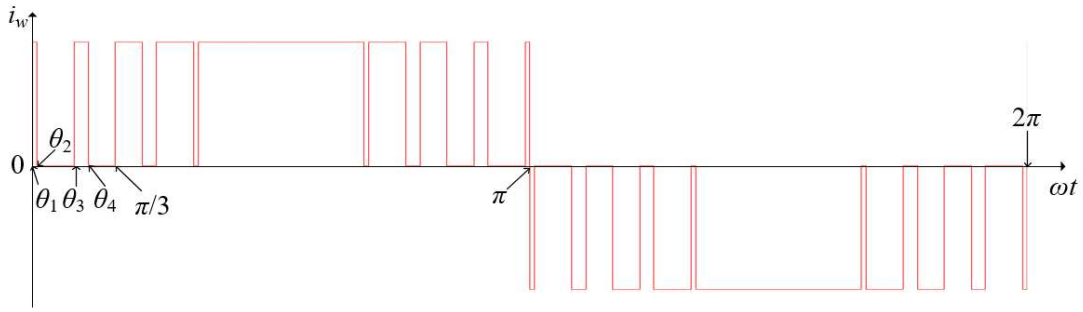


Fig. 1-4 Selective harmonic elimination scheme.

TPWM:

Fig. 1-5 shows the principle of TPWM when the switching frequency f_{sw} = 540 Hz. The signals for switches are generated by comparing the modulating wave with the carrier wave [15]. In each cycle: 1) the modulating wave is a trapezoidal wave, which is at low level in half a cycle, and at high level in the middle one-third of the other half cycle; 2) the carrier wave equals to zero when the modulating wave reaches high level or low level; and 3) the carrier wave is a triangle wave the rest of time, and the frequency of which is related to f_{sw}. The signals of other switches can be obtained by shifting the signal for S_1. It is worth mentioning that there is no zero state in TPWM, which means the bypass operation cannot be performed. And because of this, its DC current utilization is higher than SVM, which is 0.74. The active states are the same as the SVM in Table 1-1.

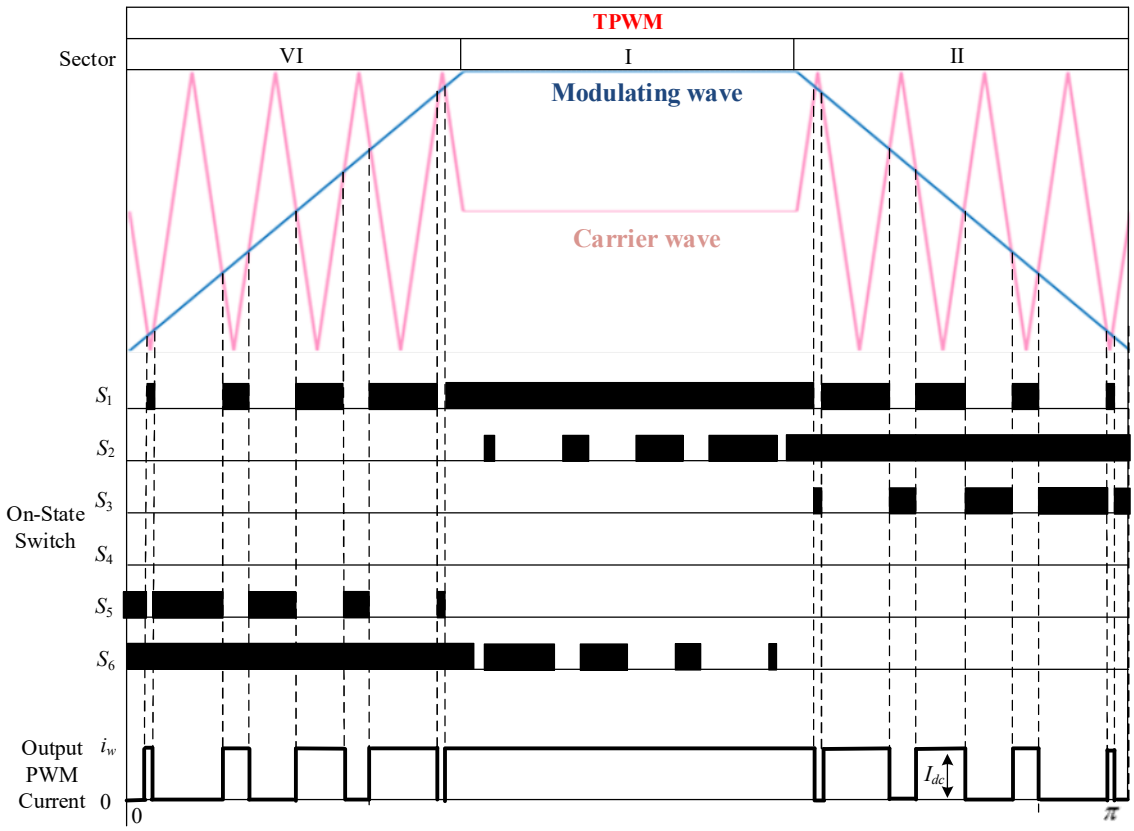


Fig. 1-5 Trapezoidal pulse width modulation.

1.1.2 Applications of current source inverter

The current source converters have been widely used in industry for decades, with its adoption evolving alongside advancements in CSC semiconductors. CSCs have been employed in high-power applications such as wind energy conversion systems and high-power medium-voltage drives. In recent years, the development of new devices, control, and modulation strategies has expanded the use of CSCs to high-switching applications, including photovoltaic systems and electric vehicles, etc. This section will provide a brief overview of the current state of CSC applications in industry.

High power medium voltage drives:

The current source inverter is ideally suited for medium voltage (MV) drives. CSI-fed drives offer a simple converter structure, motor-friendly waveforms, inherent four-quadrant operation capability, and reliable fuseless short-circuit protection, although they may have a slower dynamic response compared to VSI drives [16]. Most installed MV drives are used in applications where dynamic performance is not the primary requirement, such as high-power fans [17], pumps [18], compressors [19], and ship propellers. Consequently, CSI drives are well-suited for these types of applications. The switching devices depicted in Fig. 1-6 are synchronous gate-commutated thyristors (SGCTs), and the power rating for PWM current source drives typically ranges from 1 to 10 MW, with the potential for further increase through parallel inverters. For power ratings up to 100 MW, load-commutated inverters (LCIs) are preferred, as they offer cost and efficiency advantages that voltage source inverters (VSIs) typically cannot match [20].

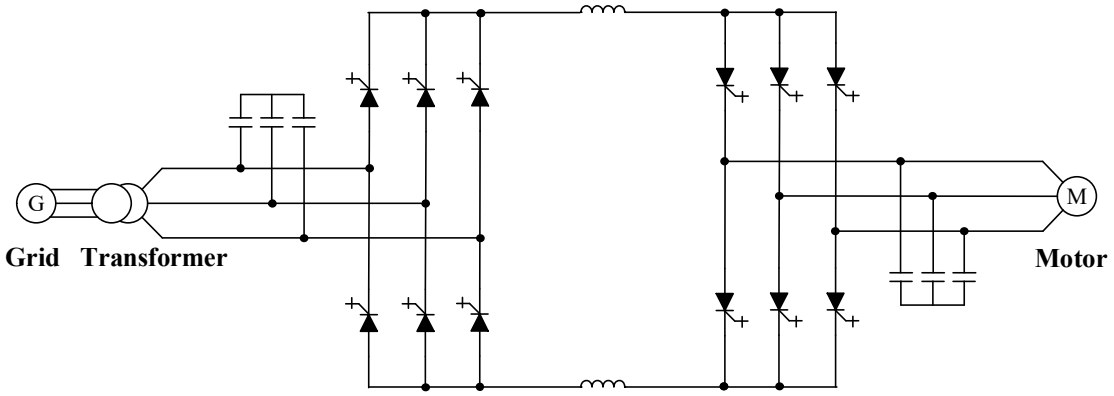


Fig. 1-6 PWM CSC-fed MV drive.

Wind energy conversion systems:

Offshore wind farms are often located far from onshore grid connections, making high voltage direct current (HVDC) transmission a viable solution for distant wind power generation. Traditionally, load-commutated converter-based HVDC (LCC-HVDC) systems have dominated the market due to their high-power rating, reliability, and efficiency [21]. In addition to conventional LCC-HVDC, PWM CSC-based HVDC

systems has self-commutated ability and can provide independent active and reactive power control [22]. To leverage the features of PWM CSC, such as reactive power control, operation without commutation voltage, and a relatively small footprint with improved harmonic performance over LCC schemes, a hybrid CSC-HVDC system was proposed [23]. This system employs a PWM CSC on the offshore wind turbine side to reduce the footprint and connects to the onshore grid through a DC cable and LCC, as shown in Fig. 1-7. This topology combines the advantages of both PWM CSC and LCC techniques for offshore wind applications. To further eliminate the need for costly and bulky offshore step-up transformers, some studies have explored series-connected PWM CSC systems to increase the power rating for high-voltage applications, treating each CSC as a module [24]. Series-connected PWM CSCs on both the offshore generator side and the onshore grid side were also discussed. On the offshore generator side, DC voltage ranging from 100 to 150 kV can be achieved by cascading an appropriate number of MV wind generators through PWM CSCs, thereby eliminating the need for a costly and bulky step-up transformer [25]. Furthermore, recent research has explored modular medium-frequency transformers (MFT) and series/parallel connection-based configurations, which can further enhance system performance [26].

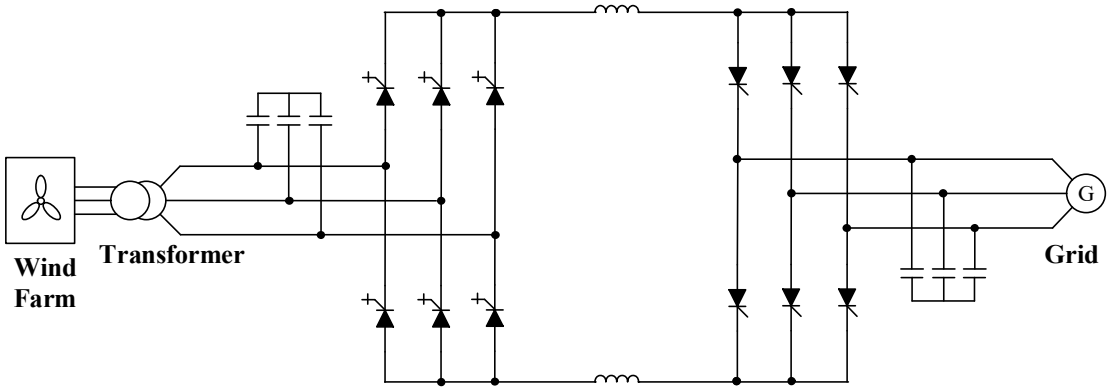


Fig. 1-7 Current source HVDC system for offshore wind conversion system.

Photovoltaic Systems:

Conventionally, the CSI applications are primarily in high-power fields where the switching frequency is limited to hundreds of hertz to minimize switching losses [27]. With the development of new switching devices such as GaN MOSFET, CSI can also be

used in low-power applications with high switching frequencies, such as grid-interfacing photovoltaic (PV) converters, electric vehicle (EV) applications, etc. Fig. 1-8 illustrates a typical single-stage boost CSI-interfaced PV application, where the boost DC/DC converter is eliminated compared to the two-stage DC/DC plus DC/AC voltage source inverter (VSI)-based PV system. This configuration results in higher efficiency and a simpler control scheme [28]. Additionally, the CSC-based PV system offers improved reliability due to its inherent short circuit protection and the elimination of the unreliable DC capacitor found in VSIs [29].

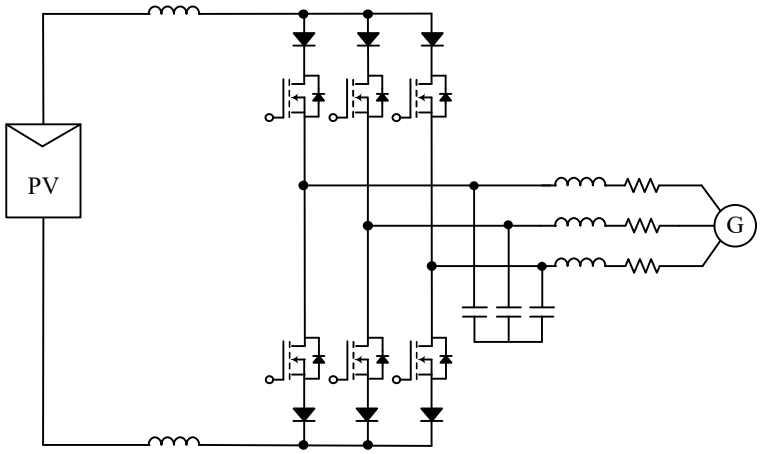


Fig. 1-8 CSI-based PV system.

1.2 Five-level current source inverters

This section covers the five-level current source inverters. Compared to the conventional three-level CSI, five-level CSIs are attracting increased attention because of their natural advantage of better harmonic performance and many topologies have been proposed [30-38]. As shown in Fig. 1-9, the existing five-level CSI topologies can be divided into two categories: the one with equivalent current sources realized by a voltage source and DC inductors [30-36], and the one with independent current sources [37-38].

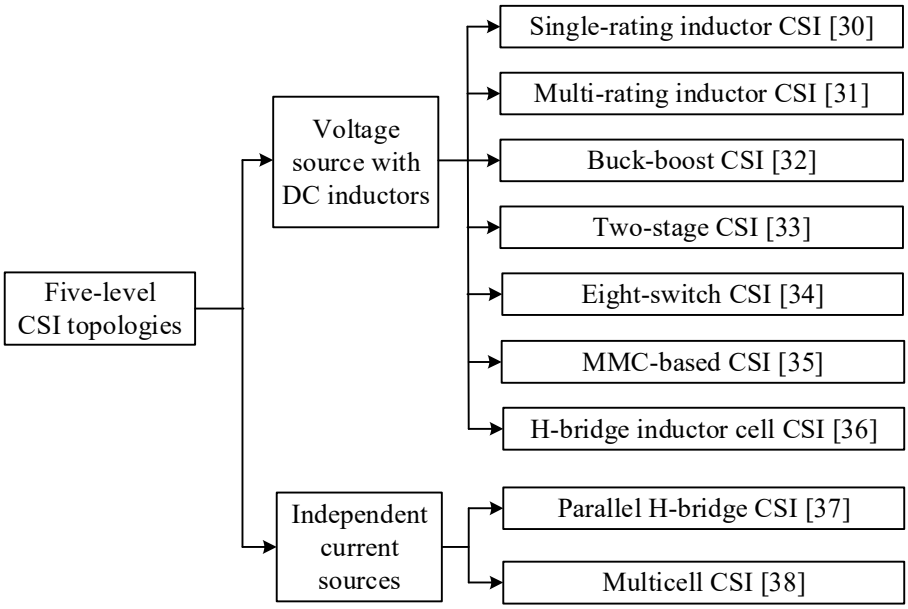


Fig. 1-9 Existing five-level CSI topologies.

1.2.1 Five-level current source inverters with dependent current source

Using a voltage source and DC inductors to generate equivalent current sources is the most common way to achieve five-level. Usually, the induced current sources are supplied to six-switch CSI modules, and the outputs of both modules are connected in parallel, superimposing the output current together to achieve five-level operation. In addition, some topologies use parallel inductors to change the DC current supplied to a single CSI module to achieve multilevel. The topologies of this category are described in detail below:

Single-rating inductor five-level current source inverter:

A five-level topology of a single-rating inductor MLC is illustrated in Fig. 1-10. It consists of two six-switch CSI modules, producing five levels ($\pm I_{dc}$, $\pm 2I_{dc}$, and 0) in the output current waveform. Each module in the single-rating inductor five-level CSI comprises three-phase legs, each with top and bottom inductors, and one top and bottom

semiconductor device per leg. The DC inductors reduce the current ripple of the module and ensure equal impedance among phases. Diodes connected in series with the switches provide reverse voltage blocking capability. The inverter is named as single-rating inductor multilevel current source converter because the input DC current is evenly distributed among the inductors, making both inductors of the same current rating [30]. This topology offers advantages such as increased current capacity and improved harmonic performance, as the PWM current levels are increased to five. The main technical challenges are the current imbalance between each CSI module and the necessity for two bulky and expensive DC inductors.

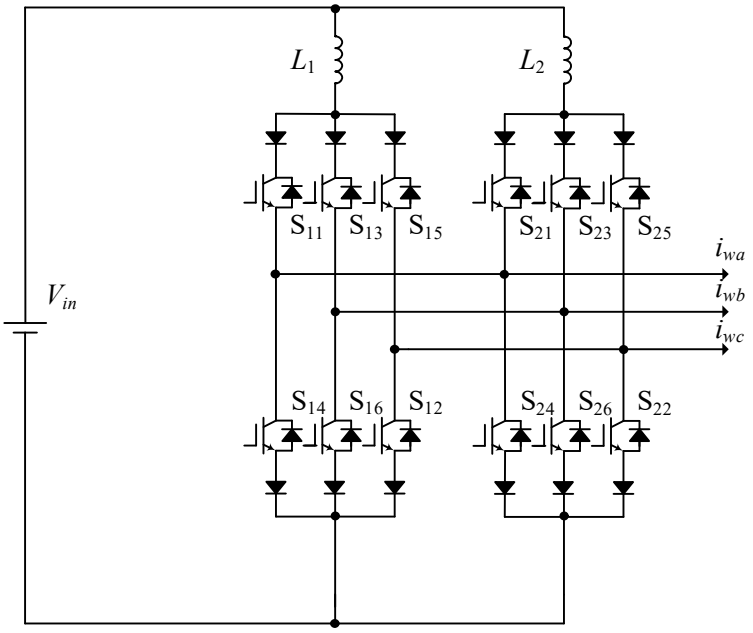


Fig. 1-10 Single-rating inductor five-level CSI.

Multi-rating inductor five-level current source inverter:

The multi-rating inductor five-level CSI is shown in Fig. 1-11. Similarly, the topology adopts two six-switch modules to generate five-level current outputs. Two different inductors ($L_1 \neq L_2$) are employed to split the input current [31], and there are no passive components in the six switch CSI modules, as shown in Fig. 1-11. With the design, the total size of DC inductors is reduced compared to the single-rating inductor CSI, resulting in reduced cost and volume, and lower losses. Besides, this topology inherits the advantages of increased current capacity and improved harmonic

performance, as the PWM current levels are increased to five. However, the problem of current imbalance still exists.

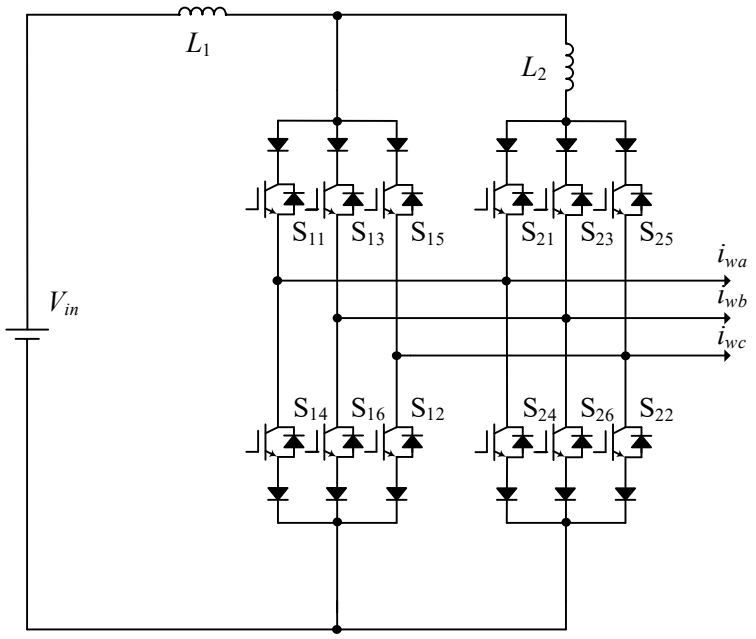


Fig. 1-11 Multi-rating inductor five-level CSI.

Buck-boost derived five-level current source inverter:

The buck-boost derived five-level CSI, illustrated in Fig. 1-12, distinguishes itself from other five-level CSIs that typically aim for voltage boost by employing a buck-boost technique to achieve low voltage output. This converter uses a voltage source along with two inductors and two six-switch CSI modules to generate a five-level output current waveform. Additional switch devices S_7 and S_8 effectively isolate the input DC rails and manage the charging and discharging processes of the DC inductors L_1 and L_2. With optimized modulation, switch S_8 can be eliminated without affecting the operation principle or performance. While other topologies struggle to maintain a constant output voltage when the input voltage varies, the buck-boost topology overcomes this issue, operating across a wide voltage conversion range with a minimal number of components [32]. The topology faces challenges related to overvoltage during mode transitions and the large size of the DC inductors.

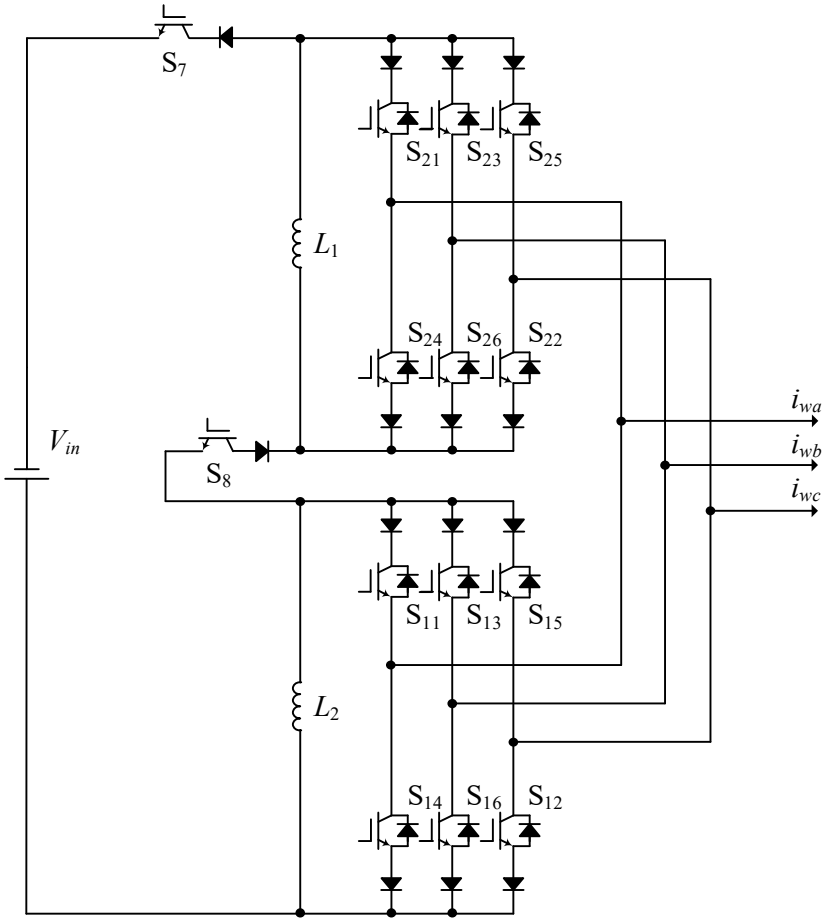


Fig. 1-12 Buck-boost derived five-level CSI.

Two-stage five-level current source inverter:

The configuration of two-stage five-level CSI is depicted in Fig. 1-13. Unlike the previously discussed topologies, it consists of a single six-switch CSI module and a DC-DC boost converter stage with four semiconductor devices. The boost stage operates at the designed switching frequency, while the six-switch CSI operates at the fundamental frequency. The boost stage provides different DC current levels to the six-switch CSI by controlling the DC-DC switching devices [33]. Compared to the above topologies with two CSI modules, the topology can achieve five-level output with reducing the switch count at the CSI side. However, it faces the technical challenges include the high number of devices in the DC-DC converter and the high rating requirements of the devices in the six-switch CSI.

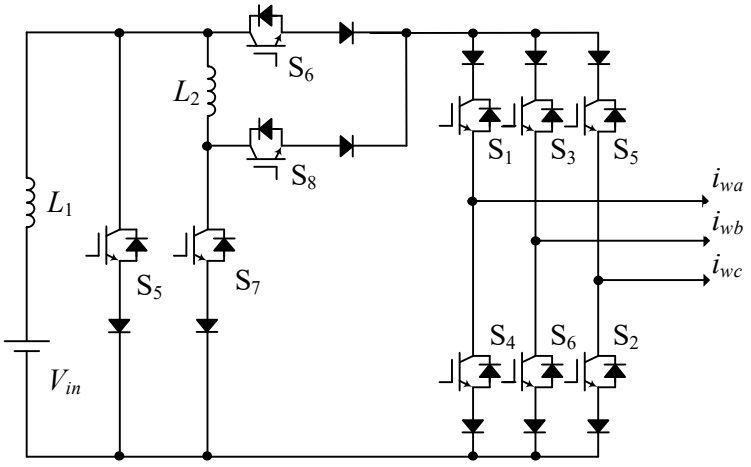


Fig. 1-13 Two-stage five-level CSI.

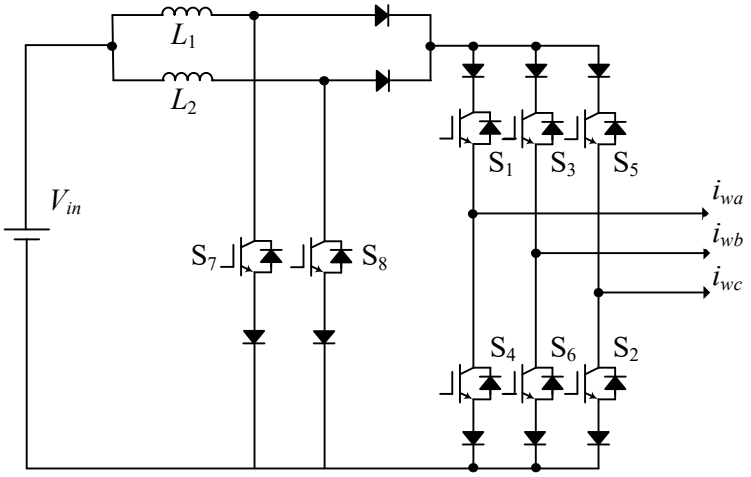


Fig. 1-14 Eight-switch five-level CSI.

Eight-switch five-level current source inverter:

Fig. 1-14 shows the eight-switch five-level CSI. Like the two-stage five-level CSI, eight-switch CSI only adopts one six-switch CSI module. The five-level output current is generated by adjusting the DC current level injected into the H6 CSI module [34]. By controlling the gating signals of switches S_7 and S_8, respective bypass loops for parallel inductors L_1 and L_2 can be generated, allowing the DC current level to be I_{L1} ($I_{L1} = I_{L2}$), $2I_{L1}$, and 0.

The topology has the advantage of reducing switch count compared to the two-stage five-level CSI. Compared with topologies with two CSI modules, the current rating of the CSI switches is doubled. The major technical challenge is the imbalance current on inductors caused by the parallel-connected inductor structure.

Modular multilevel converter-based current source inverter:

Fig. 1-15 shows the modular multilevel converter (MMC)-based CSI. The configuration of MMC has three arm-legs for three phases, and each leg has two arms, one for the positive rail and another for the negative rail. The arm comprises several modular cells to produce a multilevel output waveform. The inductor-based cells, such as the half-bridge cells or the full-bridge cells shown in Fig. 1-15, are inserted or bypassed in each arm of the converter to control the output current. The MMC's biggest advantage is its modular structure. However, the dangerous open-circuit fault (common for all current source converters) has a high possibility in MMC due to its larger number of inductors [35]. Additional antiparallel connections of press-pack diodes or thyristors need to be adopted to provide an emergency current path. Also, the large number of components and the current imbalance are common issues for MMC.

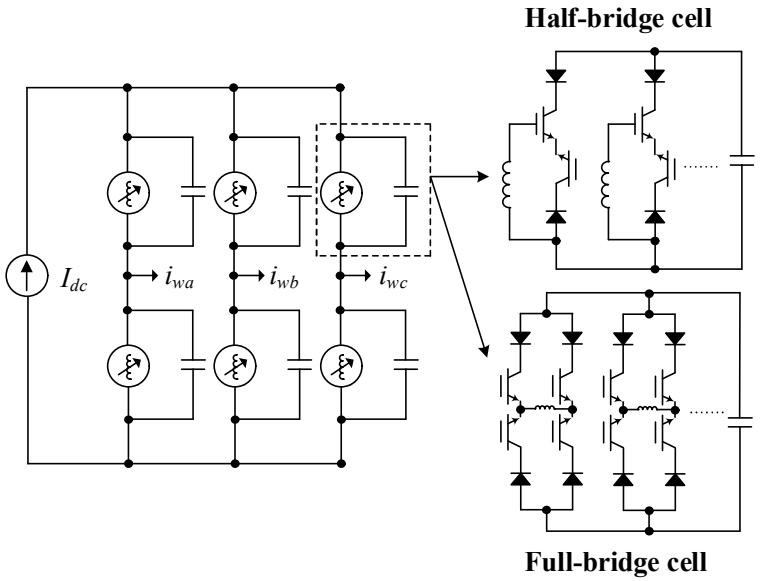


Fig. 1-15 MMC-based CSI.

H-bridge with inductor cell five-level current source inverter:

Fig. 1-16 illustrates the configuration of the H-Bridge with inductor cell five-level CSI. This single-phase CSI consists of a four-switch H-bridge and a four-switch inductor cell. Additional inductor cells can be employed to further increase the output levels. The CSI H-bridge serves as the main inverter, followed by the parallel connection of one or more inductor cells acting as auxiliary circuits. The inductor in the cell can either be connected in parallel with the loads or disconnected. When connected in parallel, the current passing through the inductor cell equals the total output current at the load, which is half of the H-bridge output. With the two operation modes of the inductor cell, the inverter achieves a five-level current at the load. The main technical challenges include current imbalance between the load and the inductor cell, as well as the need for high current rating components in the inductor cell [36].

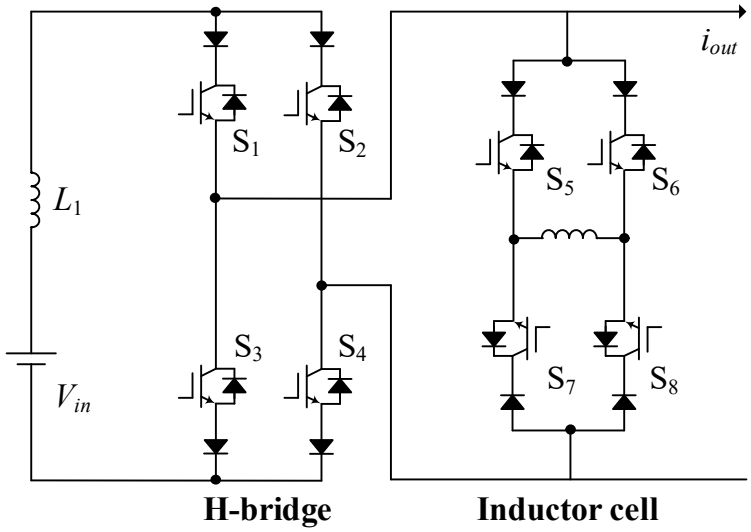


Fig. 1-16 H-Bridge with inductor cell five-level CSI.

1.2.2 Five-level current source inverters with independent current sources

Using independent current sources for each CSI module is another method to achieve five-level output currents. By connecting the outputs of two modules and ensuring that the current sources are equal, balance between the separate modules can be maintained.

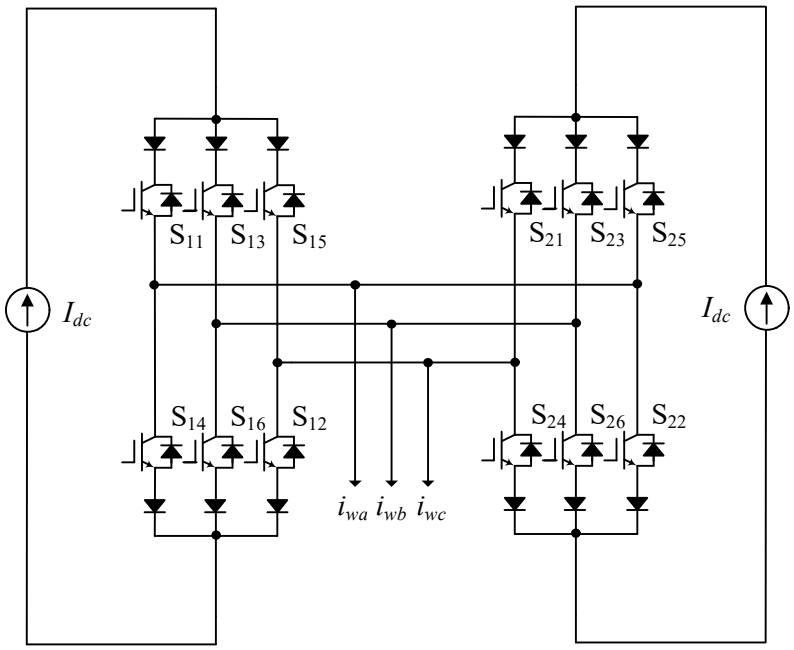


Fig. 1-17 Parallel H-bridge five-level CSI.

Parallel H-bridge five-level current source inverter:

Fig. 1-17 shows the parallel H-bridge five-level CSI. The configuration can be derived from the single-rating inductor multilevel CSI with the voltage source and parallel-connected inductors replaced by independent equal current sources. The parallel H-bridge five-level CSI consists of two six-switch CSI modules, producing five levels ($\pm I_{dc}$, $\pm 2I_{dc}$, and 0) in the output current waveform. Same as other topologies, the five-level output offers advantages such as increased current capacity and improved harmonic performance [37]. Besides, the current imbalance issue in the CSI side is solved with independent equal current sources. However, deriving independent equal current sources is a hard work. Usually, several CSRs with phase-shifting transformers need to be

adopted, and balance control is also necessary to equalize the current sources. These will add to the cost and complexity of the system.

Multicell current source converter:

Fig. 1-18 shows the multicell CSC. The topology adopts an input transformer, H6 CSR modules, and single-phase CSI modules. Each phase consists of three identical cells connected in series. Each cell consists of an LC filter, a six-switch CSR module, DC inductors, and a single-phase CSI module. At the inverter side, the output is connected in series. Therefore, the converter output has a high-voltage, low-current feature. More cells can be adopted to acquire even higher output voltage while the output current remains the same. This topology is specified for high-voltage, low-current applications with the modular modules offering the five-level or even more levels output current [38]. The current imbalance is still a concern while generating equal current sources like parallel H-bridge CSIs.

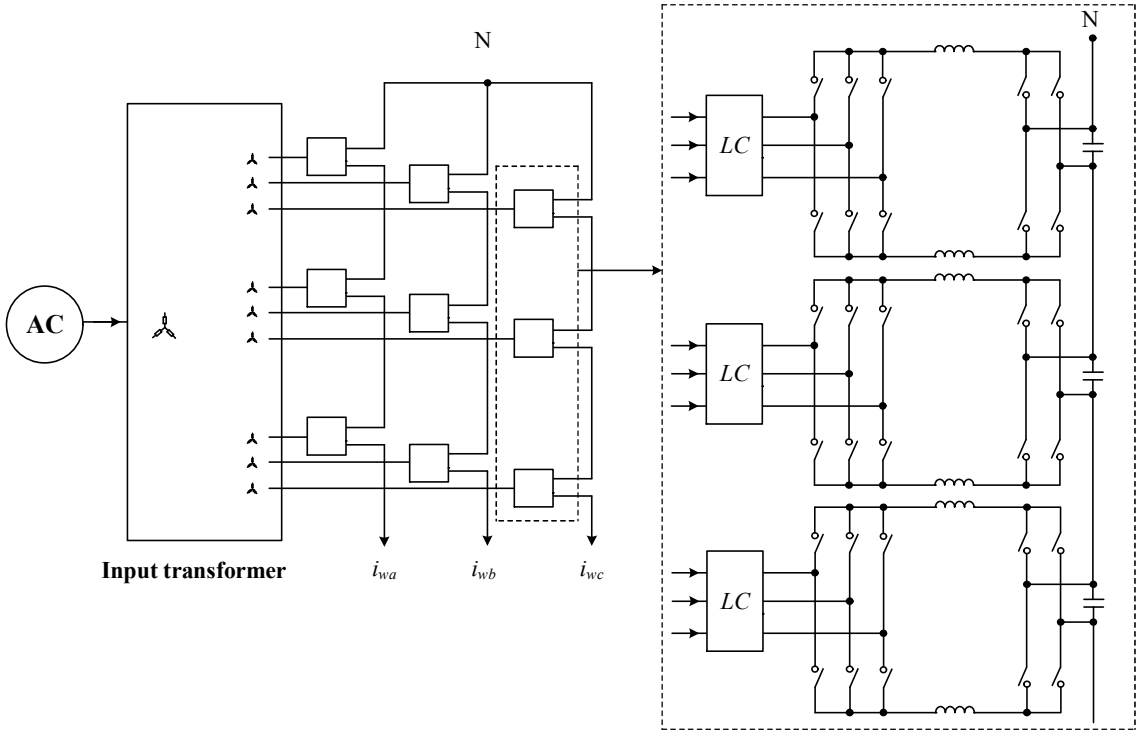


Fig. 1-18 Multicell CSC.

1.3 Current imbalance of five-level current source inverters

As discussed in the previous section, current imbalance is a major concern for five-level current source inverters. This imbalance can occur between the DC inductors or DC modules in topologies that use a voltage source and DC inductors, or during the generation of equal current sources in topologies with independent current sources. The primary cause of DC current imbalance is the unequal state voltages of switching devices [39]. Additionally, manufacturing tolerances of the components and variations in the time delay of the gating signals of the parallel inverters can also contribute to current imbalance [40]. Unbalanced DC current can degrade the quality of the AC output, increase harmonics, and necessitate larger filters. More critically, current imbalance may lead to overcurrent conditions, potentially damaging components [41]. This section delves into the mechanism of current imbalance, detailing existing solutions. By examining these solutions, their limitations are discovered, leading to the identification of the research objective.

1.3.1 Mechanism of current imbalance

The main reason of the DC current imbalance is the unequal state voltages of the switching devices. The general DC-link equivalent circuit of typical single-rating inductor five-level CSI is illustrated in Fig. 1-19. In this circuit, L_1 to L_4 are equal inductors, R_1 to R_4 represent the choke internal resistances, and V_1 to V_4 denote the inverter-side DC-link voltage, with values corresponding to the output phase voltage based on switching states. I_p and I_n indicate the total positive and negative DC current, respectively. The positive DC current for each CSI is represented by i_1 and i_3, while the negative DC current is represented by i_2 and i_4. For simplicity, the on-state voltages of semiconductor devices and voltage drops across the inductor internal resistances are neglected. The DC-link current can be expressed as follows:

$$\begin{cases} \Delta I_p = i_1 - i_3 = \dfrac{1}{L}\int (V_1 - V_3)dt \\ \Delta I_n = i_2 - i_4 = \dfrac{1}{L}\int (V_2 - V_4)dt \end{cases} \tag{1-2}$$

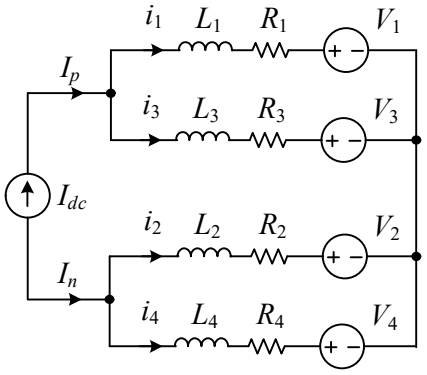


Fig. 1-19 Equivalent circuit of the single-rating inductor five-level CSI.

where Δi_p and Δi_n represent the DC-link current difference between the positive and negative buses of the two CSIs. To balance the DC current, Δi_p and Δi_n should be minimized to near zero. As V_1 to V_4 vary with switching states, the switching states of a parallel system are introduced as follows. Fig. 1-20 shows the space vector diagram of the single-rating inductor five-level CSI, which includes 19 vectors divided into four types by length: large vectors (I_{L1} to I_{L6}), medium vectors (I_{M1} to I_{M6}), small vectors (I_{S1} to I_{S6}), and zero vector (I_0). The inverter-side voltages, as analyzed in the DC-link equivalent circuit, affects the balance of DC currents [42]. The reference current is typically synthesized using three adjacent vectors. To select the appropriate vectors, the nearest three adjacent vectors form the reference vector, considering the triangle where the reference is located. The dwell time for each vector is calculated using the following equation:

$$\begin{cases} T_s = T_1 + T_2 + T_3 \\ I_{ref} = I_x T_1 + I_y T_2 + I_z T_3 \end{cases} \tag{1-3}$$

where I_x, I_y, and I_z are the three adjacent vectors forming the reference vector; T_1, T_2, and T_3 are their dwell times, and T_s is the sampling period.

Assuming the reference vector is located in subsector 4 of sector 1, as shown in Fig. 1-20, the three adjacent vectors I_{M1}, I_{S1}, and I_{S6} are selected to synthesize the reference vector. For the switching state {16;12}, V_1 to V_4 correspond to phase voltages V_a, V_b, V_a, and V_c, respectively. Based on (1-2), Δi_p remains unchanged, while Δi_n can be adjusted based on the values of V_b and V_c. If $V_b > V_c$, Δi_n increases; If $V_b < V_c$, Δi_n decreases.

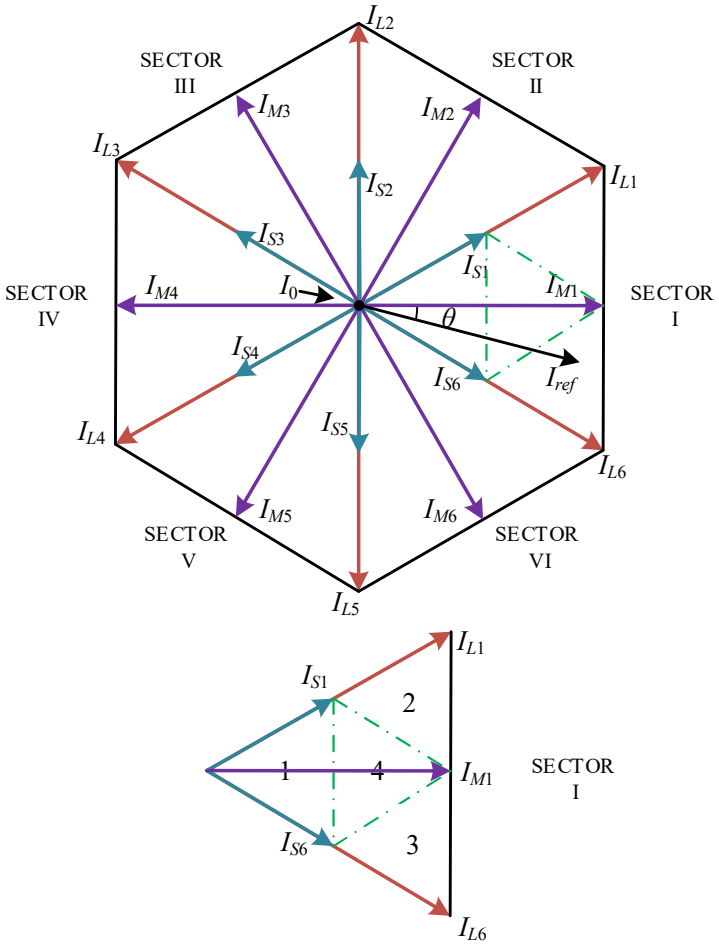


Fig. 1-20 Space vector diagram of the single-rating inductor five-level CSI.

A similar analysis can derive the DC current influence caused by other switching states, as listed in Table 1-2 (Sector I). In this table, "X" indicates no influence, "↓" indicates a decrease in DC current, and "↑" indicates an increase in DC current. The analysis shows that large vectors do not influence DC current because the turn-on devices of each CSI are the same, meaning the inverter-side DC-link voltage of each CSI remains

constant under these switching states [43]. This conclusion also applies to some zero vectors with identical switching states for each CSI. Other switching states, which result in different inverter-side DC-link voltages, can change the DC currents resulting in the DC current imbalance [44]. Even worse, in practice where component mismatches and variations in the gating signal time delays occur, the current imbalance will cause even greater damage to the inverter performance [45].

Table 1-2 DC Current variation for different switching states (Sector I)

Space vectors		On-state switches	DC current influence
Large vectors	I_{L1}	{12;12}	ΔI_p X; ΔI_n X
	I_{L6}	{61;61}	ΔI_p X; ΔI_n X
Medium vectors	I_{M1}	{12;61}	ΔI_n X; If $V_{bc} > 0$, $\Delta I_p \uparrow$
		{61;12}	ΔI_p X; If $V_{bc} > 0$, $\Delta I_n \uparrow$
Small vectors	I_{S1}	{12;14}	ΔI_p X; If $V_{bc} > 0$, $\Delta I_n \downarrow$
		{14;12}	ΔI_n X; If $V_{bc} > 0$, $\Delta I_p \downarrow$
		{12;25}	ΔI_p X; If $V_{bc} > 0$, $\Delta I_n \downarrow$
		{25;12}	ΔI_n X; If $V_{bc} > 0$, $\Delta I_p \downarrow$
		{61;23}	If $V_{bc} > 0$, $\Delta I_n \uparrow$; If $V_{ab} > 0$, $\Delta I_p \downarrow$
		{23;61}	If $V_{bc} > 0$, $\Delta I_p \uparrow$; If $V_{ab} > 0$, $\Delta I_n \downarrow$
	I_{S6}	{61;14}	ΔI_p X; If $V_{ab} > 0$, $\Delta I_n \downarrow$
		{14;61}	ΔI_n X; If $V_{ab} > 0$, $\Delta I_p \downarrow$
		{61;36}	ΔI_n X; If $V_{ab} > 0$, $\Delta I_p \downarrow$
		{36;61}	ΔI_p X; If $V_{ab} > 0$, $\Delta I_n \downarrow$
		{56;12}	If $V_{ca} > 0$, $\Delta I_n \uparrow$; If $V_{bc} > 0$, $\Delta I_p \downarrow$
		{12;56}	If $V_{ca} > 0$, $\Delta I_p \uparrow$; If $V_{bc} > 0$, $\Delta I_n \downarrow$
Zero Vectors	I_0	{14;14}{36;36}{25;25}	ΔI_p X; ΔI_n X
		{14;36}{36;25}{25;14}	If $V_{ab}/V_{bc}/V_{ca} > 0$, $\Delta I_p \downarrow$; $\Delta I_n \downarrow$
		{61;34}{23;56}{12;45}	If $V_{ab}/V_{bc}/V_{ca} > 0$, $\Delta I_p \downarrow$; $\Delta I_n \uparrow$

1.3.2 Solutions of current imbalance

To balance the DC currents, various methods have been proposed, which can be broadly categorized into open-loop and closed-loop strategies:

Open-loop strategy:

The open-loop strategy is the carrier-swapping technique applied to the phase-shifted SPWM controller [46]. This technique aims to equalize the DC current share of the modules in a single-rating inductor five-level CSI. The phase-shifted triangle carriers of the modules are swapped one at a time at each positive edge of the synchronous signal. For instance, the modified triangle carrier signal of module 1 is alternated between the original carriers 1 and 2. This helps to reduce current imbalance caused by unequal states [47]. However, this method has limited accuracy, impacts the final harmonic performance, and cannot effectively address current imbalances due to component mismatches and variations in the gating signal time delays.

Closed-loop strategy:

For the closed-loop strategies, the common method for current balancing involves sampling the DC inductor currents by additional current sensors and using these sampled currents to redistribute the switching states (zero states and active states) in the modulation schemes, as shown in Fig. 1-21. In [48], a modified SPWM technique is proposed to balance the DC current by utilizing the redundant switching states of a multi-rating inductor five-level CSI. Similarly, some techniques achieve vector-based inductor current balancing by employing zero vectors [49] or redundant small vectors [50] in SVM for the existing five-level CSI topologies. However, zero current vectors and certain small vectors are not recommended, as they introduce a bypass operation by simultaneously turning on two devices in the same inverter leg. This results in increased switching frequency and reduced DC utilization. Other SVM-based techniques achieve vector-based inductor current balancing by adjusting different medium [51] or large vectors [52]. This approach eliminates the drawbacks of using zero or small vectors and addresses the imbalance caused by unequal state voltages, component mismatches, and variations in the gating signal time delays to a significant extent. Nevertheless, these

closed-loop current balancing methods still face challenges: 1) Increased switching frequency due to the adjustment of switching states; 2) Heavy computation required by the numerous switching combinations; 3) Increased costs associated with the use of additional current sensors.

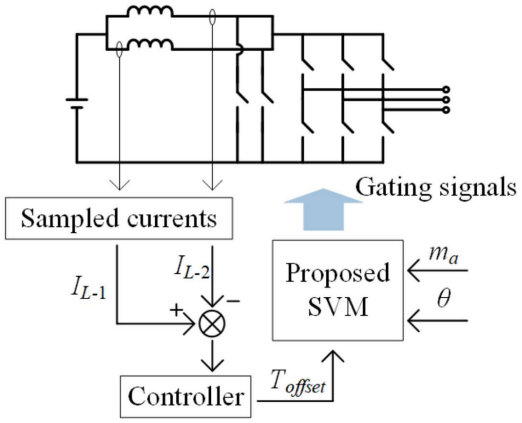


Fig. 1-21 Closed-loop control strategy for eight-switch five-level CSI [34].

1.3.3 Summary and objective

In summary, current imbalance is an unavoidable issue in existing five-level CSI topologies. It arises from unequal state voltages of switching devices, manufacturing tolerances of components, and variations in the time delay of gating signals, leading to degraded AC output quality and overcurrent problems. The recommended solution involves closed-loop control, which uses additional current sensors to sample the DC inductor currents and redistribute the switching states based on these samples. However, even with the optimal approach in literature, such drawbacks remain: 1) increased switching frequency, 2) heavy computational demands, and 3) higher costs.

Therefore, the objective of this work is to design new five-level CSI topologies with self-balancing inductor currents, eliminating the need for additional balance control.

Additionally, the design will consider inverter performance factors such as harmonic performance, overvoltage clamping, and the size of DC inductors, etc.

Following the literature review and objective analysis in Chapter 1, this work introduces three innovative five-level CSIs that solving the current imbalance of the existing topologies.

X-type Five-Level CSI: Introduced in Chapter 2, this topology is the first to feature current self-balancing, eliminating the need for complex balancing control schemes. However, at high modulation indexes where the X-type CSI excels in harmonic performance, it requires larger DC inductors, leading to higher costs, increased volume, and reduced efficiency.

Γ-type Five-Level CSI: Introduced in Chapter 3, this topology also maintains current self-balancing. At high modulation indexes, both the X-type and Γ-type CSIs offer superior harmonic performance, but the Γ-type requires significantly smaller DC inductors, resulting in lower costs, reduced volume, and higher efficiency.

H-type Five-Level CSI: Introduced in Chapter 4, this topology aims to further minimize the size of DC inductors. While retaining the current self-balancing feature, the H-type CSI achieves the smallest DC inductance, leading to the lowest costs, smallest volume, and highest efficiency. Additionally, the voltage ratings of the DC switches are significantly reduced.

Chapter 2 X-Type Five-Level Current Source Inverter[1]

In the previous chapter, the existing five-level CSI topologies from the literature are introduced with the common issue of current imbalance identified. To address the issue, a novel X-type five-level CSI with a self-balancing feature is proposed in this chapter, eliminating the need for complex and costly balancing control schemes.

This chapter begins by reviewing the causes and consequences of current imbalance. It then presents the proposed X-type CSI, including a detailed introduction, analysis, and calculations related to its configuration, operating principle, self-balancing mechanism, modulation scheme, DC utilization, switch stress, passive component sizes, and overall efficiency. Finally, the performance of the proposed inverter is verified through both simulations and experiments.

2.1 Current imbalance

As discussed in the previous chapter, current imbalance is a significant issue for five-level CSIs. This imbalance occurs between the DC inductors in topologies using a voltage source with DC inductors, or during the generation of equal current sources in topologies with independent current sources. The primary cause of DC current imbalance is the unequal state voltages of switching devices. For example, in Fig. 2-1, when switches S_{13}, S_{14}, S_{22}, and S_{23} of the single-rating five-level CSI are on, the clamped line-to-line voltages for each six-switch CSI module differ, finally resulting in different inductor current changes for each module. Additionally, manufacturing tolerances of components (e.g., $L_1 \neq L_2$) and variations in the time delay of the gating signals of the parallel inverters can also contribute to current imbalance. Unbalanced DC current can degrade the quality of the AC output, increase harmonics, and necessitate larger filters. More critically, current imbalance may lead to overcurrent conditions, potentially damaging components. The mainstream solution for current imbalance involves closed-loop control, which uses additional current sensors to sample the DC inductor currents

and adjust the switching states accordingly. However, even with the best approaches in the literature, there are still drawbacks: 1) increased switching frequency, 2) heavy computational demands, and 3) higher costs.

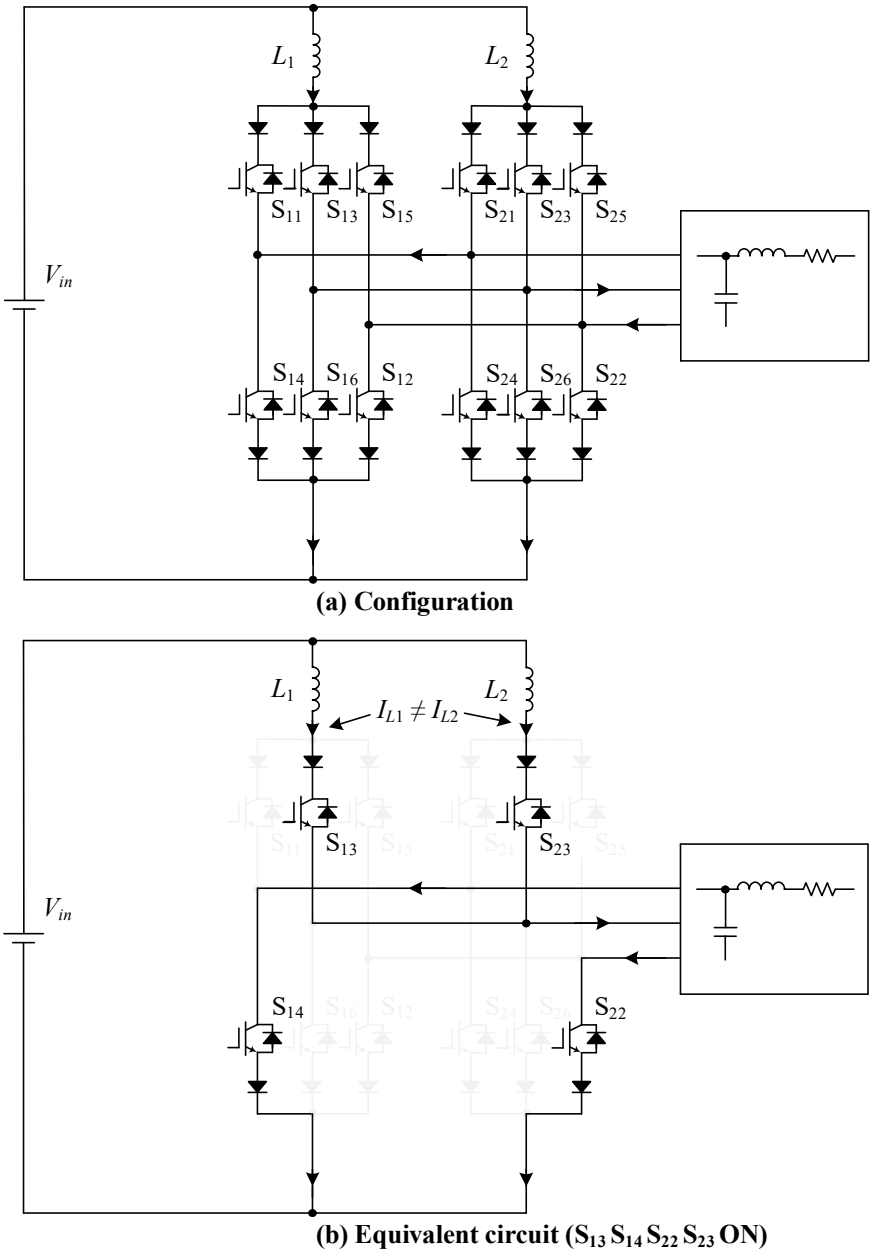


Fig. 2-1 Single-rating inductor five-level CSI.

2.2 X-type five-level current source inverter

To address the current imbalance without incorporating a complex and expensive balance control system, an innovative X-type five-level current source inverter is introduced in this section. This newly designed inverter capitalizes on the charging and discharging processes of the DC inductors, resulting in a self-balancing feature. This section provides a detailed introduction, analysis and calculations concerning the inverter structure, operation principle, self-balancing mechanism, modulation scheme, DC utilization, switch stress, size of passive components, and the efficiency of the proposed inverter.

2.2.1 Topology

Fig. 2-2 illustrates the topology of the proposed X-type five-level CSI.

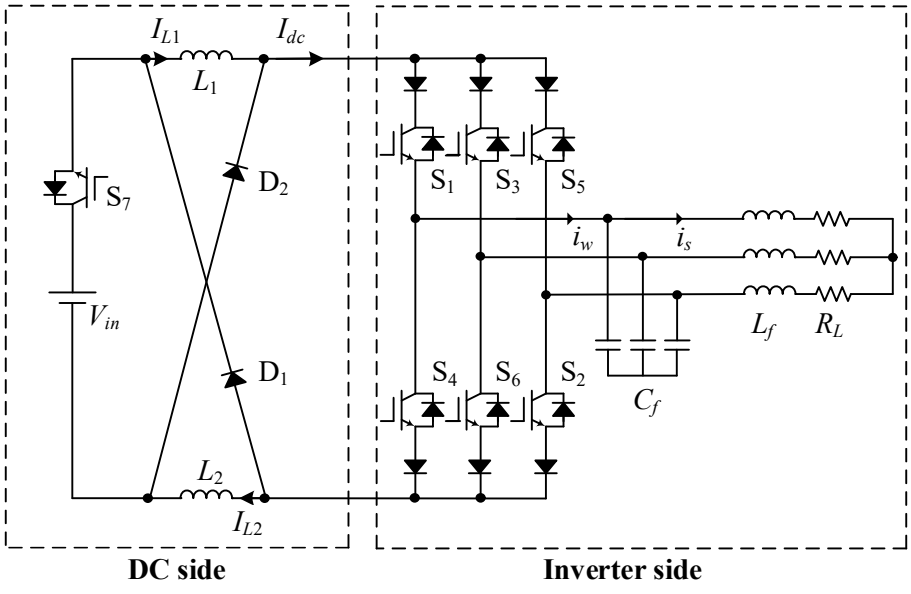


Fig 2-2 Proposed X-type five-level CSI.

On the inverter side, a single six-switch CSI is used, featuring the following components:

1) Switching devices: S_1 to S_6 are power switches with reverse voltage blocking capabilities, such as gate turn-Off thyristors (GTO), symmetrical gate commutated thyristors (SGCT), or insulated gate bipolar transistors (IGBT)/metal-oxide-semiconductor field-effect transistors (MOSFET) in series with a diode.

2) Three-phase capacitor: Located at the inverter output, this capacitor C_f aids in the commutation of the switching devices. For example, when switch S_1 is turned off, the inverter PWM current i_w drops to zero rapidly. The capacitor provides a path for the energy trapped in the phase-A load inductance, preventing high voltage spikes that could damage the switching devices.

3) LC filter: The combination of C_f and load inductance L_f together form an LC filter. This filter removes most of the harmonics from the PWM current i_w, ensuring the sinusoidal current i_s meets specific output requirements (e.g. the current harmonics distortion criteria for the design of electrical systems in IEEE 519-2014).

4) Inverter output: As an example, the output is connected to an AC motor in Fig. 2-2, represented by load inductance L_f and load resistance R_L. Additionally, the output can be connected with grid, with power factor control being required.

On the DC side, an DC-DC converter is used, featuring the following components:

1) Input source: The proposed inverter uses a single voltage source, akin to other topologies discussed in Section 1.2.1.

2) DC inductors: The inductors L_1 and L_2 make the DC current I_{dc} smooth and continuous, while also facilitates the inverter's operational principles (discussed detailly in the next section).

3) Additional components: S_7 can be an IGBT or MOSFET, and D_1 and D_2 are power diodes. These components are included to support the unique operations of the inverter.

2.2.2 Five-level output generation

Fig. 2-3 illustrates the two operation modes of the proposed inverter:

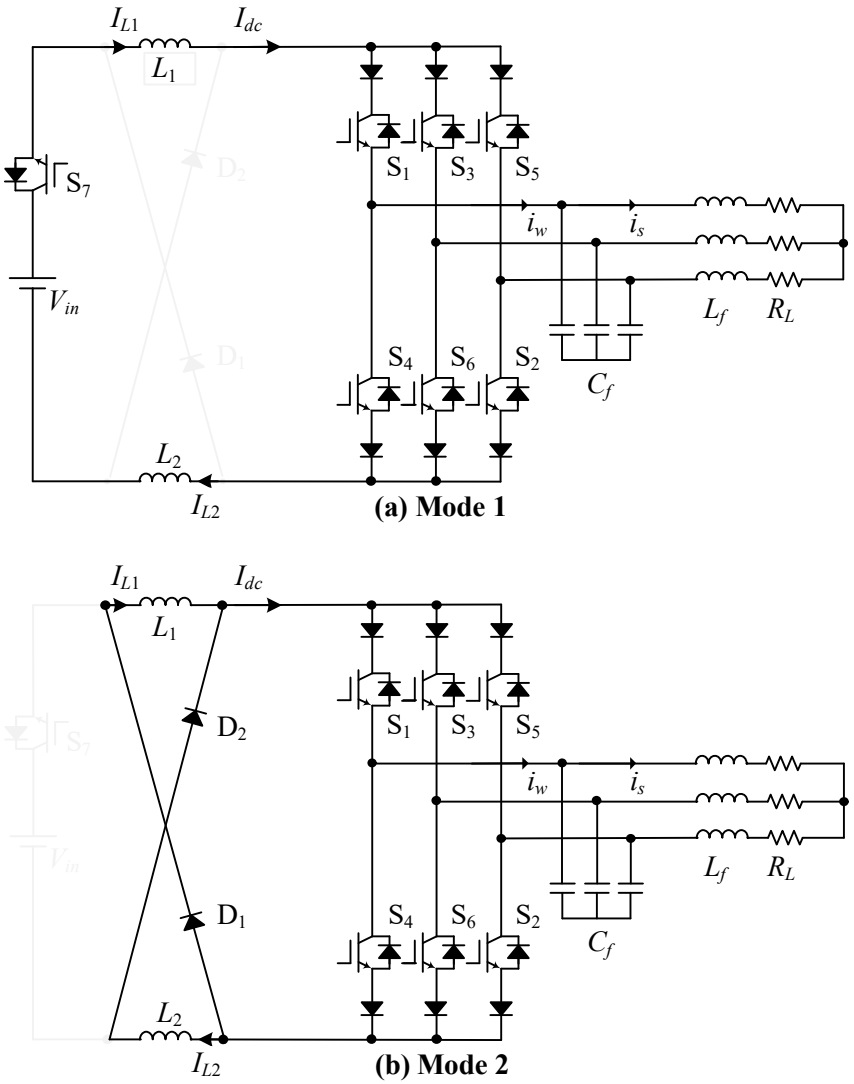


Fig. 2-3 Operation modes of the X-type five-level CSI.

Mode 1: Illustrated in Fig. 2-3 (a), S_7 is turned on, and DC inductors L_1 and L_2 are connected in series. The currents through both inductors I_{L1} and I_{L2}, as well as the DC current I_{dc}, are equal (I_{dc}=I_{L1}= I_{L2}=I_L). Therefore, the output PWM current has three levels, I_L, 0, and -I_L.

Mode 2: Illustrated in Fig. 2-3 (b), S_7 is turned off, and the input source V_{in} is disconnected. L_1 and L_2 are connected in parallel through D_1 and D_2, respectively. The two inductors now act as parallel-connected current sources. I_{dc} equals the combination of the two inductor currents ($I_{dc}=I_{L1}+I_{L2}=2I_L$). Hence, $2I_L$, 0, and $-2I_L$ are generated at the CSI output.

Five-level output currents can be obtained with the above two operation modes working alternatively ($\pm I_L$, 0, and $\pm 2I_L$). For example, when S_1, S_2, and S_7 are turned on, the three-phase output currents i_{wA}, i_{wB}, and i_{wC} are I_L, 0, and $-I_L$, respectively; when S_1 and S_2 are turned on, i_{wA}, i_{wB}, and i_{wC} are $2I_L$, 0, and $-2I_L$, respectively.

2.2.3 Modulation design

Switching states: According to the two operation modes of the proposed inverter shown in the last section, the switching states and corresponding output PWM currents are shown in Table 2-1. There are a total of 15 switching states, including active and zero switching states. Similar to existing CSIs, the modulation scheme for the proposed CSI is not unique. Any CSI modulation scheme can be designed as long as the switching states in Table 2-1 are satisfied. In this work, an space vector modulation (SVM)-based scheme is developed as an example for the proposed X-type five-level CSI.

Space vectors: The resultant space vectors for the switching states are shown in the space vector diagram in Fig. 2-4, where I_{L1} to I_{L6} are the large vectors, I_{S1} to I_{S6} are the small vectors, and I_0 is the zero vector. The large/small vectors form a hexagon with six equal sectors, while the zero vector lies at the center. Note that the transformation from switching states to space vectors is the same as the conventional CSIs, thus not repeated here, please refer to [1] for such details. To facilitate the dwell time calculation, the space vector diagram can be divided into six triangular sectors (I to VI), each of which can be further divided into five subsectors (1 to 5), as shown in Fig. 2-4. Eventually, there are 30 subsectors in total.

Table 2-1 Space vectors of the proposed inverter

Space vectors		On-state switches	Output currents		
			i_{wA}	i_{wB}	i_{wC}
Large vectors	I_{L1}	{12}	$2I_L$	0	$-2I_L$
	I_{L2}	{23}	0	$2I_L$	$-2I_L$
	I_{L3}	{34}	$-2I_L$	$2I_L$	0
	I_{L4}	{45}	$-2I_{dc}$	0	$2I_L$
	I_{L5}	{56}	0	$-2I_L$	$2I_L$
	I_{L6}	{61}	$2I_L$	$-2I_L$	0
Small vectors	I_{S1}	{127}	I_L	0	$-I_L$
	I_{S2}	{237}	0	I_L	$-I_L$
	I_{S3}	{347}	$-I_L$	I_L	0
	I_{S4}	{457}	$-I_L$	0	I_L
	I_{S5}	{567}	0	$-I_L$	I_L
	I_{S6}	{617}	I_L	$-I_L$	0
Zero vectors	I_0	{147}	0	0	0
		{257}			
		{367}			

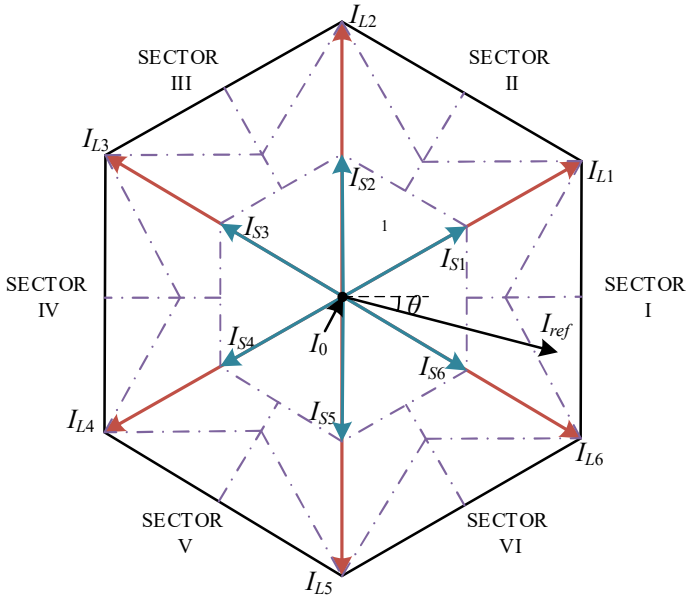


Fig. 2-4 Space vector diagrams of the proposed inverter.

Dwell time calculation: The reference vector I_{ref} is synthesized by three vectors. Depending on the different sectors and subsectors I_{ref} falls into, the synthesized scheme is listed below:

1) one zero vector and two small vectors in Subsector 1.

2) two small vectors and one large vector in Subsector 2 and 4.

3) one small vector and two large vectors in Subsector 3 and 5.

For example, with I_{ref} falling into Subsector 3 in Sector I, as shown in Fig. 2-5, it is synthesized by one small vector (I_{S6}) and two large vectors (I_{L6} and I_{L1}).

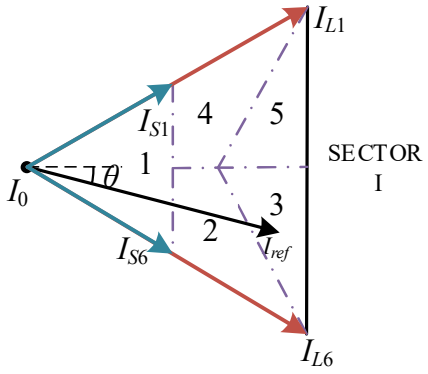


Fig. 2-5 Space vector diagrams in Sector 1.

By converting the three-phase (abc) current vectors into two-phase ($\alpha\beta$) based on the ampere-second balancing principle, the relationships between the vectors and dwell times can be derived:

$$\begin{cases} I_{ref}T_s = I_{ap}T_p + I_{aq}T_q + I_{ar}T_r \\ T_s = T_p + T_q + T_r \end{cases} \tag{2-1}$$

where the subscript a represents small (S), large (L), or zero (0) vectors; T_s the sampling period; T_p, T_q, and T_r represent the dwell times for the respective vectors.

Applying the example in Fig. 2-5 when I_{ref} falling into Subsector 3 in Sector I, equation (2-1) can be simplified as:

$$\begin{cases} I_{ref}T_s = I_{L1}T_4 + I_{S6}T_1 + I_{L6}T_2 \\ T_s = T_4 + T_1 + T_2 \end{cases} \tag{2-2}$$

Table 2-2 Vector Dwell Times of Different Subsectors

Subsector	Vector	Dwell time	Dwell time calculation
1	I_0	T_0	$T_s - T_1 - T_3$
	I_{S6}	T_1	$(\cos\theta - \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L6}	T_2	0
	I_{S1}	T_3	$(\cos\theta + \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L1}	T_4	0
2	I_0	T_0	0
	I_{S6}	T_1	$T_s - T_2 - T_3$
	I_{L6}	T_2	$(2 * \cos\theta * m_a - 1) * T_s$
	I_{S1}	T_3	$(\cos\theta + \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L1}	T_4	0
3	I_0	T_0	0
	I_{S6}	T_1	$T_s - T_2 - T_4$
	I_{L6}	T_2	$((1.5 * \cos\theta - 0.5 * \sqrt{3}\sin\theta) * m_a - 1) * T_s$
	I_{S1}	T_3	0
	I_{L1}	T_4	$0.5 * (\cos\theta + \sqrt{3}\sin\theta) * T_s * m_a$
4	I_0	T_0	0
	I_{S6}	T_1	$(\cos\theta - \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L6}	T_2	0
	I_{S1}	T_3	$T_s - T_1 - T_4$
	I_{L1}	T_4	$(2 * \cos\theta * m_a - 1) * T_s$
5	I_0	T_0	0
	I_{S6}	T_1	0
	I_{L6}	T_2	$0.5 * (\cos\theta - \sqrt{3}\sin\theta) * T_s * m_a$
	I_{S1}	T_3	$T_s - T_2 - T_4$
	I_{L1}	T_4	$((1.5 * \cos\theta + 0.5 * \sqrt{3}\sin\theta) * m_a - 1) * T_s$

Following the above procedure, each selected vector's dwell times under different subsectors and sectors can be calculated and summarized in Table 2-2, where m_a is the modulation index.

Table 2-3 Sequence design of the proposed inverter

	Sequence	Subsector 1	Subsector 2	Subsector 4	Subsector 1
$0.5 < m_a < 0.577$	SQ1	I_{S1}-I_0-I_{S6}	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{S1}-I_{L1}	I_{S1}-I_0-I_{S6}
	SQ2	I_{S1}-I_0-I_{S6}	I_{L6}-I_{S6}-I_{S1}	I_{L1}-I_{S1}-I_{S6}	I_{S1}-I_0-I_{S6}
	SQ3	I_{S1}-I_{S6}-I_0	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{S1}-I_{L1}	I_{S1}-I_{S6}-I_0
	SQ4	I_{S6}-I_{S1}-I_0	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{S1}-I_{L1}	I_{S6}-I_{S1}-I_0
	Sequence	Subsector 2	Subsector 3	Subsector 5	Subsector 4
$0.577 < m_a < 0.667$	SQ5	I_{L6}-I_{S6}-I_{S1}	N/A	N/A	I_{S6}-I_{S1}-I_{L1}
	SQ6	I_{L6}-I_{S6}-I_{S1}	N/A	N/A	I_{L1}-I_{S1}-I_{S6}
	SQ7	I_{S1}-I_{S6}-I_{L6}	N/A	N/A	I_{S6}-I_{S1}-I_{L1}
	SQ8	I_{S1}-I_{S6}-I_{L6}	N/A	N/A	I_{L1}-I_{S1}-I_{S6}
$m_a > 0.667$	SQ9	I_{L6}-I_{S6}-I_{S1}	I_{S6}-I_{L6}-I_{L1}	I_{L6}-I_{L1}-I_{S1}	I_{S6}-I_{S1}-I_{L1}
	SQ10	I_{L6}-I_{S6}-I_{S1}	I_{S6}-I_{L6}-I_{L1}	I_{S1}-I_{L1}-I_{L6}	I_{S6}-I_{S1}-I_{L1}
	SQ11	I_{L6}-I_{S6}-I_{S1}	I_{L1}-I_{L6}-I_{S6}	I_{L6}-I_{L1}-I_{S1}	I_{L1}-I_{S1}-I_{S6}
	SQ12	I_{L6}-I_{S6}-I_{S1}	I_{L1}-I_{L6}-I_{S6}	I_{S1}-I_{L1}-I_{L6}	I_{L1}-I_{S1}-I_{S6}
	SQ13	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{L6}-I_{L1}	I_{L6}-I_{L1}-I_{S1}	I_{S6}-I_{S1}-I_{L1}
	SQ14	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{L6}-I_{L1}	I_{S1}-I_{L1}-I_{L6}	I_{S6}-I_{S1}-I_{L1}
	SQ15	I_{S1}-I_{S6}-I_{L6}	I_{L1}-I_{L6}-I_{S6}	I_{L6}-I_{L1}-I_{S1}	I_{L1}-I_{S1}-I_{S6}
	SQ16	I_{S1}-I_{S6}-I_{L6}	I_{L1}-I_{L6}-I_{S6}	I_{S1}-I_{L1}-I_{L6}	I_{L1}-I_{S1}-I_{S6}

Sequence sequences*:* Similar to the space vector modulation for the conventional CSI, the switching sequence design for the X-type CSI should also satisfy the following two requirements for the minimization of switching frequencies [1]:

1) The transition from one switching state to the next involves only two switches, one being switches on and one being switches off.

2) The transition for I_{ref} moving from one sector/subsector to the next requires the minimum number of switchings.

In the X-type five-level CSI, varying m_a values result in I_{ref} traversing different subsectors, as illustrated in Fig. 2. The scenarios are as follows (in respective sector): **Case 1**: for $m_a <$ 0.5, I_{ref} stays in Subsector 1; **Case 2**: for $0.5 < m_a < 0.577$, I_{ref} follows the path: Subsector 1 - Subsector 2 - Subsector 4 - Subsector 1; **Case 3**: for $0.577 < m_a < 0.667$, I_{ref} follows the path: Subsector 2 - Subsector 4; **Case 4**: for $0.667 < m_a < 1$, I_{ref} follows the path: Subsector 2 - Subsector 3 - Subsector 5 - Subsector 4.

When $m_a < 0.5$ (case 1), the X-type functions as a three-level CSI, therefore, this case will not be discussed. In the design, m_a should always be larger than 0.5. Table 2-3 presents the switching sequences meeting the specified design criteria (mentioned above) in case 2, case 3, and case 4.

2.2.4 Self-balancing mechanism

Unlike other five-level CSI topologies requiring extra control schemes for the unbalanced inductor currents, the inductor currents of the proposed inverter have a self-balancing feature. Fig. 2-6 shows the simulated waveforms of inductor currents (i_{L1} and i_{L2}) and inductor voltages (V_{L1} and V_{L2}). Noted that the inductors are set differently (L_1 = 20 mH and L_2 = 10 mH) to simulate the inductor mismatch.

As shown in Fig. 2-6, each switching period is divided into the following four parts:

1) t_0 - t_1: At time t_0, S_7 is switched off, and the inverter starts operating in mode 2 (input source V_{in} disconnected), where the two inductors are connected in parallel and act as parallel-connected current sources. Between time t_0 and t_1, since both inductors are connected in parallel, the voltages across the two inductors are the same ($V_{L1} = V_{L2} = V_{dc}$). In addition, they are clamped by the filter capacitor voltage ($V_{L1} = V_{L2} = V_c$) of the CSI (please refer to [1] for details of CSI operations). Since the unequal state voltages, inductor currents i_{L1} and i_{L2} are decreasing at different rates, resulting in unbalanced instantaneous inductor currents ($i_{L1} \neq i_{L2}$) as shown in Fig. 2-6. The corresponding equivalent circuit under this time interval is shown in Fig. 2-7 (a).

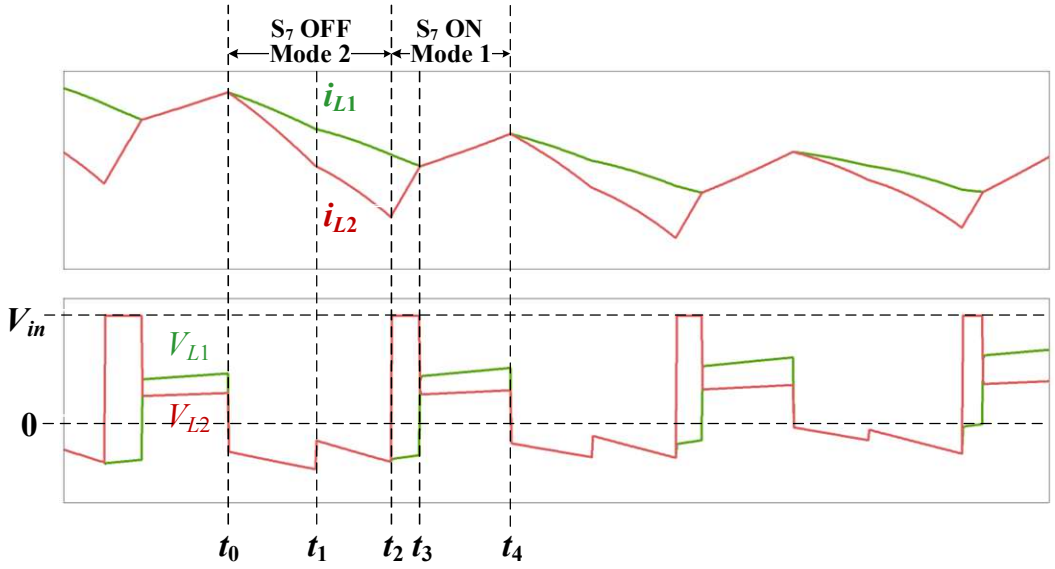


Fig. 2-6 Transient waveforms of the proposed inverter.

2) t_1 - t_2: At time t_1, there is a change in the switching states of the CSI, resulting in a change in the DC-link voltage V_{dc}. The resultant inductor voltages V_{L1} and V_{L2} change accordingly, as shown in Fig. 2-6. Between time t_1 and t_2, the inverter still operates in mode 2, where the inductor currents i_{L1} and i_{L2} continue to decrease at different rates until time t_2 (the end of mode 2), at which the difference between i_{L1} and i_{L2} reaches the maximum as shown in Fig. 2-6. The corresponding equivalent circuit under this time interval is shown in Fig. 2-7 (b).

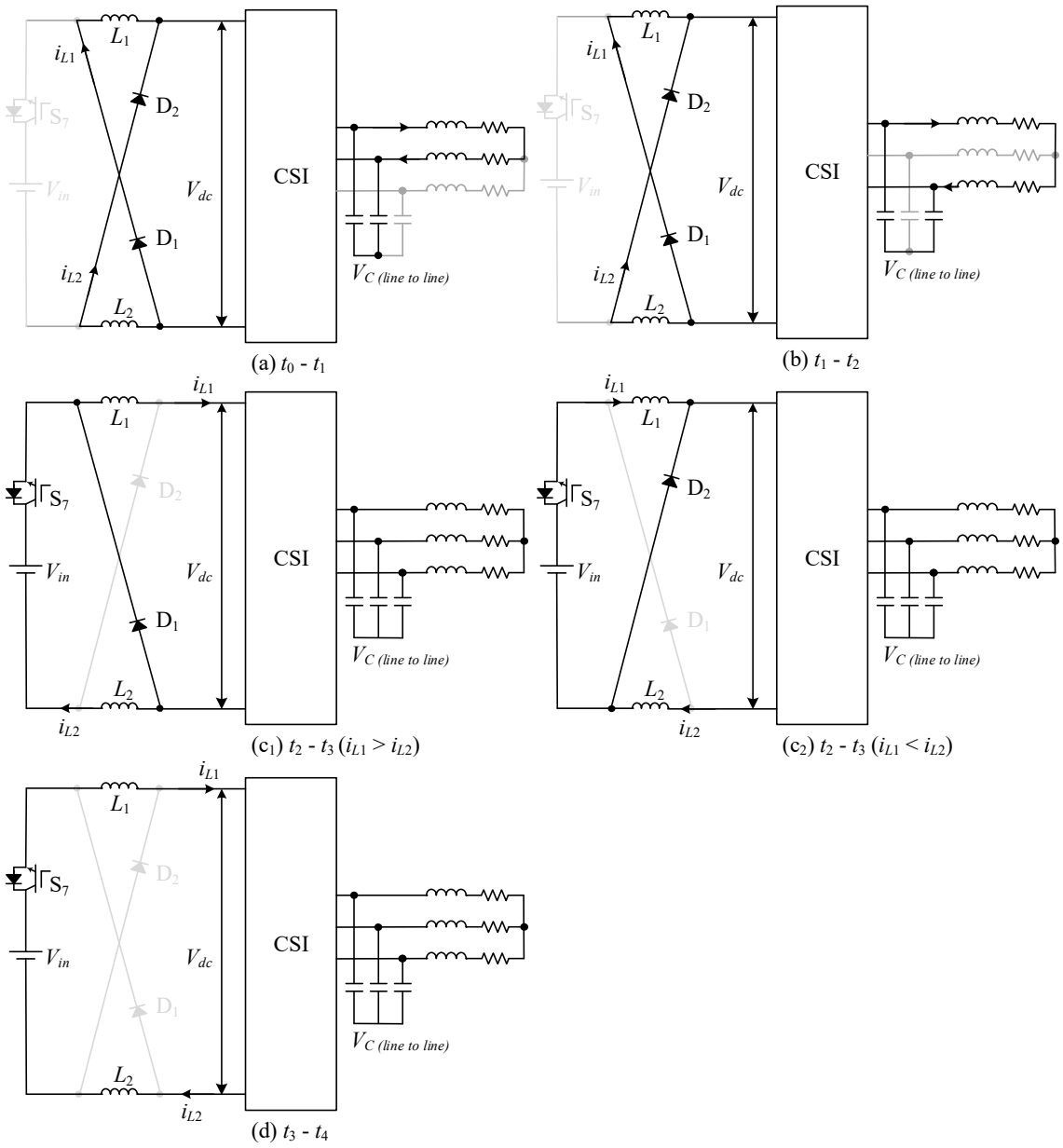


Fig. 2-7 Transient states of the proposed inverter.

3) t_2 - t_3: At time t_2, S_7 is switched on, and the two inductors start to be connected in series, forcing the inductor currents i_{L1} and i_{L2} to be the same as shown in Fig. 2-6. In this process, the inductor voltages suffer an overvoltage due to $i_{L1} \neq i_{L2}$. However, as shown in Fig. 2-6, this overvoltage is clamped by the input voltage V_{in}. This is because once the inductor voltage, V_{L2}, for example, reaches V_{in}, the diode D_1 will then be forward-biased and turned on. As a result, V_{L2} will be clamped at V_{in}. The corresponding equivalent

circuit is shown in Fig. 2-7 (c_1). The same applies when the overvoltage occurs at V_{L1}, and the corresponding equivalent circuit is shown in Fig. 2-7 (c_2).

4) t_3 - t_4: At time t_3, i_{L1} and i_{L2} become identical, D_1 is then inactive. Between t_3 and t_4, S_7 remains turned on, L_1 and L_2 are connected in series, and the inverter operates in mode 1. Inductor currents i_{L1} and i_{L2} are self-balanced and keep identical. V_{L1} and V_{L2} are different due to the introduced inductor mismatch. The corresponding equivalent circuit under this time interval is shown in Fig. 2-7 (d).

5) At time t_4, S_7 is switched off again, and the cycle from 1) is repeated.

In summary, the X-type CSI has an imbalance inductor currents in mode 2 just like other five-level topologies. However, the inductor currents of the proposed inverter have a self-balanced capability due to the series-connection of DC inductors in mode 1, eliminating the needs for extra balancing schemes. Besides, the proposed inverter benefits from the inherent overvoltage clamping feature, neither extra overvoltage clamping schemes nor overrated devices are needed.

2.2.5 DC utilization

To derive the proposed converter's DC utilization, the analysis is divided into the dc side and the inverter side.

Fig. 2-8 illustrates the simplified DC side circuits. During Mode 1, switch S_7 is turned on, the currents through both inductors I_{L1} and I_{L2}, as well as the DC current I_{dc}, are equal (I_{dc}=I_{L1}= I_{L2}=I_L). During Mode 2, S_7 is turned off, I_{dc} equals the combination of the two inductor currents (I_{dc}=I_{L1}+I_{L2}=2I_L). The input voltage V_{in} and dc voltage V_{dc} are related by applying the voltage-second principle to the DC inductor:

$$\frac{V_{in}-V_{dc}}{2}D=V_{dc}(1-D) \tag{2-3}$$

where D is the duty cycle of S_7.

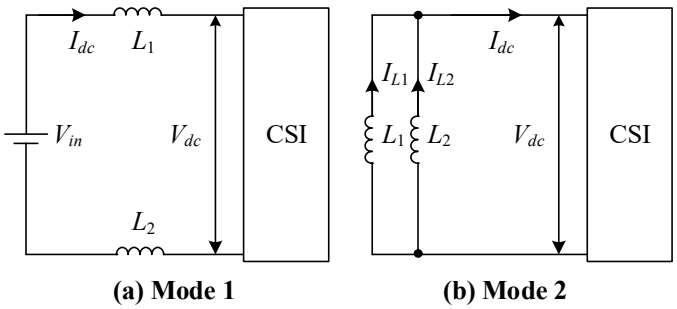


Fig. 2-8 Simplified DC side circuits in Mode 1 and 2.

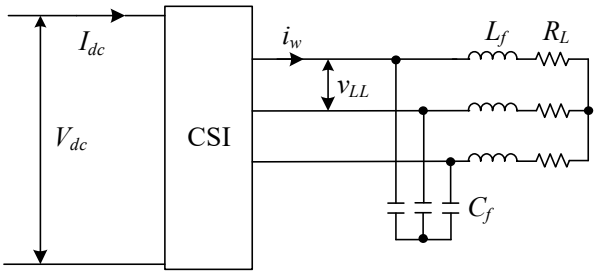


Fig. 2-9 Simplified inverter side circuit.

Fig. 2-9 illustrates the simplified inverter side circuit. Neglecting the power losses of the inverter, the input power should be equal to the output power of the CSI:

$$V_{dc} I_{dc\_avg} = \sqrt{3} V_{LL} I_{w1} \cos\varphi \tag{2-4}$$

where V_{LL} is the line-to-line voltage at the inverter output, I_{w1} is the RMS value of the fundamental component of i_w, φ is the power factor angle, and I_{dc_avg} is the average input current of the CSI and is expressed as:

$$I_{dc\_avg} = I_L D + 2I_L(1-D) \tag{2-5}$$

where the first term on the right is the current result from Mode 1 and the second term from Mode 2.

Since the inverter side of X-type CSI is the same as conventional 3-level CSI, the inverter side current gain of the proposed one is also the same as that of conventional CSI, as shown in (2-6), where m_a is the modulation index:

$$G_i = \frac{\sqrt{2}I_{w1}}{I_{dc}} = m_a \tag{2-6}$$

Using the designed SVM-based scheme, the relationships between duty cycle D and modulation index m_a can be expressed as (2-7):

$$D = 2 - \frac{6m_a}{\pi} \tag{2-7}$$

Combining (2-3), (2-4), (2-5), (2-6), and (2-7) gives the voltage gain, that is:

$$G_v = \frac{V_{LL}}{V_{in}} = \frac{2 - \frac{6m_a}{\pi}}{\sqrt{6}m_a \cos\varphi} \tag{2-8}$$

Fig. 2-10 illustrates the voltage gain of the proposed inverter. The voltage gain decreases with m_a increasing.

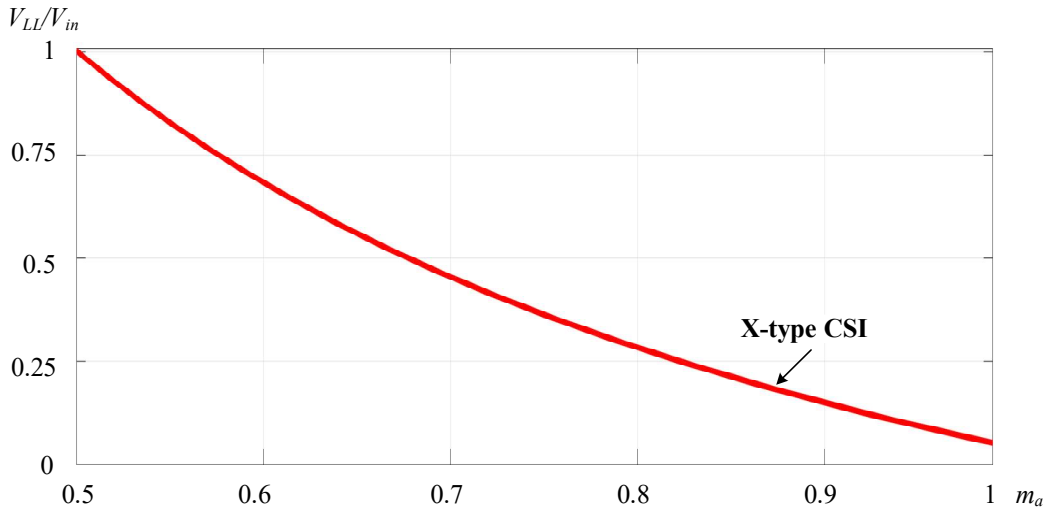


Fig. 2-10 Voltage gain of the proposed inverter.

In order to insure the five-level output, the working range of the X-type CSI is $0.5<m_a<1$. Within this working range, the proposed inverter is a voltage buck converter, the higher voltage gain is acquired at low modulation indexes and the maximum gain is around 1 when m_a=0.5.

2.2.6 Passive component sizes

The size of the passive components significantly impacts the cost and volume of the CSI system. This section addresses this aspect by examining the sizes of the DC inductor and the LC filter:

DC inductor size:

L_1 and L_2, the DC inductors in the proposed inverter, are the key components maintaining the operation modes of the proposed converter. At the same time, the size of the DC inductors also determines DC current ripple. For keeping the DC current ripple less than a certain value (12%, for example) to maintain the continuity and smoothness of the DC current, the minimum value of the DC inductors is shown in (2-9):

$$L_1 = L_2 = \frac{L_{total}}{2} = \frac{1}{2} * \frac{(V_{in} - V_{dc})\Delta t}{12\% I_L} \tag{2-9}$$

where Δt is the dwell times shown in Table 2-2. The relationships between V_{in} and V_{dc} can be derived in (2-3).

Through the relationship between load terminal current and voltage, the relationship between DC current I_{dc} and PWM current I_w in (2-6), and the voltage gain in (2-7), the expression of I_{dc} can be given by (2-10). It can be found that I_{dc} is related to load resistance R, modulation index m_a, and input voltage V_{in}.

$$I_{dc} = \frac{V_{LL}\cos\varphi}{\sqrt{6}m_a R} = \frac{(2-\frac{6m_a}{\pi})V_{in}}{6m_a^2 R} \tag{2-10}$$

Submitting equations (2-3), (2-8), and (2-10) into (2-9), the input inductance can be expressed as (2-11):

$$L_1 = L_2 = \frac{(2-\frac{\pi}{3m_a})V_{in}\Delta t}{2*12\%I_{dc}} = \frac{3m_a^2 R(2-\frac{\pi}{3m_a})\Delta t}{12\%(2-\frac{\pi}{6m_a})} \tag{2-11}$$

where Δt is the dwell times shown in Table 2-2, it can be seen that V_{in} in the numerator cancels out the V_{in} contained in I_L in the denominator. Therefore, the magnitude of L_{dc} has nothing to do with V_{in}. When the load resistance R is fixed, the size of the DC inductors is only related to the modulation index m_a.

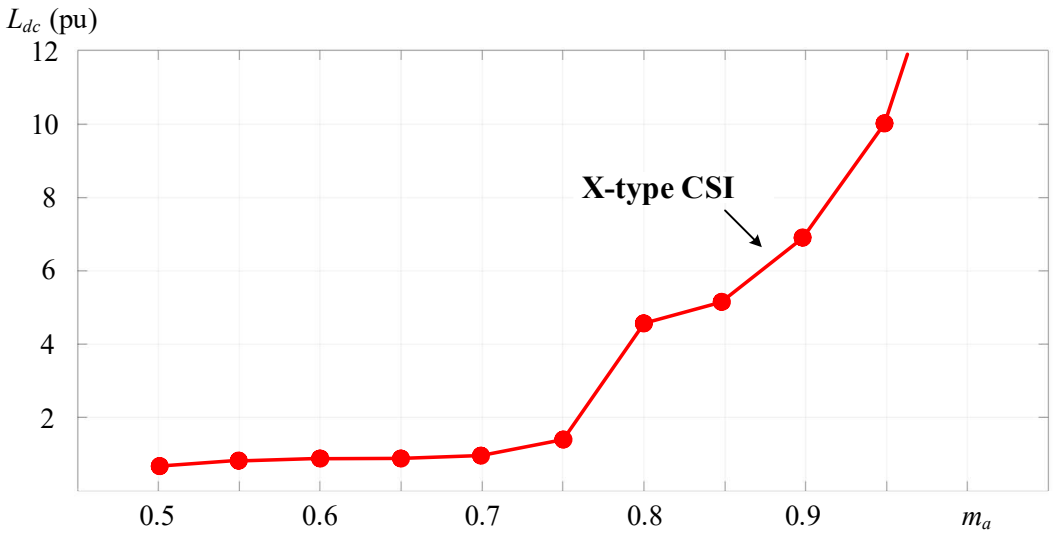


Fig. 2-11 Required input inductance at different modulation index.

In order to investigate the optimal operating range of the proposed inverter, the required L_{dc} at different m_a is calculated and verified by simulation. The data are shown in Fig. 2-11. When m_a = 0.5, the required inductance is around 0.6 pu, just like the conventional five-level CSIs; when $m_a < 0.7$, L_{dc} is less than 1.0 pu; when $m_a > 0.8$, L_{dc} is

larger than 4 and increases with m_a. Therefore, regarding the reduction of the DC inductance, the proposed inverter is suggested to operate in the m_a range of 0.5-0.7, requiring about 1.0 pu L_{dc}.

LC filter size:

The size of the LC filter is determined by the harmonic performance of i_w, and the transfer function of the filter can be shown as follows:

$$\frac{i_s(j\omega)}{i_w(j\omega)} = \frac{1}{(j\omega)^2 L_f C_f + (j\omega) R_f C_f + 1} \tag{2-12}$$

where R_f is the line resistance, i_s is the sinusoidal current after the filter, L_f is the line inductance, C_f is the filter capacitor, and w is the angular frequency.

The grid codes have requirements on both total harmonic distortion (THD) and individual harmonics of the grid-connected current. Therefore, the output filter should be sized so that all harmonics meet the grid codes (IEEE 519-2014) [53]. It is usually stipulated that the THD of i_s should be at most 5% for motor loads. Note that the LC filter design is a well-discussed topic [54], thus not detailed here.

Table 2-4 Minimum Filter Capacitor for the Proposed Converter

R=0.1 pu, L=0.1 pu									
m_a	0.55	0.6	0.65	0.7	0.75	0.8	0.85	0.9	0.95
i_w THD (%)	60.2	62.1	60.6	61.6	61.3	59.8	58.7	57.3	55.3
i_s THD (%)	5	5	5	5	5	5	5	5	5
C_{min} (pu)	0.233	0.243	0.236	0.239	0.238	0.232	0.228	0.223	0.215

In order to investigate the optimal operating range of the proposed inverter, the required C_f at different m_a is acquired, as shown in Table 2-4. With R_L and L_f both set to 0.1 pu, the required C_f is in the range of 0.215-0.243 pu. The required C_f decreases with

m_a increasing, therefore the proposed inverter is suggested to be operated at high m_a ranges regarding the reduction of C_f.

In summary, the study of passive component sizes reveals differing trends for DC inductors and LC filters. As the modulation index increases, the size of the required LC filter for the proposed inverter decreases, while the size of the DC inductor increases. This complicates the determination of the inverter's operating range.

2.2.7 Switch voltage stresses

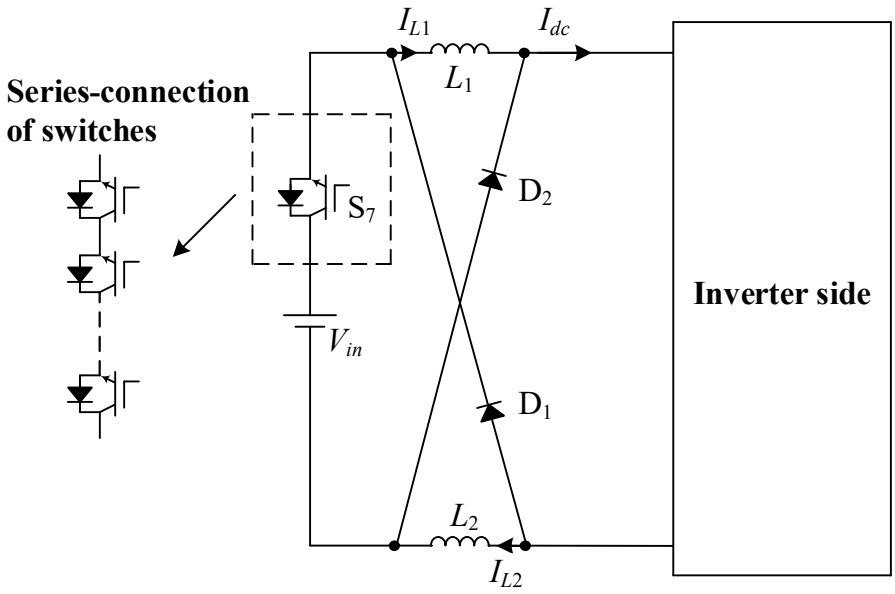


Fig. 2-12 Series-connection of switches for S_7.

Section 2.2.5 investigates the DC utilization of the proposed inverter and reveals that the X-type CSI functions as a voltage buck converter, with the voltage gain decreasing as the modulation index m_a increases. This characteristic also influences the voltage stress on the inverter side switches (S_1-S_6). Additionally, due to the unique design of the operation modes, the switching of the DC side switch S_7 determines whether the input source is connected, resulting in the voltage stress on S_7 being equal to the sum of the voltage stress on an inverter side switch (such as S_1) and the input voltage V_{in}. This is a

drawback, as the voltage stress on S_7 will be significantly higher than that on S_1-S_6. Therefore, in practical applications, S_7 should be constructed by connecting multiple switches in series, as shown in Fig. 2-12.

Table 2-5 Voltage stresses of the switches

	V_{in} (pu)	Maximum voltage stress (pu)		Stress ratio S_7/S_1
		S_1-S_6	S_7	
m_a= 0.5	1	0.998	1.998	2.002
m_a = 0.6	1	0.846	1.846	2.182
m_a = 0.7	1	0.546	1.546	2.832
m_a = 0.8	1	0.316	1.316	4.165
m_a = 0.9	1	0.183	1.183	6.464
m_a = 1.0	1	0.067	1.067	15.925

Table 2-5 lists the voltage stresses on the inverter side switches S_1-S_6, the voltage stress on the DC side switch S_7, and the stress ratio (indicating the number of switches needed in series for S_7). It is evident that the stress ratio increases with higher m_a. Even at low m_a values (0.5-0.7), the stress ratio of S_7 compared to S_1 is 2-3 times, necessitating three switches in series for S_7, and even more switches at higher m_a. This increases the number of switches in the proposed inverter, consequently raising the cost of the system.

2.2.8 Efficiency

The losses in the proposed converter primarily arise from semiconductor devices and inductors. The efficiency study methodology is based on varying the DC inductor (L_{dc}) at different modulation indexes (m_a). This approach aims to identify the inverter's optimal operating point rather than to display the efficiency profile using the same L_{dc} across the entire operating range (different m_a).

The semiconductor losses, encompassing losses from IGBTs and diodes in the proposed converter, fall into conduction losses, switching losses, and off-state losses. The off-state losses can be disregarded due to the negligibly small leakage current during the device's off-state [55]. Consequently, only conduction losses and switching losses are considered in this section.

For conduction losses, the formulas are outlined in (2-13), where V_{CE0} denotes the IGBT on-state zero-current collector-emitter voltage, V_{F0} is the diode zero-current forward on-state voltage, R_C represents the collector-emitter on-state resistance, R_D is the diode on-state resistance, and I_{C_AVG}/I_{C_RMS} stands for the average/RMS value of the conduction current.

As for switching losses, the formulas are provided in (2-14), where E_{on} and E_{off} denote the turn-on and turn-off energy losses per pulse of the IGBT, f_{sw} is the switching frequency, V_{nom} and I_{nom} are the rated voltage and current of the IGBT, V and I represent the instantaneous values during switching, E_{rr} is the turn-off energy losses of the diode, f_{D_off} is the diode turn-off frequency, V_b is the reverse blocking voltage, and V_{b_nom} is the rated reverse blocking voltage.

$$\begin{cases} P_{con\_IGBT} = V_{CE0} * I_{C\_AVG} + R_C * I_{C\_RMS}^2 \\ P_{con\_Diode} = V_{F0} * I_{C\_AVG} + R_D * I_{C\_RMS}^2 \end{cases} \tag{2-13}$$

$$\begin{cases} P_{sw\_IGBT} = (E_{on} + E_{off}) * f_{sw} * \dfrac{V}{V_{nom}} * \dfrac{I}{I_{nom}} \\ P_{sw\_diode} = E_{rr} * f_{D\_off} * \dfrac{V_b}{V_{nom}} \end{cases} \tag{2-14}$$

Inductive losses encompass AC winding losses, DC winding losses, and core losses. The primary factors influencing inductive losses include winding diameter and length, average inductor current, fundamental frequency, and the type of inductor material [56-57]. In circuits related to CSC, where the mandatory DC inductor is typically substantial, DC winding losses often constitute the predominant portion of inductor losses. These

losses are contingent on the inductor current and the DC resistance of the inductor (DCR). A larger L_{dc} results in a greater DCR, thereby leading to increased DC winding losses. In the proposed inverter and the preceding X-type CSI, both requiring a considerably larger L_{dc} than usual at certain modulation indexes, DC winding losses become even more crucial.

In general, power losses are influenced by both DC and AC inductors, the modulation scheme, switching frequency, conduction current, voltage stress on the switch, and switch characteristics, including saturation voltage, turn-on energy losses, and turn-off energy losses.

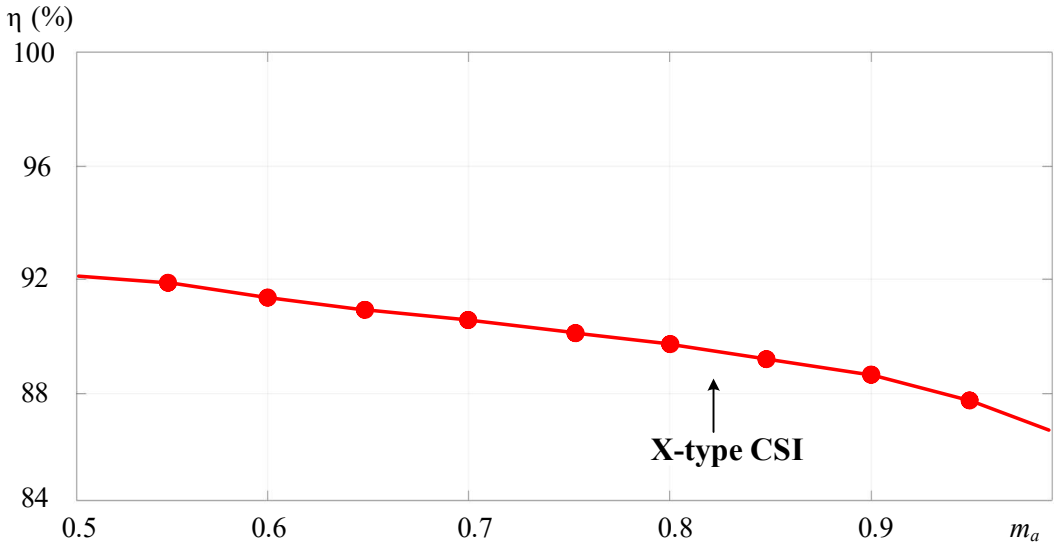


Fig. 2-13 Efficiency profile of the proposed inverter.

In order to investigate the best working range for the proposed inverter regarding the efficiency, the efficiency data is calculated and verified through PSIM. Fig. 2-13 shows the efficiency profiles of the proposed X-type CSI, maintaining an input voltage set at 3000 V. Power switches FZ250R65KE3 and power diodes DD250S65K3 are employed with the switching frequency of 4320Hz. The modulation index m_a spans from 0.5 to 1. The proposed inverter has a maximum efficiency of 92% at m_a = 0.5, and continuously drops as m_a increasing. Compared with conventional CSIs that experience current imbalance issues, the proposed X-type CSI has a lower efficiency, mainly due to the

larger L_{dc} resulting in increased inductive losses. For example, the parallel H-bridge five-level CSI has an efficiency of around 98.5% under a switching frequency of 540 Hz [1]. The calculated efficiency of this inverter under 4320 Hz is around 93.3%, where the DC inductor contributes 2%, the conduction loss contributes 1% and the switching loss contributes 3.7%. The method used for efficiency calculation is a well-used one in industry [58].

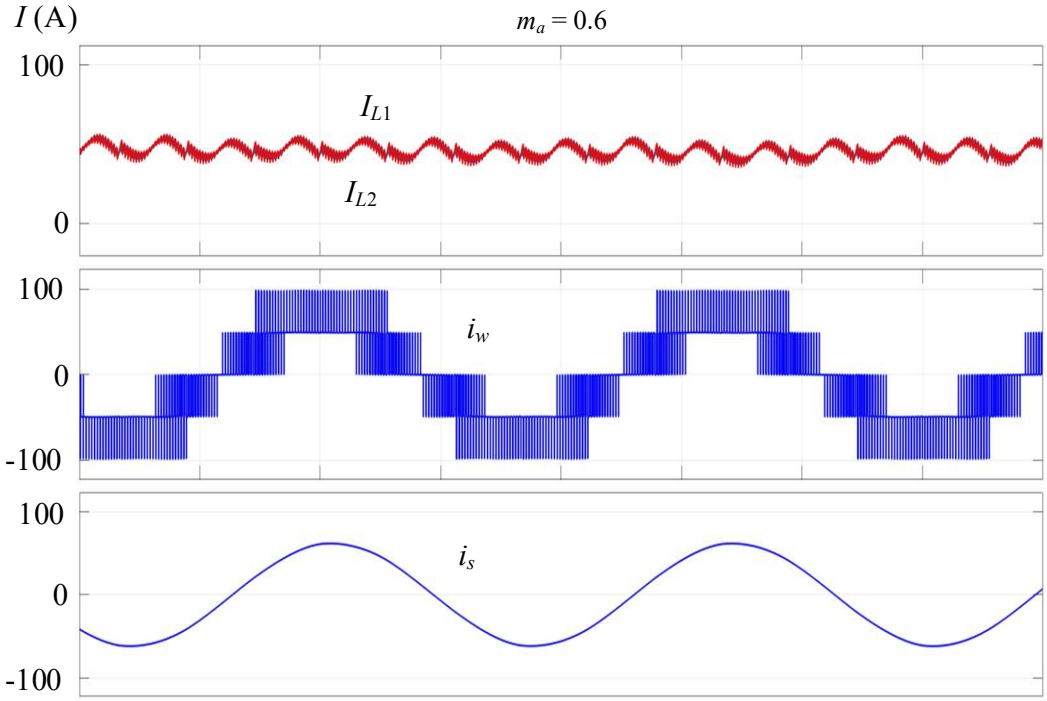
2.3 Performance verification

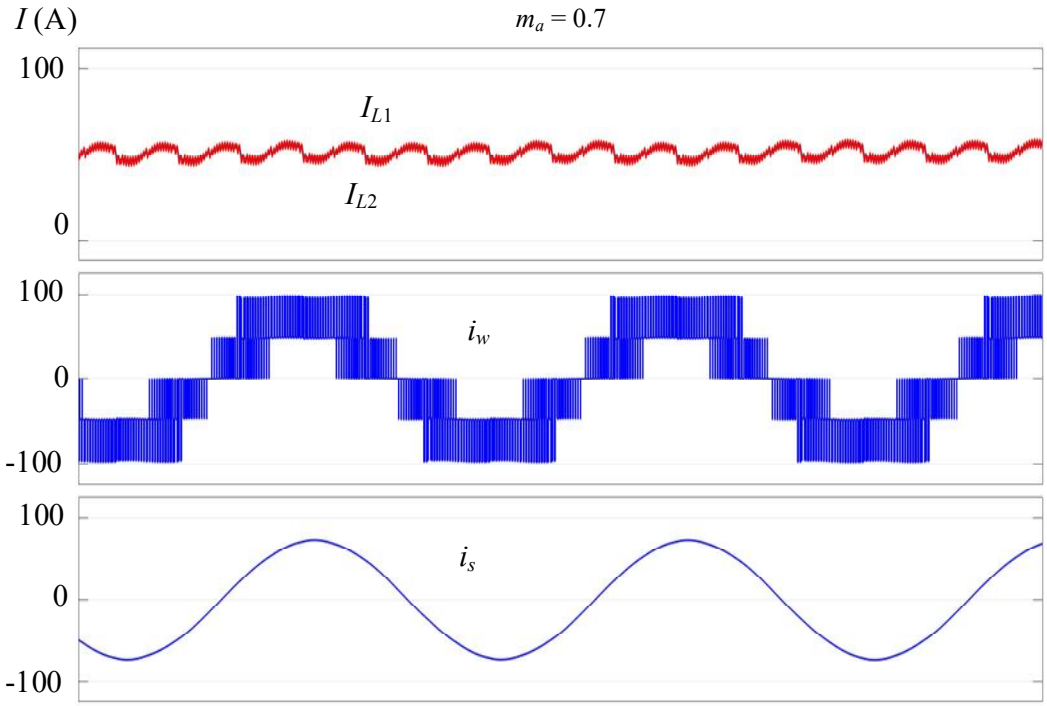
Table 2-6 Parameters in performance verification

Parameters	Simulation	Experiment
DC current	$I_{L1} = I_{L2} = 50$ A	$I_{L1} = I_{L2} = 5$ A
Fundamental frequency	60 Hz	10 Hz
Switching frequency	4320 Hz	720 Hz
Frequency modulation index m_f	72	72
Input inductance	10 mH, 12 mH	50 mH, 60 mH
Filter capacitance	55.7 uF	100 uF
Output load	10 Ω, 0.8 mH	1 Ω, 5 mH

In this section, the performance of the proposed X-type CSI is verified through both simulation and experiment, where the parameters shown in Table 2-6. Two input inductors are intentionally set to different values (10/12 mH in simulation and 50/60 mH in experiment) to simulate the mismatches of DC inductors. Note that due to the minimum overlap achieved by the dSPACE controller used in the experiments is too large at 2e-5, some narrow pulses are filtered out, leading to unexpectedly poor harmonics. To solve this issue while ensuring the experiment effectiveness, both the fundamental frequency (60 Hz reduced to 10 Hz) and the switching frequency (4320 Hz

to 720 Hz) are reduced, while the frequency modulation index m_f remains the same before and after.





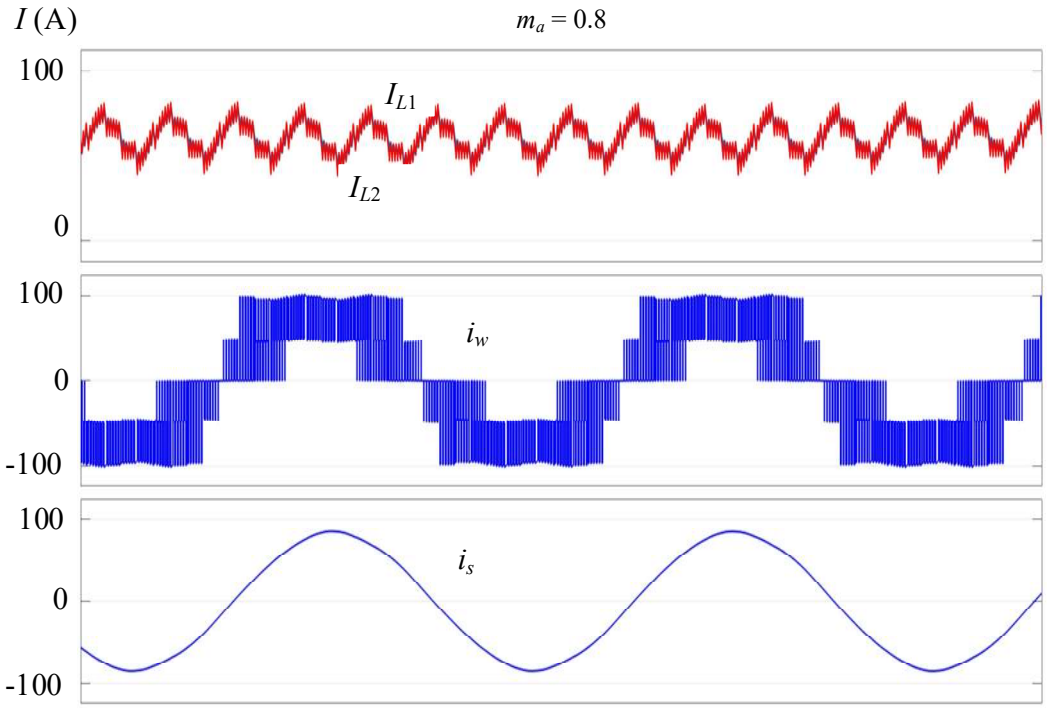


Fig. 2-14 Simulated waveforms of the proposed inverter.

A simulation model is built for the proposed converter through MATLAB/Simulink. A 3000 V voltage source is employed in the simulation with a power rating of 30 kW-0.4 MW.

Fig. 2-14 demonstrates the waveforms of the proposed inverter under the selected parameters with modulation index m_a set to 0.6, 0.7, and 0.8. As expected, the inductor currents i_{L1} and i_{L2} have a self-balancing capability, and the output PWM current i_w has five current levels (-100A, -50A, 0, 50A, 100A) with excellent symmetry. The load current i_s increases as m_a increases, with expected sinusoidal waves acquired. The current ripple of inductor current becomes larger when m_a increasing, indicating the larger L_{dc} required.

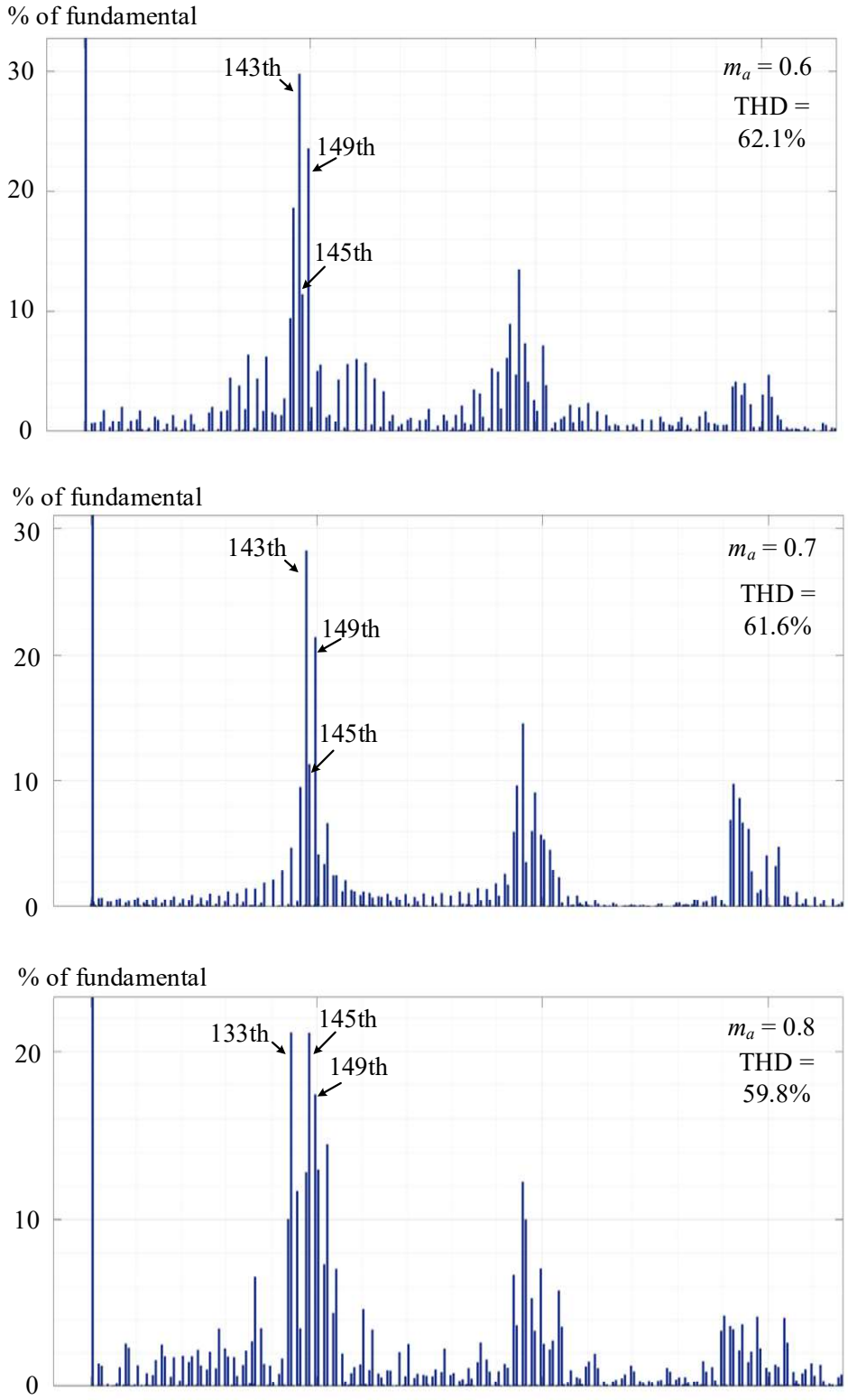
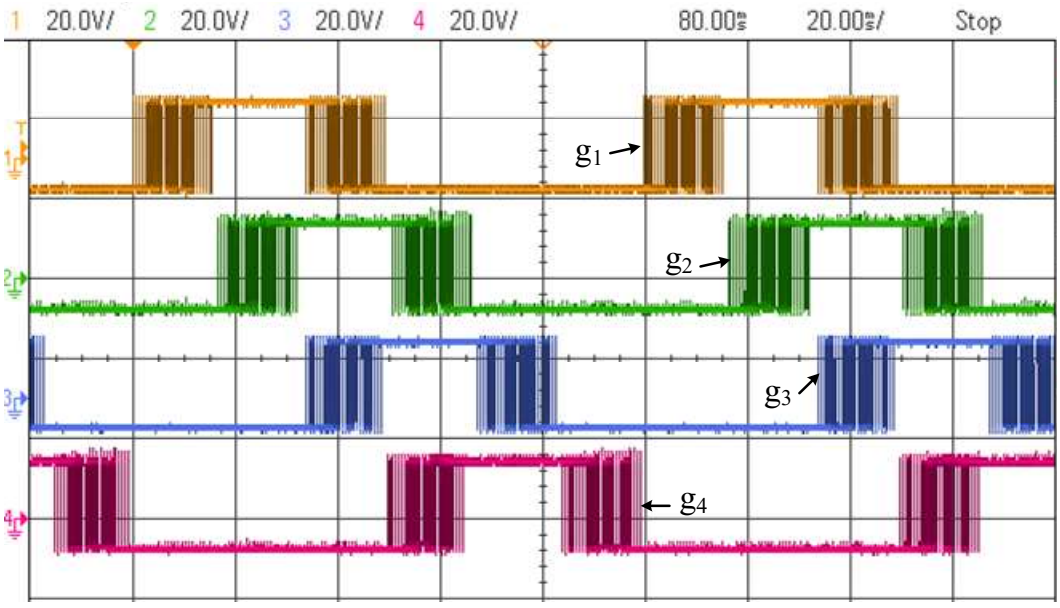


Fig. 2-15 Harmonic performance of the proposed inverter.

The harmonic content of PWM current i_w for the inverter operating at a 60 Hz fundamental frequency with a 4320 Hz switching frequency is also shown in Fig. 2-15. The total harmonic distortion (THD) of i_w are 62.1%, 61.6%, and 59.8% for m_a set to 0.6, 0.7, and 0.8, respectively. The dominant harmonics are around 8640 Hz (144^{th}), with about 25% of the fundamental current. This is in line with the characteristic of the conventional SVM that the frequency of the dominant harmonic is about twice the switching frequency ($2m_f$) [1]. When m_a increased from 0.6 to 0.8, as we can see from Fig. 2-14, the percentage of fundamental for the dominant harmonics reduces from around 30% to 21%, this indicates the better harmonic performance at large modulation indexes.

A down-scaled experiment is also constructed to verify the performance of the proposed inverter. Fig. 2-17 shows the gating signals of the converter under m_a = 0.8, where g_1-g_6 represent the gating signals for CSI side switches S_1-S_6, and g_7 represents the gating signals for DC side switch S_7. As expected, the switching frequency of S_7 is much larger than those of S_1-S_6.



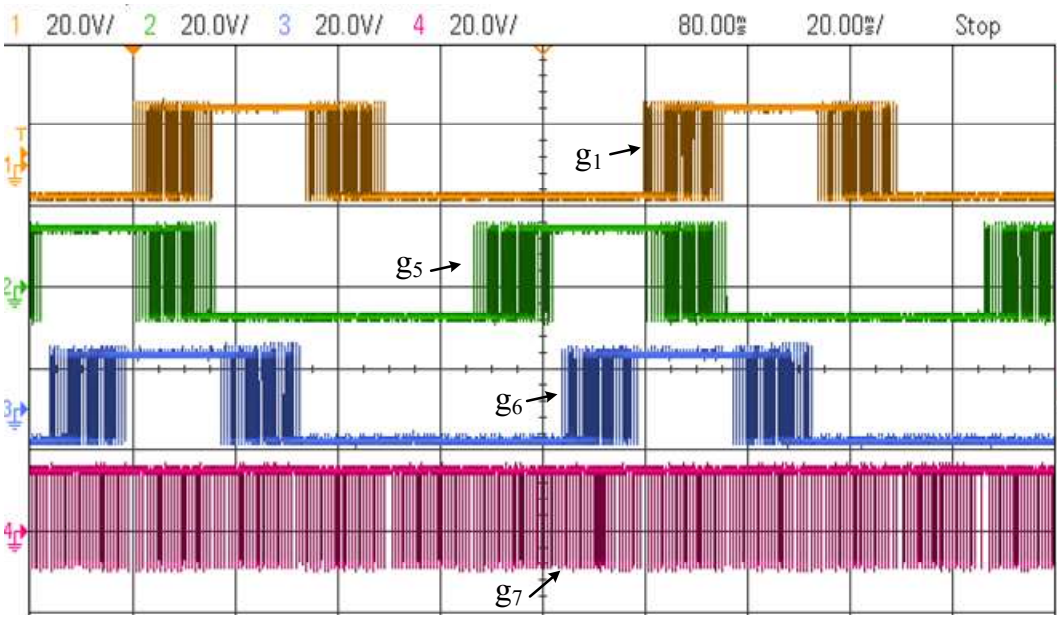
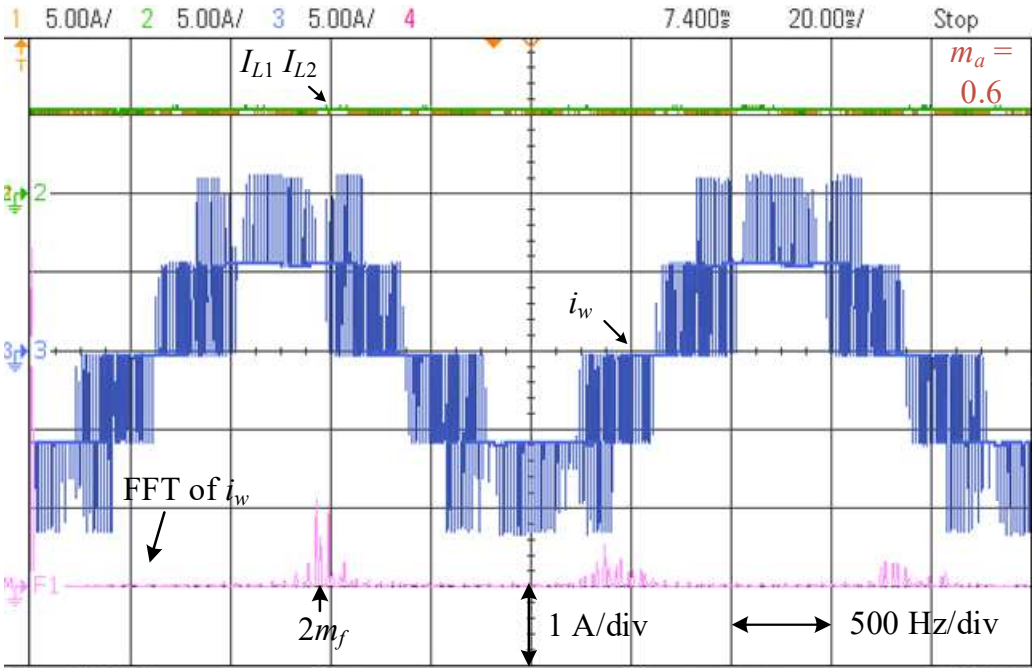


Fig. 2-16 Gating signals of the proposed inverter.



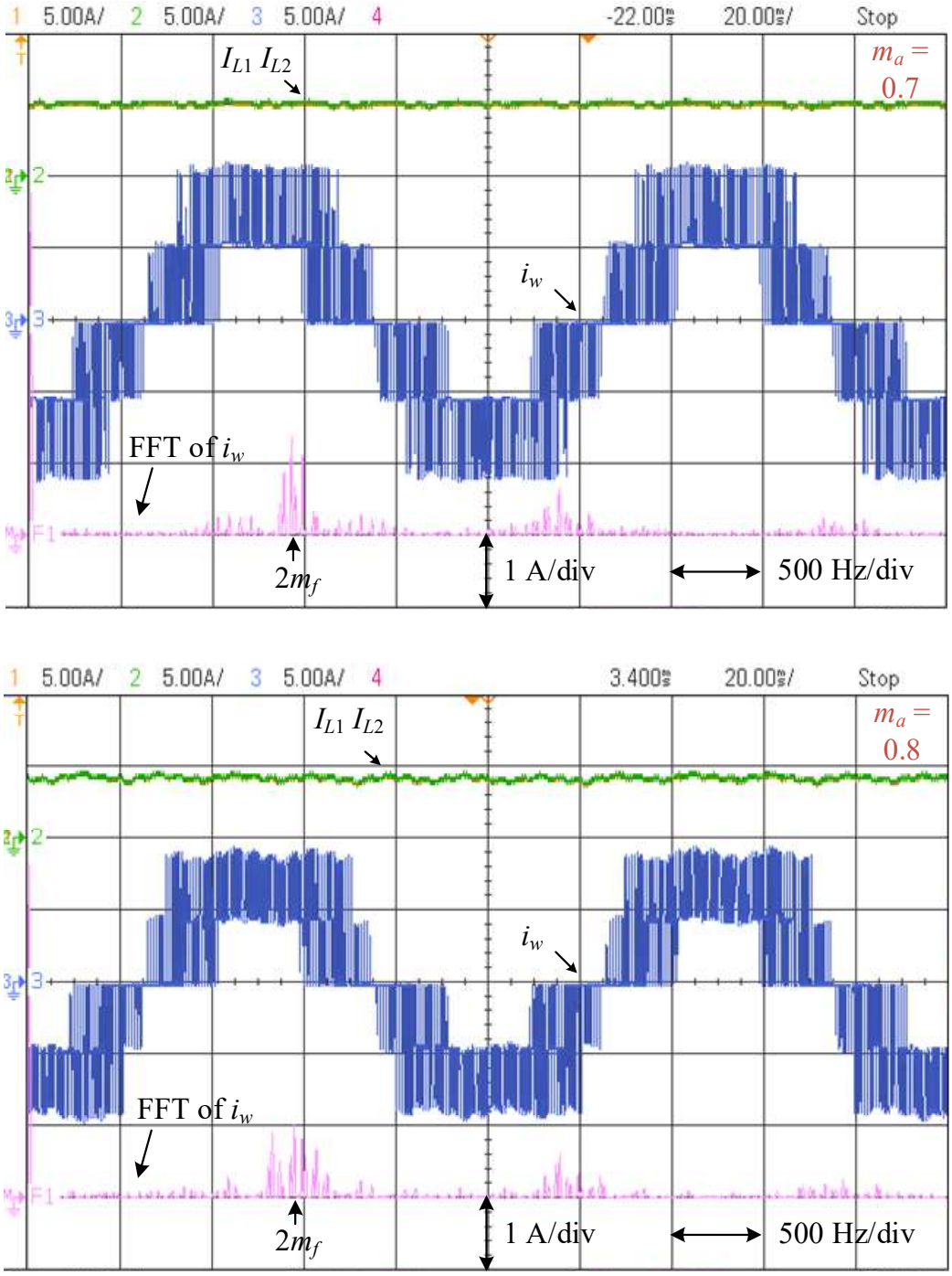


Fig. 2-17 Experimental waveforms under steady state.

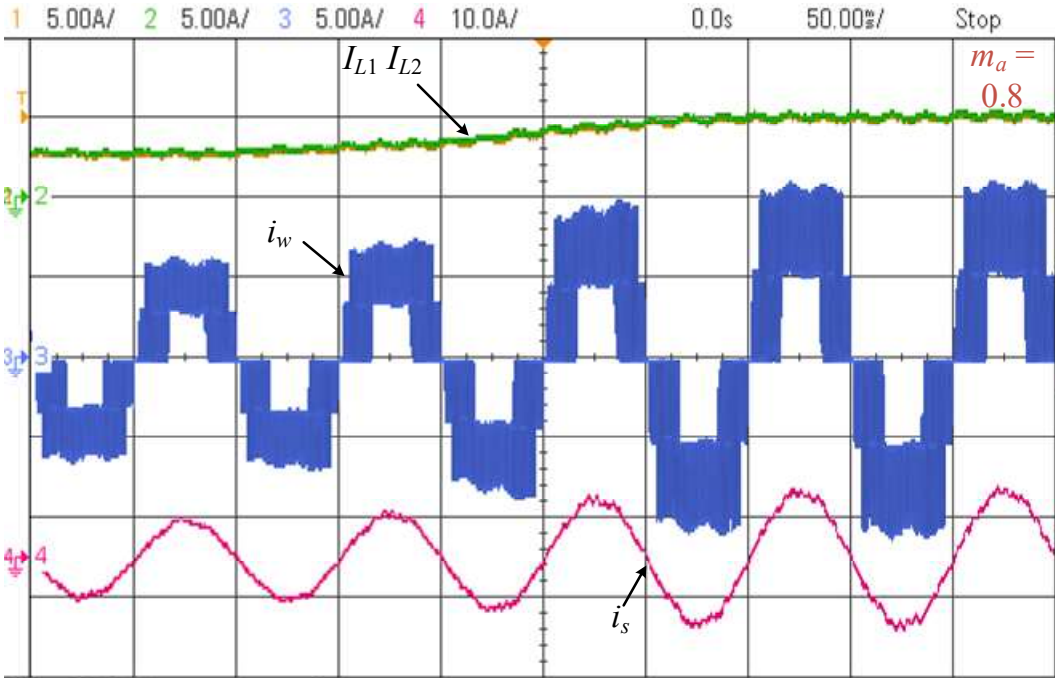


Fig. 2-18 Experimental waveforms under dynamic state.

Fig. 2-18 shows the waveforms under I_{L1} = I_{L2} = 5 A with different m_a. The current ripple of inductor current becomes larger when m_a increasing, indicating the larger L_{dc} required. The harmonic performance of i_w under different m_a is also shown in the figure, it has five current levels (-10A, -5A, 0, 5A, 10A) with excellent symmetry. The dominant harmonic orders are around $2m_f$ (around 1440Hz in the experiment).

Fig. 2-19 shows the waveforms of the proposed topology under dynamic state (I_{L1} = I_{L2} increased from 3 A to 5 A). The inductor currents I_{L1} and I_{L2}, the PWM current i_w, and the sinusoidal output current i_s are obtained. It can be found that 5 levels at the output PWM current are generated; PWM current and sinusoidal output current are increased accordingly; I_{L1} and I_{L2} have the self-balancing capability in both cases.

2.4 Summary

In this chapter, a novel X-type five-level current source inverter is proposed. Utilizing unique operation principles and an SVM-based scheme, this proposed inverter is the first

five-level CSI to achieve self-balancing inductor currents, eliminating the need for complex and costly balancing control schemes. In addition, the proposed inverter has an overvoltage clamping feature, neither additional schemes nor overrated devices are needed.

The DC utilization, passive component sizes, and efficiency are investigated in this work to identify the optimal operating range for the proposed inverter. At high modulation indexes where the proposed inverter has a better harmonic performance, the inverter suffers from low gain, as well as the large DC inductance resulting in increased cost and low efficiency.

Additionally, the DC side of the proposed inverter requires a series connection of switches due to the higher voltage gain on the switch compared to the CSI side, which will add the total switch count resulting in increased costs and losses.

Chapter 3 Γ-Type Five-Level Current Source Inverter[2]

In the previous chapter, an X-type five-level current source inverter was introduced. The inverter is notable for its unique operating principles, and with its newly designed SVM-based scheme, it becomes the first five-level CSI to achieve self-balancing inductor currents without requiring complex and costly balancing control schemes. However, at high modulation indexes where the proposed inverter has better harmonic performance, the inverter suffers from low gain, as well as the large DC inductance resulting in increased cost and low efficiency. Additionally, the DC side of the proposed inverter necessitates a series connection of switches, further driving up the cost.

This chapter begins by reviewing the advantages of the current self-balancing feature and the drawbacks of the X-type CSI. A Γ-type five-level CSI is then proposed, which retains the current self-balancing feature. At high modulation indexes, where both proposed inverters exhibit better harmonic performance, the Γ-type CSI requires significantly smaller DC inductors, leading to reduced cost, volume, and higher efficiency. The configuration, operating principle, self-balancing mechanism, modulation scheme, DC utilization, switch stress, passive component sizes, and overall efficiency of the newly proposed inverter are analyzed and compared with the X-type CSI. Finally, the performance of the proposed inverter is validated through both simulations and experiments.

3.1 Review of X-type five-level CSI

The X-type five-level CSI was introduced in the previous chapter. Its unique operation principle allows for self-balanced inductor currents, eliminating the need for additional current balancing control schemes.

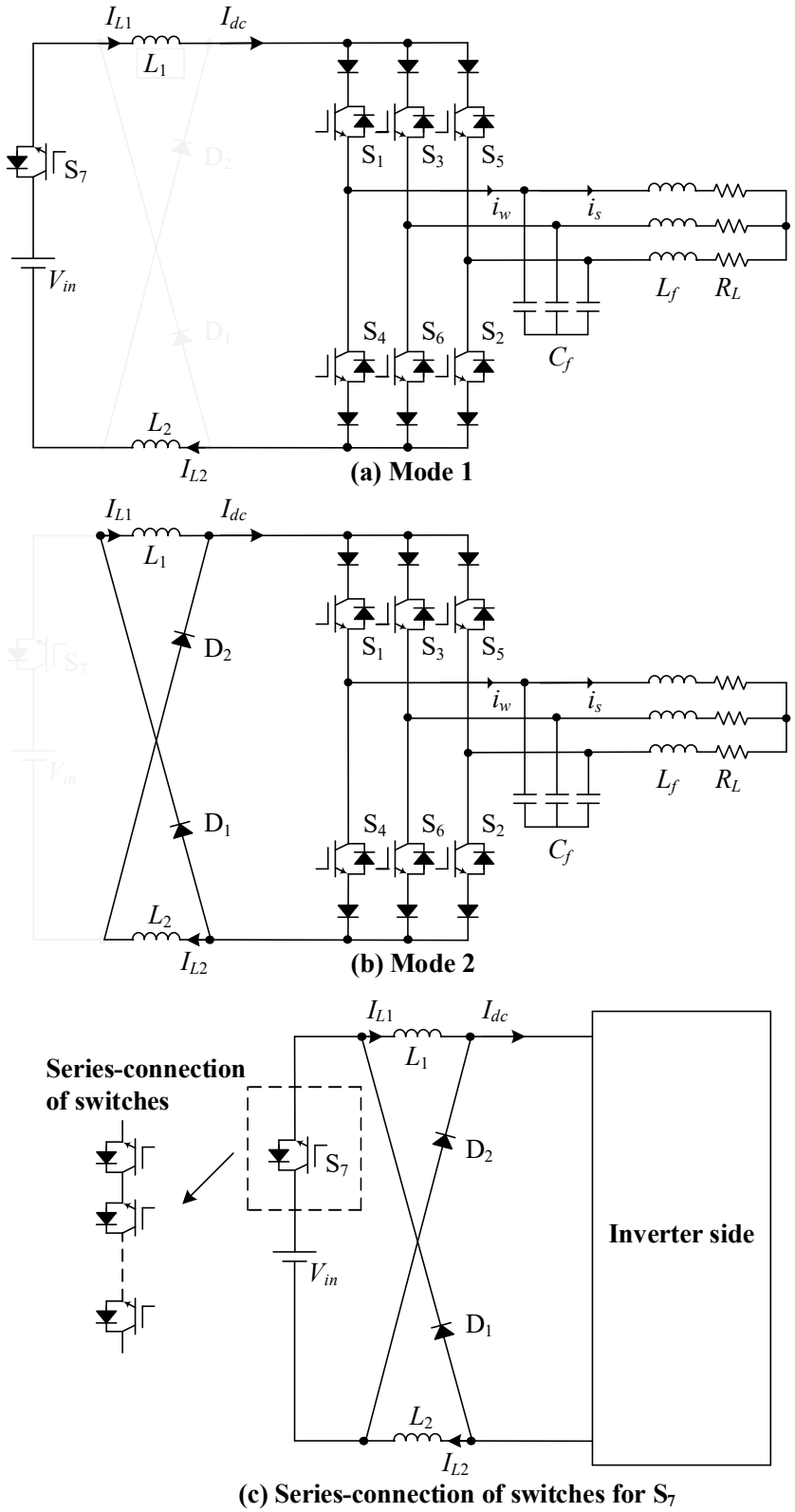


Fig. 3-1 Review of X-type five-level CSI.

Fig. 3-1 (a) and 3-1 (b) illustrate the operation modes, where inductors L_1 and L_2 are connected in series and parallel. In Mode 1, the DC current I_{dc} equals the inductor current, and in Mode 2, it equals twice the inductor current. By alternating between these two modes, a five-level output can be achieved. The self-balancing of inductor currents occurs in Mode 1, where L_1 and L_2 are connected in series, forcing their currents to be equal. Additionally, its overvoltage clamping feature ensures that no extra schemes or overrated devices are needed during mode transitions.

The primary technical challenge of the X-type CSI is the requirement for large DC inductors resulting in increased cost and low efficiency. At high modulation indexes, where CSI-based topologies perform better in terms of harmonic performance, the X-type CSI predominantly operates in Mode 2. As shown in Fig. 3-1 (b), the input source is disconnected in Mode 2, causing the DC inductors to act as parallel-connected equivalent current sources. This necessitates a lengthy inductor discharge time, ultimately leading to large DC inductor sizes. Another drawback is that the DC switch S_7 experiences higher voltage stress than the CSI switches S_1-S_6, necessitating a series connection of switches to form S_7, as depicted in Fig. 3-1 (c), which will add the total switch count resulting in increased costs and losses.

3.2 Γ-type five-level current source inverter

A Γ-type five-level CSI is proposed retaining the current self-balancing feature of the X-type CSI. At high modulation indexes where the both proposed inverters have better harmonic performance, the Γ-type CSI requires much smaller DC inductors, resulting in reduced cost and volume, and higher efficiency. The inverter structure, operating principle, self-balancing mechanism, modulation scheme, DC utilization, switch stress, passive component sizes, and overall efficiency of the newly proposed inverter are analyzed and compared with the X-type CSI.

3.2.1 Topology

Fig. 3-2 illustrates the topology of the proposed Γ-type five-level CSI.

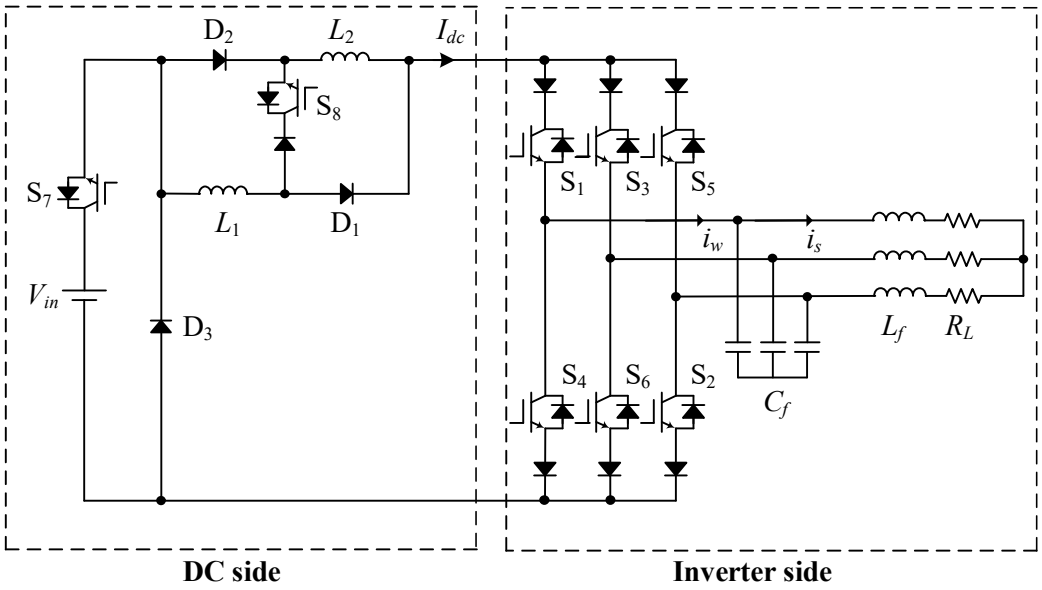


Fig. 3-2 Proposed Γ-type five-level CSI.

On the inverter side, the same single six-switch CSI as X-type CSI is used, featuring the following components:

1) Switching devices: S_1 to S_6 are power switches with reverse voltage blocking capabilities, such as gate turn-Off thyristors (GTO), symmetrical gate commutated thyristors (SGCT), or insulated gate bipolar transistors (IGBT)/metal-oxide-semiconductor field-effect transistors (MOSFET) in series with a diode.

2) Three-phase capacitor: Located at the inverter output, this capacitor C_f aids in the commutation of the switching devices. For example, when switch S_1 is turned off, the inverter PWM current i_w drops to zero rapidly. The capacitor provides a path for the energy trapped in the phase-A load inductance, preventing high voltage spikes that could damage the switching devices.

3) LC filter: The combination of C_f and load inductance L_f together form an LC filter. This filter removes most of the harmonics from the PWM current i_w, ensuring the sinusoidal current i_s meets specific output requirements (e.g. the current harmonics distortion criteria for the design of electrical systems in IEEE 519-2014).

4) Inverter output: As an example, the output is connected to an AC motor in Fig. 3-2, represented by load inductance L_f and load resistance R_L. Additionally, the output can be connected with grid, with power factor control being required.

On the DC side, a different DC-DC converter is used, featuring the following components:

1) Input source: The proposed inverter uses a single voltage source, akin to other topologies discussed in Section 1.2.1, and the X-type five-level CSI in Section 2.2.1.

2) DC inductors: The inductors L_1 and L_2 make the DC current I_{dc} smooth and continuous, while also facilitates the inverter's operational principles

3) Additional components: S_7 can be an IGBT or MOSFET, S_8 should be a switch with reverse voltage-blocking capability such as SGCT, IGBT with diode, etc., and D_1-D_3 are power diodes. These components are included to support the unique operations of the inverter.

3.2.2 Five-level output generation

Fig. 3-3 illustrates the two operation modes of the proposed inverter:

Mode 1: Illustrated in Fig. 3-3 (a), S_7 is turned on and S_8 is turned off, DC inductors L_1 and L_2 are connected in parallel. L_1 and L_2 are connected in parallel through D_1 and D_2, respectively. The two inductors now act as parallel-connected current sources. I_{dc} equals

the combination of the two inductor currents (I_{dc}=I_{L1}+I_{L2}=2I_L). Therefore, the output PWM current has three levels, 2I_L, 0, and -2I_L.

The currents through both inductors I_{L1} and I_{L2}, as well as the DC current I_{dc}, are equal (I_{dc}=I_{L1}= I_{L2}=I_L). Therefore, the output PWM current has three levels, I_L, 0, and -I_L.

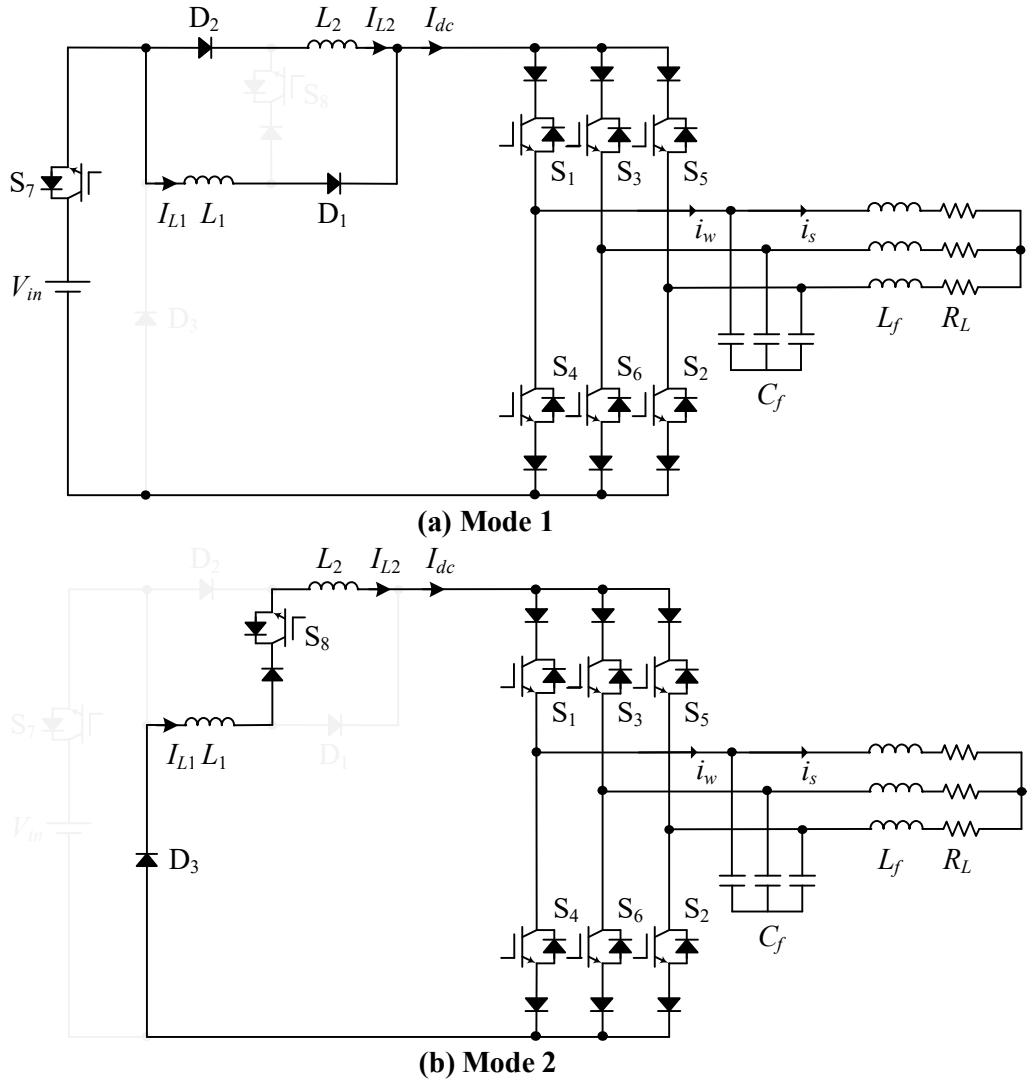


Fig. 3-3 Operation modes of the Γ-type five-level CSI.

Mode 2: Illustrated in Fig. 3-3 (b), S_7 is turned off and S_8 is turned on, the input source V_{in} is disconnected, and DC inductors L_1 and L_2 are connected in series. L_1 and L_2 are connected in parallel through D_1 and D_2, respectively. The currents through both

inductors I_{L1} and I_{L2}, as well as the DC current I_{dc}, are equal (I_{dc}=I_{L1}= I_{L2}=I_L). Hence, I_L, 0, and -I_L are generated at the CSI output.

Five-level output currents can be obtained with the above two operation modes working alternatively (±I_L, 0, and ±2I_L). For example, when S_1, S_2, and S_8 are turned on, the three-phase output currents i_{wA}, i_{wB}, and i_{wC} are I_L, 0, and -I_L, respectively; when S_1, S_2, and S_7 are turned on, i_{wA}, i_{wB}, and i_{wC} are 2I_L, 0, and -2I_L, respectively.

3.2.3 Modulation design

A similar SVM-based scheme (designed in Section 2.2.3) can be used here with different switching states of the Γ-type five-level CSI applied:

Switching states: According to the two operation modes of the proposed inverter shown in the last section, the switching states and corresponding output PWM currents are shown in Table 3-1. There are a total of 18 switching states, including active and zero switching states. Similar to existing CSIs, the modulation scheme for the proposed CSI is not unique. Any CSI modulation scheme can be designed as long as the switching states in Table 3-1 are satisfied.

Table 3-1 Space vectors of the proposed inverter

Space vectors		On-state switches	Output currents		
			i_{wA}	i_{wB}	i_{wC}
Large vectors	I_{L1}	{127}	2I_L	0	-2I_L
	I_{L2}	{237}	0	2I_L	-2I_L
	I_{L3}	{347}	-2I_L	2I_L	0
	I_{L4}	{457}	-2I_{dc}	0	2I_L
	I_{L5}	{567}	0	-2I_L	2I_L
	I_{L6}	{617}	2I_L	-2I_L	0
Small vectors	I_{S1}	{128}	I_L	0	-I_L
	I_{S2}	{238}	0	I_L	-I_L
	I_{S3}	{348}	-I_L	I_L	0
	I_{S4}	{458}	-I_L	0	I_L

	I_{S5}	{568}	0	$-I_L$	I_L
	I_{S6}	{618}	I_L	$-I_L$	0
Zero Vectors	I_0	{147} {257} {367} {148} {258} {368}	0	0	0

Space vectors: The resultant space vectors for the switching states are shown in the space vector diagram in Fig. 3-4, where I_{L1} to I_{L6} are the large vectors, I_{S1} to I_{S6} are the small vectors, and I_0 is the zero vector. The large/small vectors form a hexagon with six equal sectors, while the zero vector lies at the center. Note that the transformation from switching states to space vectors is the same as the conventional CSIs, thus not repeated here, please refer to [1] for such details. To facilitate the dwell time calculation, the space vector diagram can be divided into six triangular sectors (I to VI), each of which can be further divided into five subsectors (1 to 5), as shown in Fig. 3-4. Eventually, there are 30 subsectors in total.

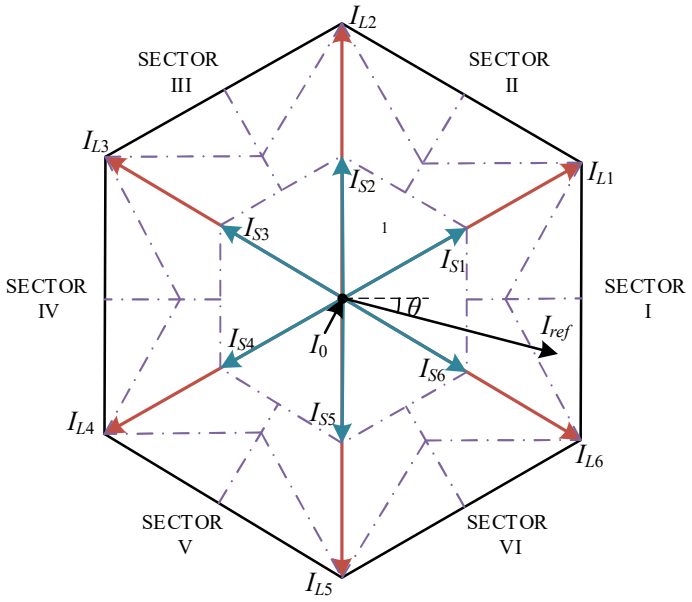


Fig. 3-4 Space vector diagrams of the proposed inverter.

Dwell time calculation: The reference vector I_{ref} is synthesized by three vectors. Depending on the different sectors and subsectors I_{ref} falls into, the synthesized scheme is listed below:

1) one zero vector and two small vectors in Subsector 1.

2) two small vectors and one large vector in Subsector 2 and 4.

3) one small vector and two large vectors in Subsector 3 and 5.

For example, with I_{ref} falling into Subsector 3 in Sector I, as shown in Fig. 3-5, it is synthesized by one small vector (I_{S6}) and two large vectors (I_{L6} and I_{L1}).

By converting the three-phase (abc) current vectors into two-phase ($\alpha\beta$) based on the ampere-second balancing principle, the relationships between the vectors and dwell times can be derived:

$$\begin{cases} I_{ref}T_s = I_{ap}T_p + I_{aq}T_q + I_{ar}T_r \\ T_s = T_p + T_q + T_r \end{cases} \tag{3-1}$$

where the subscript a represents small (S), large (L), or zero (0) vectors; T_s the sampling period; T_p, T_q, and T_r represent the dwell times for the respective vectors.

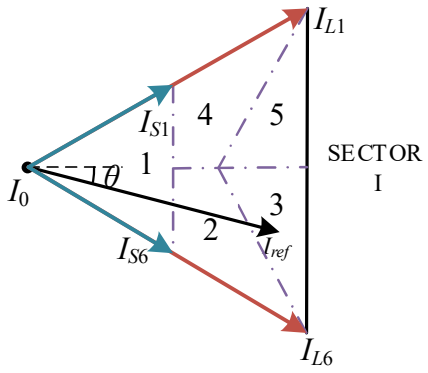


Fig. 3-5 Space vector diagrams in Sector 1.

Applying the example in Fig. 3-5 when I_{ref} falling into Subsector 3 in Sector I, equation (2-1) can be simplified as:

$$\begin{cases} I_{ref}T_s = I_{L1}T_4 + I_{S6}T_1 + I_{L6}T_2 \\ T_s = T_4 + T_1 + T_2 \end{cases} \tag{3-2}$$

Following the above procedure, each selected vector's dwell times under different subsectors and sectors can be calculated and summarized in Table 3-2, where m_a is the modulation index.

Table 3-2 Vector Dwell Times of Different Subsectors

Subsector	Vector	Dwell time	Dwell time calculation
1	I_0	T_0	$T_s - T_1 - T_3$
	I_{S6}	T_1	$(\cos\theta - \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L6}	T_2	0
	I_{S1}	T_3	$(\cos\theta + \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L1}	T_4	0
2	I_0	T_0	0
	I_{S6}	T_1	$T_s - T_2 - T_3$
	I_{L6}	T_2	$(2 * \cos\theta * m_a - 1) * T_s$
	I_{S1}	T_3	$(\cos\theta + \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L1}	T_4	0
3	I_0	T_0	0
	I_{S6}	T_1	$T_s - T_2 - T_4$
	I_{L6}	T_2	$((1.5 * \cos\theta - 0.5 * \sqrt{3}\sin\theta) * m_a - 1) * T_s$
	I_{S1}	T_3	0
	I_{L1}	T_4	$0.5 * (\cos\theta + \sqrt{3}\sin\theta) * T_s * m_a$
4	I_0	T_0	0
	I_{S6}	T_1	$(\cos\theta - \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L6}	T_2	0
	I_{S1}	T_3	$T_s - T_1 - T_4$
	I_{L1}	T_4	$(2 * \cos\theta * m_a - 1) * T_s$
5	I_0	T_0	0
	I_{S6}	T_1	0
	I_{L6}	T_2	$0.5 * (\cos\theta - \sqrt{3}\sin\theta) * T_s * m_a$
	I_{S1}	T_3	$T_s - T_2 - T_4$
	I_{L1}	T_4	$((1.5 * \cos\theta + 0.5 * \sqrt{3}\sin\theta) * m_a - 1) * T_s$

Table 3-3 Sequence design of the proposed inverter

	Sequence	Subsector 1	Subsector 2	Subsector 4	Subsector 1
$0.5 < m_a < 0.577$	SQ1	I_{S1}-I_0-I_{S6}	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{S1}-I_{L1}	I_{S1}-I_0-I_{S6}
	SQ2	I_{S1}-I_0-I_{S6}	I_{L6}-I_{S6}-I_{S1}	I_{L1}-I_{S1}-I_{S6}	I_{S1}-I_0-I_{S6}
	SQ3	I_{S1}-I_{S6}-I_0	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{S1}-I_{L1}	I_{S1}-I_{S6}-I_0
	SQ4	I_{S6}-I_{S1}-I_0	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{S1}-I_{L1}	I_{S6}-I_{S1}-I_0
	Sequence	Subsector 2	Subsector 3	Subsector 5	Subsector 4
$0.577 < m_a < 0.667$	SQ5	I_{L6}-I_{S6}-I_{S1}	N/A	N/A	I_{S6}-I_{S1}-I_{L1}
	SQ6	I_{L6}-I_{S6}-I_{S1}	N/A	N/A	I_{L1}-I_{S1}-I_{S6}
	SQ7	I_{S1}-I_{S6}-I_{L6}	N/A	N/A	I_{S6}-I_{S1}-I_{L1}
	SQ8	I_{S1}-I_{S6}-I_{L6}	N/A	N/A	I_{L1}-I_{S1}-I_{S6}
$m_a > 0.667$	SQ9	I_{L6}-I_{S6}-I_{S1}	I_{S6}-I_{L6}-I_{L1}	I_{L6}-I_{L1}-I_{S1}	I_{S6}-I_{S1}-I_{L1}
	SQ10	I_{L6}-I_{S6}-I_{S1}	I_{S6}-I_{L6}-I_{L1}	I_{S1}-I_{L1}-I_{L6}	I_{S6}-I_{S1}-I_{L1}
	SQ11	I_{L6}-I_{S6}-I_{S1}	I_{L1}-I_{L6}-I_{S6}	I_{L6}-I_{L1}-I_{S1}	I_{L1}-I_{S1}-I_{S6}
	SQ12	I_{L6}-I_{S6}-I_{S1}	I_{L1}-I_{L6}-I_{S6}	I_{S1}-I_{L1}-I_{L6}	I_{L1}-I_{S1}-I_{S6}
	SQ13	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{L6}-I_{L1}	I_{L6}-I_{L1}-I_{S1}	I_{S6}-I_{S1}-I_{L1}
	SQ14	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{L6}-I_{L1}	I_{S1}-I_{L1}-I_{L6}	I_{S6}-I_{S1}-I_{L1}
	SQ15	I_{S1}-I_{S6}-I_{L6}	I_{L1}-I_{L6}-I_{S6}	I_{L6}-I_{L1}-I_{S1}	I_{L1}-I_{S1}-I_{S6}
	SQ16	I_{S1}-I_{S6}-I_{L6}	I_{L1}-I_{L6}-I_{S6}	I_{S1}-I_{L1}-I_{L6}	I_{L1}-I_{S1}-I_{S6}

Sequence sequences*:* Similar to the space vector modulation for the conventional CSI, the switching sequence design for the X-type CSI should also satisfy the following two requirements for the minimization of switching frequencies [1]:

1) The transition from one switching state to the next involves only two switches, one being switches on and one being switches off.

2) The transition for I_{ref} moving from one sector/subsector to the next requires the minimum number of switchings.

In the X-type five-level CSI, varying m_a values result in I_{ref} traversing different subsectors, as illustrated in Fig. 2. The scenarios are as follows (in respective sector):

Case 1: for $m_a < 0.5$, I_{ref} stays in Subsector 1.

Case 2: for $0.5 < m_a < 0.577$, I_{ref} follows the path: Subsector 1 - Subsector 2 - Subsector 4 - Subsector 1.

Case 3: for $0.577 < m_a < 0.667$, I_{ref} follows the path: Subsector 2 - Subsector 4.

Case 4: for $0.667 < m_a < 1$, I_{ref} follows the path: Subsector 2 - Subsector 3 - Subsector 5 - Subsector 4.

When $m_a < 0.5$ (case 1), the X-type functions as a three-level CSI, therefore, this case will not be discussed. In the design, m_a should always be larger than 0.5. Table 3-3 presents the switching sequences meeting the specified design criteria (mentioned above) in case 2, case 3, and case 4.

3.2.4 Self-balancing mechanism

Same as the previous proposed X-type CSI, the Γ-type five-level also has the inductor current self-balancing feature. Fig. 3-6 shows the simulated waveforms of inductor currents (i_{L1} and i_{L2}) and inductor voltages (V_{L1} and V_{L2}). Noted that the inductors are set differently (L_1 = 10 mH and L_2 = 20 mH) to simulate the inductor mismatch.

As shown in Fig. 2-6, each switching period is divided into the following four parts:

1) t_0 - t_1: At time t_0, S_7 is switched on and S_8 is switched off. The inverter starts operating in Mode 1, where the two inductors are charging in parallel. Between t_0 and t_1, since both inductors are charging in parallel, the voltages across the two inductors are the same (V_{L1} = V_{L2} = V_{in} - V_{dc}). Since the introduced mismatch in the inductors, inductor currents i_{L1} and i_{L2} are increasing at different rates, resulting in different instantaneous inductor currents ($i_{L1} \neq i_{L2}$), as shown in Fig. 3-6. The corresponding equivalent circuit under this time interval is shown in Fig. 3-7 (a).

2) t_1 - t_2: At time t_1, there is a change in the switching states of the CSI, resulting in a change in V_{dc}. The resultant V_{L1} and V_{L2} change accordingly, as shown in Fig. 3-6. Between t_1 and t_2, the inverter still operates in Mode 1, where i_{L1} and i_{L2} continue to increase at different rates until time t_2 (the end of Mode 1), at which the difference between i_{L1} and i_{L2} reaches the maximum as shown in Fig. 3-6. The equivalent circuit under this time interval is shown in Fig. 3-7 (b)

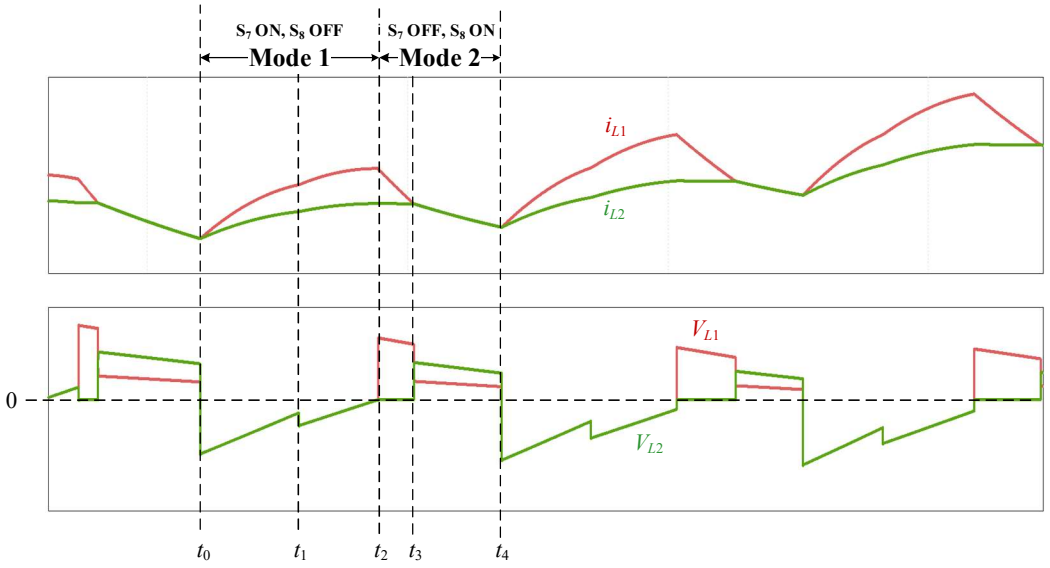


Fig. 3-6 Transient waveforms of the proposed inverter.

3) t_2 - t_3: At time t_2, S_8 is switched on, and S_7 is switched off, the two inductors start to discharge in series. i_{L1} and i_{L2} are supposed to be the same. If so, the inductor voltages suffer an overvoltage due to $i_{L1} \neq i_{L2}$. However, as shown in Fig. 3-6, the inductor currents are not immediately the same after time t_2, and there is no overvoltage. This is

because when V_{L1} becomes larger than V_{L2} at time t_2, the diode D_1 (D_2 for the case when $L_1 > L_2$) will then be forward-biased and turned on. As a result, i_{L2} decreases gradually until it equals i_{L2} at t_3, and then D_1 is turned off. There is no change in currents; thus, no overvoltage occurs. The equivalent circuit is shown in Fig. 3-7 (c).

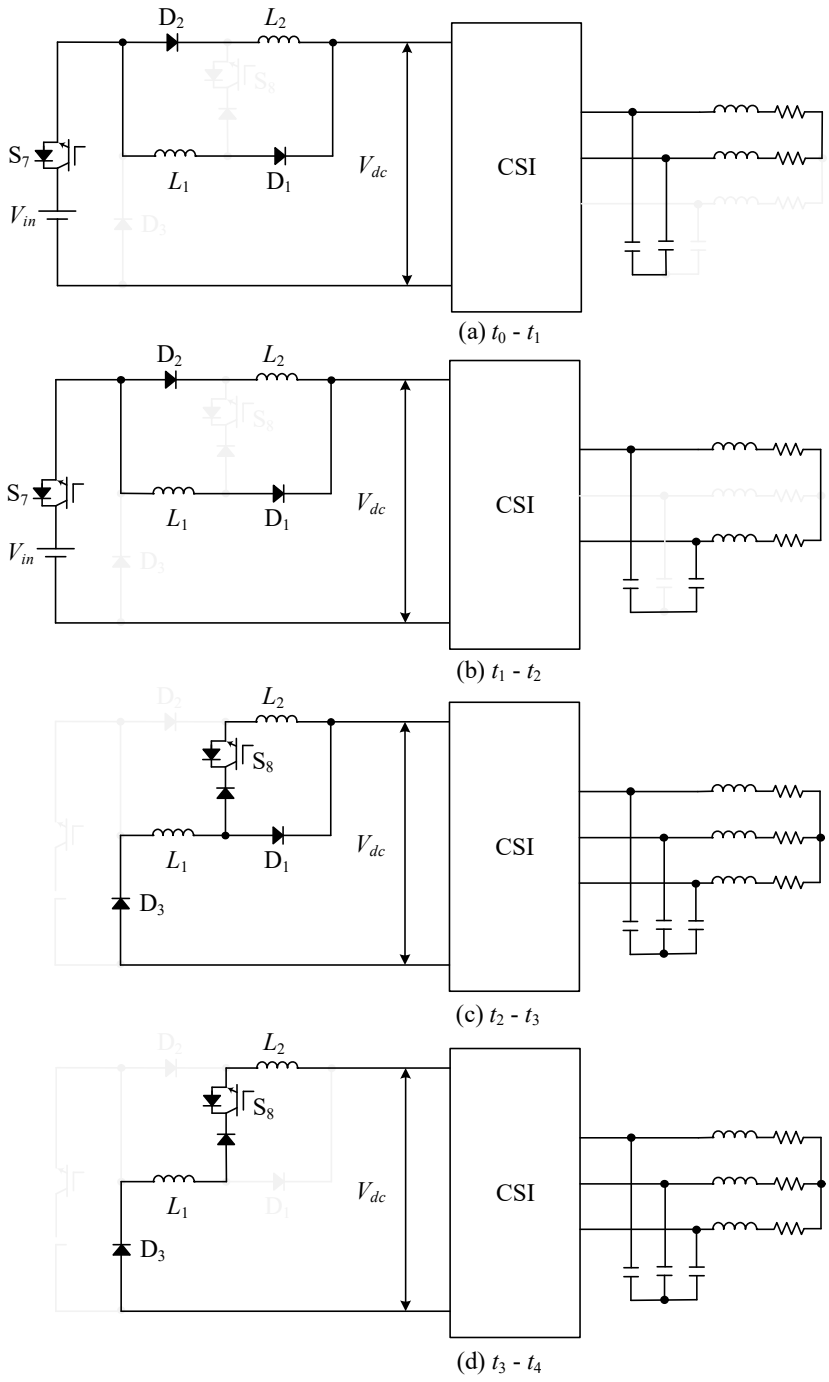


Fig. 3-7 Transient states of the proposed inverter.

4) t_3 - t_4: At time t_3, i_{L1} and i_{L2} become identical, D_1 is then inactive. Between t_3 and t_4, S_7 remains turned off, and S_8 remains turned on. L_1 and L_2 are connected in series, and the inverter operates in Mode 2. Due to the series-connection, i_{L1} and i_{L2} keep identical, and the self-balancing feature is insured. V_{L1} and V_{L2} are different due to inductor mismatch. The equivalent circuit under this time interval is shown in Fig. 3-7 (d).

5) At time t_4, S_7 is switched on, S_8 is switched off, and the cycle from 1) is repeated.

In summary, the self-balancing feature of the inductor currents is achieved in Mode 2 when the inductors are connected in series. Besides, the gradual change in inductor voltages during mode transitions, facilitated by the additional diodes, ensures that no overvoltage occurs.

3.2.5 DC utilization

To derive the proposed converter's DC utilization, the analysis is divided into the DC side and the inverter side.

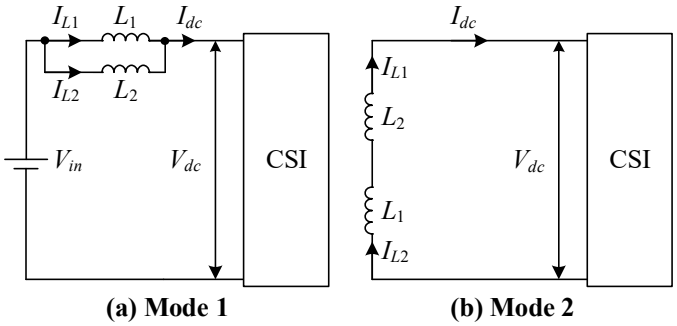


Fig. 3-8 Simplified dc side circuits in Mode 1 and 2.

Fig. 3-8 illustrates the simplified dc side circuits. During Mode 1, switch S_7 is turned on and switch S_8 is turned off, I_{dc} equals the combination of the two inductor currents ($I_{dc}=I_{L1}+I_{L2}=2I_L$). During Mode 2, S_7 is turned off and S_8 is turned off, the currents through both inductors I_{L1} and I_{L2}, as well as the DC current I_{dc}, are equal ($I_{dc}=I_{L1}= I_{L2}=I_L$).

The duty cycle of S_7, denoted as D, serves to illustrate the relationship between the input voltage V_{in} and the DC voltage V_{dc}. Applying the voltage-second principle to the DC inductor yields the following equation (3-3), where V_{in}-V_{dc} represents the inductor voltage for both L_1 and L_2 in Mode 1, and $0.5V_{dc}$ is the inductor voltage for both L_1 and L_2 in Mode 2 (assuming equal inductances for L_1 and L_2). Consequently, the relationship ratio between V_{in} and V_{dc} is expressed by D, as indicated in (7).

$$(V_{in}-V_{dc})D=0.5V_{dc}(1-D) \tag{3-3}$$

$$\frac{V_{dc}}{V_{in}}=\frac{2D}{1+D} \tag{3-4}$$

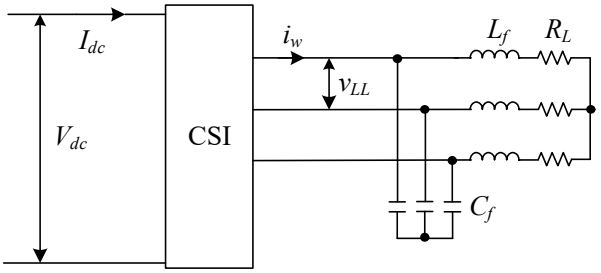


Fig. 3-9 Simplified inverter side circuit.

For the DC-AC segment, as shown in Fig. 3-9, assuming neglectable power losses in the inverter, the input power of the CSI equals the output power of the CSI. This leads to equation (3-5), where the left side denotes the input power of the six-switch CSI, and the right side represents the output power. V_{LL} signifies the line-to-line voltage at the inverter output, I_{w1} is the RMS value of the fundamental component of i_w, φ is the power factor angle, and I_{dc_avg} is the average input current of the CSI, expressible as (3-6). It's important to note that $2I_LD$ and $I_L(1\text{-}D)$ are the current outcomes from Mode 1 and Mode 2, respectively, aligning with (3-3).

$$V_{dc}I_{dc\_avg}=\sqrt{3}V_{LL}I_{w1}\cos\varphi \tag{3-5}$$

$$I_{dc\_avg}=2I_LD+I_L(1-D) \tag{3-6}$$

The correlation between I_{w1} in (3-5) and I_{dc} in (3-6) can be articulated as (3-7), stemming from the definition of the modulation index m_a. Furthermore, with the designated modulation, m_a determines the total time for each switch to turn on or off, thereby enabling the expression of the duty cycle D of S_7 in terms of m_a, as depicted in (3-8).

$$G_i = \frac{\sqrt{2} I_{w1}}{I_{dc}} = m_a \tag{3-7}$$

$$D = \frac{6 m_a}{\pi} - 1 \tag{3-8}$$

By substituting equations (3-6), (3-7) and (3-8) into (3-5), the relationship ratio between V_{LL} and V_{dc} can be formulated as equation (3-9). Notably, as m_a is eliminated in both the numerator and denominator of the fraction, this ratio is solely affected by the load.

$$\frac{V_{LL}}{V_{dc}} = \frac{\sqrt{6}}{\pi \cos\varphi} \tag{3-9}$$

Integrating equations (3-4), (3-8), and (3-9) yields the voltage gain of the proposed converter, denoted by m_a:

$$G_v = \frac{V_{LL}}{V_{in}} = \frac{\frac{12 m_a}{\pi} - 2}{\sqrt{6} m_a \cos\varphi} \tag{3-10}$$

Fig. 3-10 depicts a comparison of voltage gain between the proposed Γ-type CSI and the X-type CSI. Both inverters are operated under $m_a > 0.5$ to guarantee the generation of a five-level output. The voltage gain of the Γ-type CSI steadily increases with m_a and significantly surpasses that of the X-type CSI under high modulation indexes.

In order to insure the five-level output, the working range of the proposed inverter is $0.5<m_a<1$. Within this working range, the proposed inverter is a voltage buck converter,

the higher voltage gain is acquired at low modulation indexes and the maximum gain is around 1 when m_a=1.

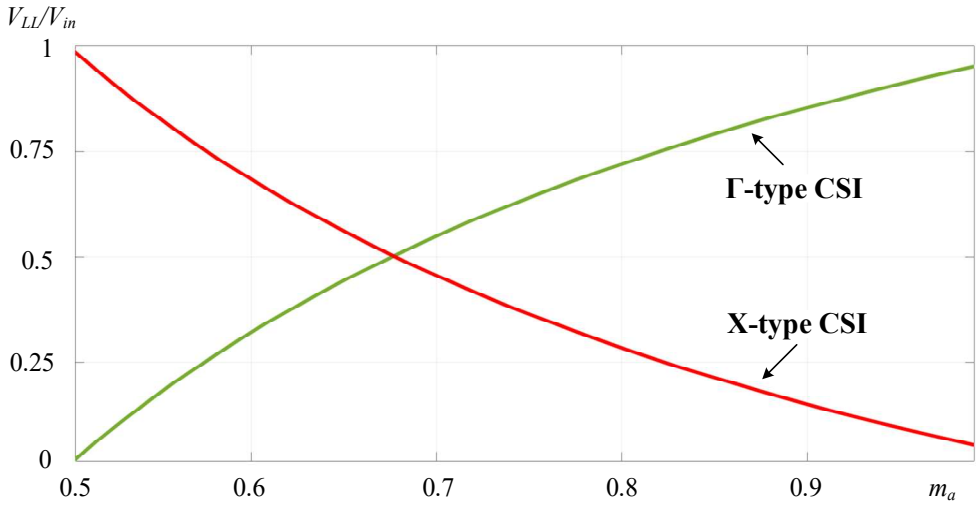


Fig. 3-10 Voltage gain comparison between the proposed inverters.

3.2.6 Passive component sizes

The size of the passive components significantly impacts the cost and volume of the CSI system. This section addresses this aspect by examining the sizes of the DC inductor and the LC filter:

DC inductor size:

L_1 and L_2, the DC inductors in the proposed inverter, are the key components maintaining the operation modes of the proposed converter. At the same time, the size of the DC inductors also determines DC current ripple. For keeping the DC current ripple less than a certain value (12%, for example) to maintain the continuity and smoothness of the DC current, the minimum value of the DC inductors is shown in (3-11):

$$L_1 = L_2 = \frac{L_{total}}{2} = \frac{1}{2} * \frac{(V_{in} - V_{dc})\Delta t}{12\% I_L} \tag{3-11}$$

where Δt is the dwell times shown in Table 3-2. The relationships between V_{in} and V_{dc} is derived in (3-4).

Through the relationship between load terminal current and voltage, the relationship between DC current I_{dc} and PWM current I_w in (3-7), and the voltage gain in (3-10), the expression of I_{dc} can be given by (3-12). It can be found that I_{dc} is related to load resistance R, modulation index m_a, and input voltage V_{in}.

$$I_{dc} = \frac{V_{LL}\cos\varphi}{\sqrt{6}m_a R} = \frac{(\frac{6m_a}{\pi} - 1)V_{in}}{6m_a^2 R} \tag{3-12}$$

$$L_1 = L_2 = \frac{(\frac{\pi}{3m_a} - 1)V_{in}\Delta t}{12\% I_{dc}} \quad \frac{3m_a^2 R_L(\frac{\pi}{3m_a} - 1)\Delta t}{12\%(\frac{6m_a}{\pi} - 1)} \tag{3-13}$$

Submitting equations (3-4), (3-10), and (3-12) into (3-11), the input inductance can be expressed as (3-13). V_{in} in the numerator cancels out the V_{in} contained in I_{dc} in the denominator. Therefore, the magnitude of L_{dc} has nothing to do with V_{in}. When the load resistance R is fixed, the size of the DC inductors is only related to the modulation index m_a.

In order to investigate the optimal operating range of the proposed inverter, the required L_{dc} at different m_a is calculated and verified by simulation. Fig. 3-11 presents a comparison of the required L_{dc} under varying m_a values between the proposed Γ-type CSI and the X-type CSI. The Γ-type CSI demands approximately 0.7-1 pu L_{dc} under high modulation indexes ($m_a > 0.8$), only slightly exceeding the requirements for conventional 3-level CSI (0.6 pu). In contrast, the X-type CSI necessitates over 4 pu L_{dc} within this range. Therefore, regarding the reduction of the DC inductance, the proposed inverter is suggested to operate in the m_a range of 0.8-1, requiring about 1.0 pu L_{dc}.

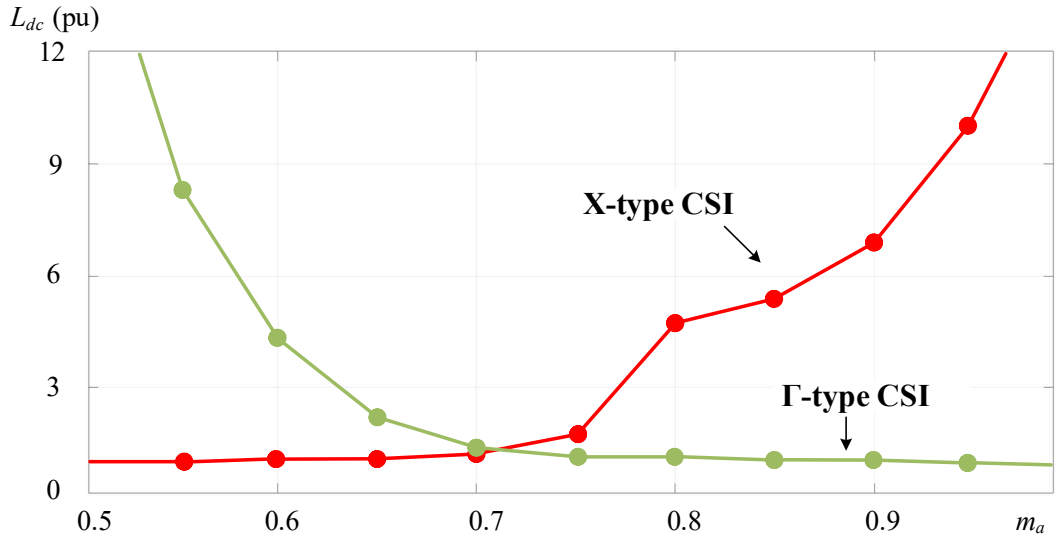


Fig. 3-11 Required input inductance at different modulation index.

LC filter size:

Same as other CSI-based topologies, the size of the LC filter is determined by the harmonic performance of i_w, and the transfer function of the filter can be shown as follows:

$$\frac{i_s(j\omega)}{i_w(j\omega)} = \frac{1}{(j\omega)^2 L_f C_f + (j\omega) R_f C_f + 1} \tag{3-14}$$

where R_f is the line resistance, i_s is the sinusoidal current after the filter, L_f is the line inductance, C_f is the filter capacitor, and w is the angular frequency.

Table 3-4 Minimum Filter Capacitor for the Proposed Converter

R=0.1 pu, L=0.1 pu									
m_a	0.55	0.6	0.65	0.7	0.75	0.8	0.85	0.9	0.95
i_w THD (%)	64.3	64.0	62.1	59.9	59.1	58.7	57.3	56.7	55.3
i_s THD (%)	5	5	5	5	5	5	5	5	5
C_{min} (pu)	0.251	0.250	0.243	0.233	0.230	0.225	0.223	0.219	0.215

The grid codes have requirements on both total harmonic distortion (THD) and individual harmonics of the grid-connected current. Therefore, the output filter should be sized so that all harmonics meet the grid codes (IEEE 519-2014) [53]. It is usually stipulated that the THD of i_s should be at most 5% for motor loads. Note that the LC filter design is a well-discussed topic [54], thus not detailed here.

In order to investigate the optimal operating range of the proposed inverter, the required C_f at different m_a is acquired, as shown in Table 3-4. With R_L and L_f both set to 0.1 pu, the required C_f is in the range of 0.215-0.251 pu. The required C_f decreases with m_a increasing, therefore the proposed inverter is suggested to be operated at high m_a ranges regarding the reduction of C_f.

In summary, the study of passive component sizes reveals differing trends for DC inductors and LC filters. As the modulation index increases, the proposed inverter requires smaller DC inductors and LC filters. This suggests that the Γ-type five-level CSI is better working at high modulation indexes.

3.2.7 Switch voltage stresses

Similar as X-type CSI, the DC side switches (S_7 and S_8) of the Γ-type CSI have different voltage stresses compared to the CSI side switches S_1-S_6. Table 3-5 lists the stress ratio of the DC side switch by the CSI side switch (indicating the number of switches needed in series for S_7). It is evident that the stress ratio decreases with higher m_a. At m_a=0.5, both S_7 and S_8 need a series-connection of 8 switches, as shown in Fig. 3-12. On the other hand, when the inverter is working at high modulation indexes ($0.8<m_a=1$), the voltage stresses of S_7 and S_8 are lower than the CSI switches, no series-connection is needed.

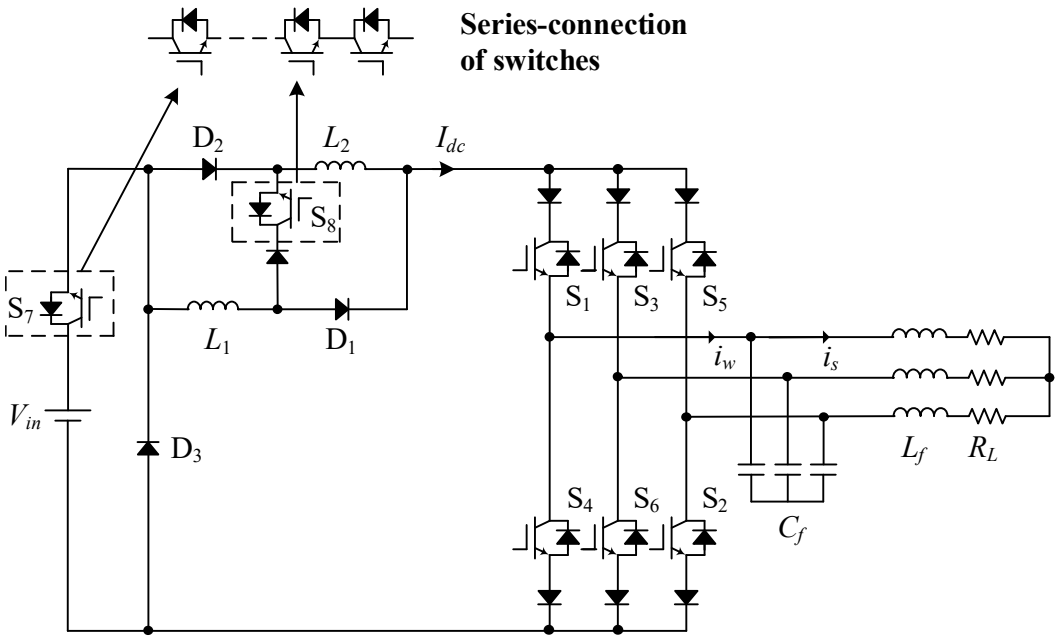


Fig. 3-12 Series-connection of switches for DC side switches.

Table 3-5 Voltage stresses of the switches

	V_{in} (pu)	Stress ratio S_7/S_1	Stress ratio S_8/S_1
m_a= 0.5	1	7.230	7.087
m_a = 0.6	1	2.611	2.274
m_a = 0.7	1	1.359	1.164
m_a = 0.8	1	0.857	0.738
m_a = 0.9	1	0.789	0.684
m_a = 1.0	1	0.769	0.564

In summary, the inverter is suggested to work at high modulation indexes to save the total switch count.

3.2.8 Efficiency

The losses in the proposed converter primarily arise from semiconductor devices and inductors. The efficiency study methodology is based on varying the DC inductor (L_{dc}) at different modulation indexes (m_a). This approach aims to identify the inverter's optimal operating point rather than to display the efficiency profile using the same L_{dc} across the entire operating range (different m_a).

The semiconductor losses, encompassing losses from IGBTs and diodes in the proposed converter, fall into conduction losses, switching losses, and off-state losses. The off-state losses can be disregarded due to the negligibly small leakage current during the device's off-state [55]. Consequently, only conduction losses and switching losses are considered in this section.

For conduction losses, the formulas are outlined in (3-15), where V_{CE0} denotes the IGBT on-state zero-current collector-emitter voltage, V_{F0} is the diode zero-current forward on-state voltage, R_C represents the collector-emitter on-state resistance, R_D is the diode on-state resistance, and I_{C_AVG}/I_{C_RMS} stands for the average/RMS value of the conduction current.

As for switching losses, the formulas are provided in (3-16), where E_{on} and E_{off} denote the turn-on and turn-off energy losses per pulse of the IGBT, f_{sw} is the switching frequency, V_{nom} and I_{nom} are the rated voltage and current of the IGBT, V and I represent the instantaneous values during switching, E_{rr} is the turn-off energy losses of the diode, f_{D_off} is the diode turn-off frequency, V_b is the reverse blocking voltage, and V_{b_nom} is the rated reverse blocking voltage.

$$\begin{cases} P_{con\_IGBT} = V_{CE0} * I_{C\_AVG} + R_C * I_{C\_RMS}^2 \\ P_{con\_Diode} = V_{F0} * I_{C\_AVG} + R_D * I_{C\_RMS}^2 \end{cases} \tag{3-15}$$

$$\begin{cases} P_{sw\_IGBT} = (E_{on} + E_{off}) * f_{sw} * \dfrac{V}{V_{nom}} * \dfrac{I}{I_{nom}} \\ P_{sw\_diode} = E_{rr} * f_{D\_off} * \dfrac{V_b}{V_{nom}} \end{cases} \tag{3-16}$$

Inductive losses encompass AC winding losses, DC winding losses, and core losses. The primary factors influencing inductive losses include winding diameter and length, average inductor current, fundamental frequency, and the type of inductor material [56-57]. In circuits related to CSC, where the mandatory DC inductor is typically substantial, DC winding losses often constitute the predominant portion of inductor losses. These losses are contingent on the inductor current and the DC resistance of the inductor (DCR). A larger L_{dc} results in a greater DCR, thereby leading to increased DC winding losses. In the proposed inverter and the preceding X-type CSI, both requiring a considerably larger L_{dc} than usual at certain modulation indexes, DC winding losses become even more crucial.

In general, power losses are influenced by both DC and AC inductors, the modulation scheme, switching frequency, conduction current, voltage stress on the switch, and switch characteristics, including saturation voltage, turn-on energy losses, and turn-off energy losses.

In order to investigate the best working range for the proposed inverter regarding the efficiency, the efficiency data is calculated and verified through PSIM. Fig. 3-13 shows the efficiency profiles of the proposed inverter compared with previous X-type CSI, maintaining an input voltage set at 3000 V. Power switches FZ250R65KE3 and power diodes DD250S65K3 are employed with the switching frequency of 4320Hz. With the same applied input voltage source, the efficiency of the proposed converter increases with m_a, surpassing that of the X-type at high modulation indexes (reaching the highest value at 92.2% when m_a = 1). The efficiency tends toward zero when m_a = 0.5 because the Γ-type CSI nears a critical point, predominantly operating in Mode 2 (solely inductor discharge mode), causing the required inductance value to approach infinity. This phenomenon is akin to the behavior of the X-type CSI when m_a = 1. At large m_a, the Γ-

type CSI requires significantly smaller L_{dc} compared to the X-type (0.8 pu/10 pu at m_a = 0.95), resulting in markedly lower dc winding losses. Despite the Γ-type CSI having a higher count of switches and diodes, its efficiency far surpasses that of the X-type, primarily due to this difference. Conversely, under small m_a, the efficiency of the Γ-type is diminished due to the substantial DC inductors resulting in increased DC winding losses.

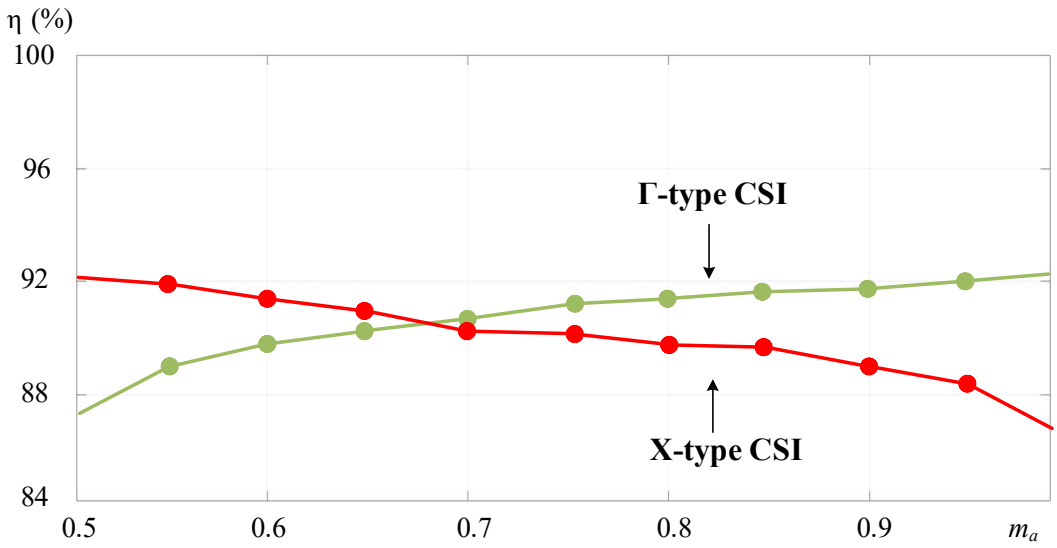


Fig. 3-13 Efficiency profile of the proposed inverter.

3.3 Performance verification

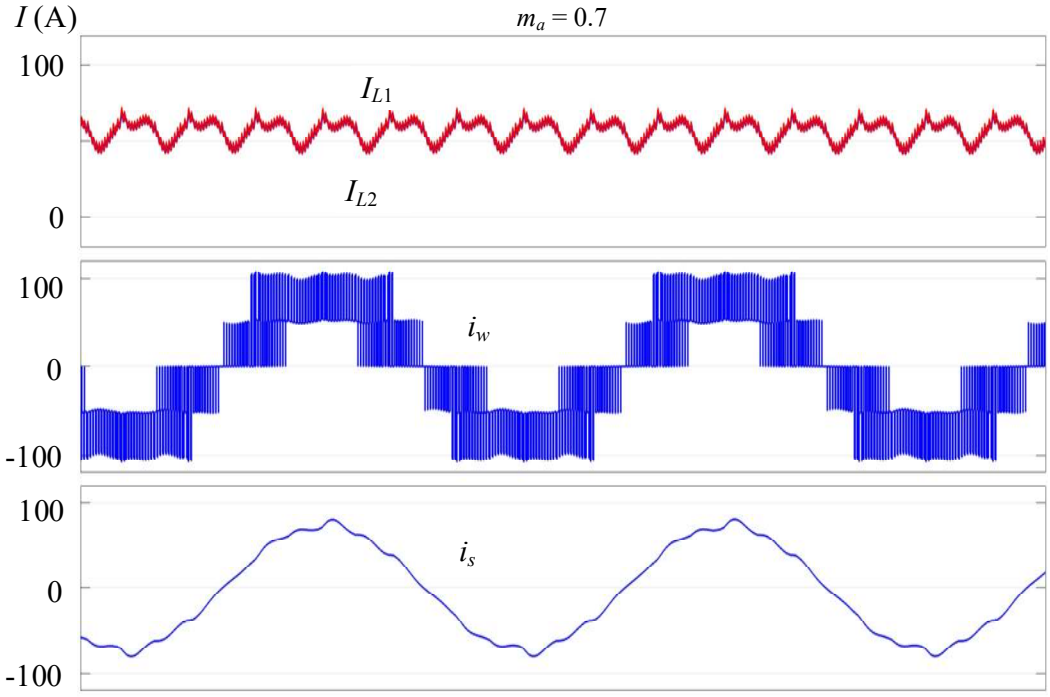
In this section, the performance of the proposed Γ-type CSI is verified through both simulation and experiment, where the parameters shown in Table 3-6. Two input inductors are intentionally set to different values (3/4 mH in simulation and 15/25 mH in experiment) to simulate the mismatches of DC inductors. In contrast to the parameters used in the X-type five-level CSI experiment, these input inductors are significantly reduced (10/12 mH and 50/60 mH for X-type), while keeping other parameters constant. Note that due to the minimum overlap achieved by the dSPACE controller used in the experiments is too large at 2e-5, some narrow pulses are filtered out, leading to

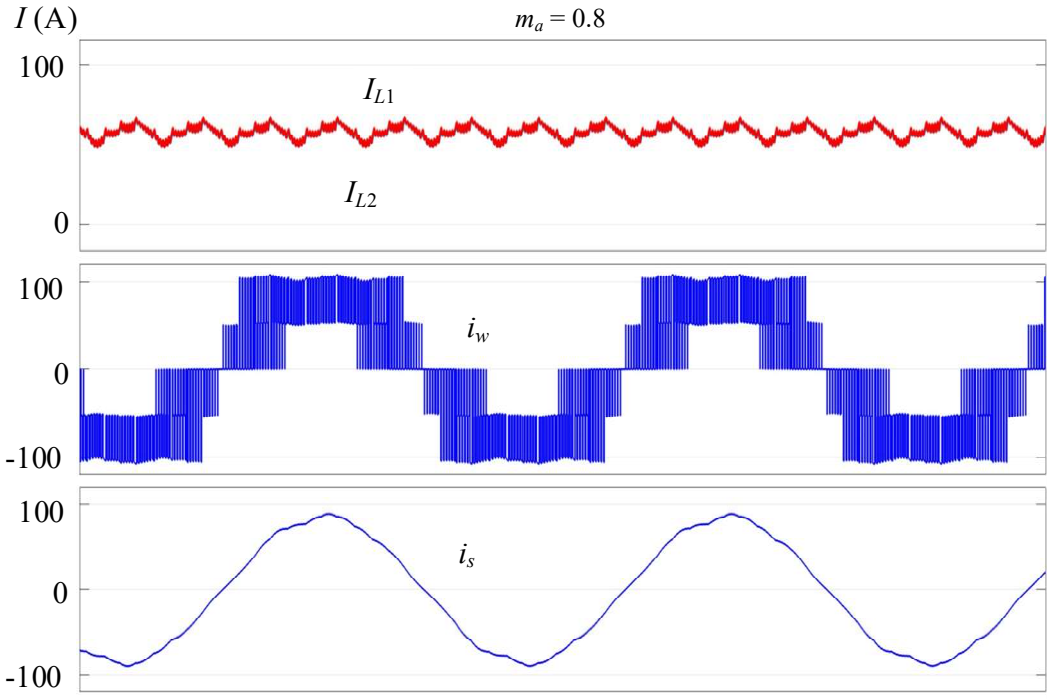
unexpectedly poor harmonics. To solve this issue while ensuring the experiment effectiveness, both the fundamental frequency (60 Hz reduced to 10 Hz) and the switching frequency (4320 Hz to 720 Hz) are reduced, while the frequency modulation index m_f remains the same before and after.

A simulation model is built for the proposed converter through MATLAB/Simulink. A 3000 V voltage source is employed in the simulation with a power rating of 30 kW-0.4 MW. Fig. 3-14 demonstrates the waveforms of the proposed inverter under the selected parameters with modulation index m_a set to 0.7, 0.8, and 0.9. As expected, the inductor currents i_{L1} and i_{L2} have a self-balancing capability, and the output PWM current i_w has five current levels (-100A, -50A, 0, 50A, 100A) with excellent symmetry. The load current i_s increases as m_a increases, with expected sinusoidal waves acquired. The current ripple of inductor current becomes larger when m_a increasing, indicating the larger L_{dc} required.

Table 3-6 Parameters in performance verification

Parameters	Simulation	Experiment
DC current	$I_{L1} = I_{L2} = 50$ A	$I_{L1} = I_{L2} = 5$ A
Fundamental frequency	60 Hz	10 Hz
Switching frequency	4320 Hz	720 Hz
Frequency modulation index m_f	72	72
Input inductance	3 mH, 4 mH	15 mH, 25 mH
Filter capacitance	55.7 uF	100 uF
Output load	10 Ω, 0.8 mH	1 Ω, 5 mH


I (A)
m_a = 0.7
100
I_{L1}
I_{L2}
0
100
i_w
0
-100
100
i_s
0
-100


I (A)
m_a = 0.8
100
I_{L1}
I_{L2}
0
100
i_w
0
-100
100
i_s
0
-100

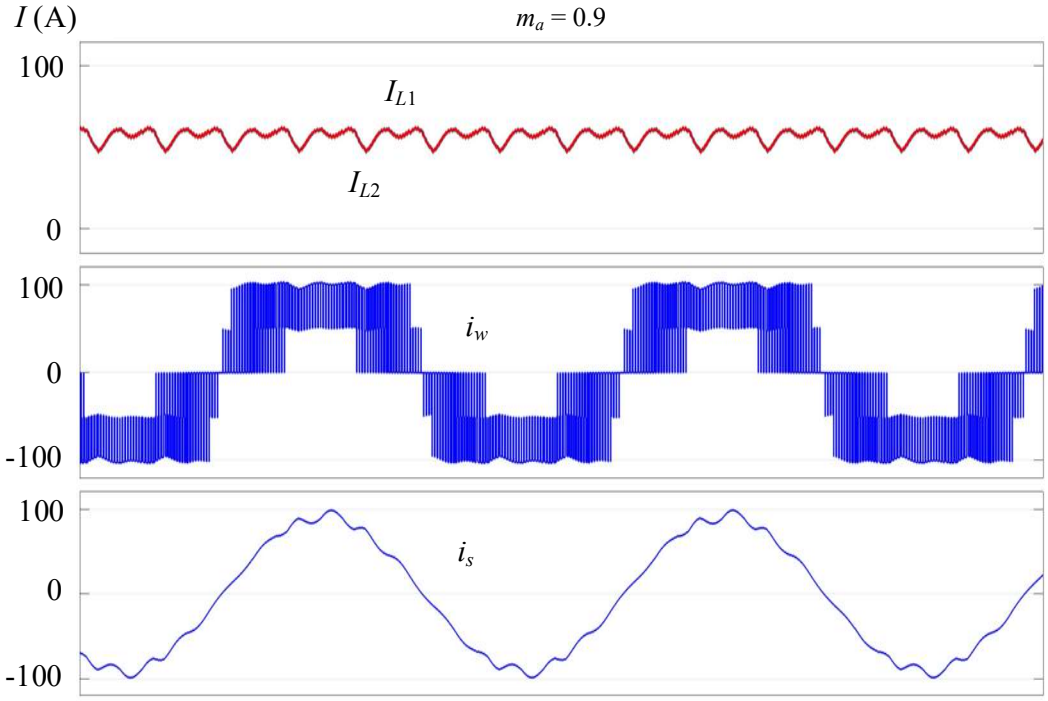


Fig. 3-14 Simulated waveforms of the proposed inverter.

The harmonic content of PWM current i_w for the inverter operating at a 60 Hz fundamental frequency with a 4320 Hz switching frequency is also shown in Fig. 3-14. The total harmonic distortion (THD) of i_w are 59.9%, 58.7%, and 56.7% for m_a set to 0.7, 0.8, and 0.9, respectively. The dominant harmonics are around 8640 Hz (144^{th}), with about 20-30% of the fundamental current. This is in line with the characteristic of the conventional SVM that the frequency of the dominant harmonic is about twice the switching frequency ($2m_f$) [1]. When m_a increased from 0.7 to 0.9, as we can see from Fig. 3-15, the percentage of fundamental for the dominant harmonics also reduces, this indicates the better harmonic performance at large modulation indexes.

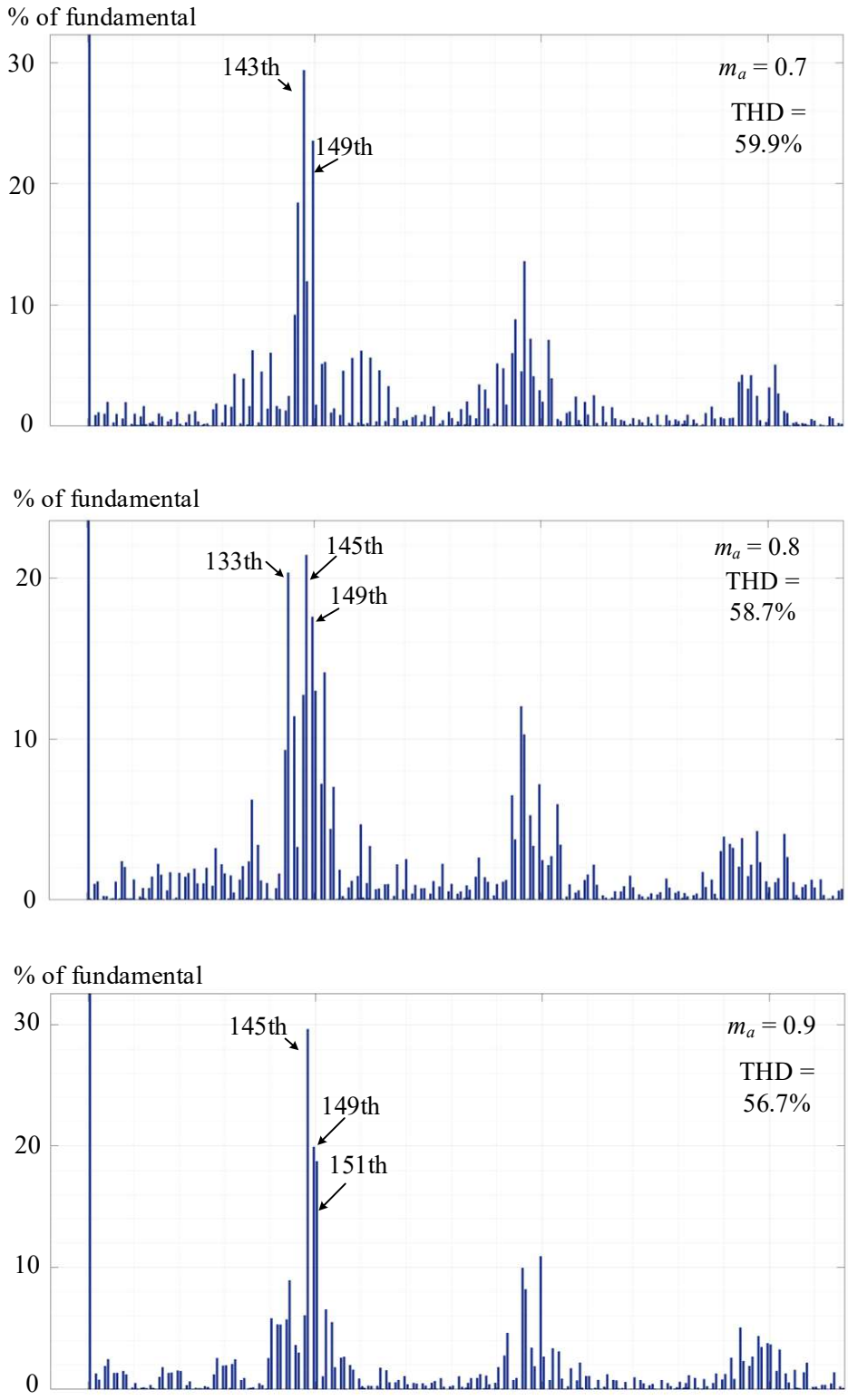


Fig. 3-15 Harmonic performance of the proposed inverter.

A down-scaled experiment is constructed using experimental setup. Fig. 3-16 shows the gating signals of the converter under m_a = 0.8, where g_1-g_6 represent the gating signals for CSI side switches S_1-S_6, and g_7 represents the gating signals for DC side switch S_7. As expected, the switching frequency of S_7 is much larger than those of S_1-S_6.

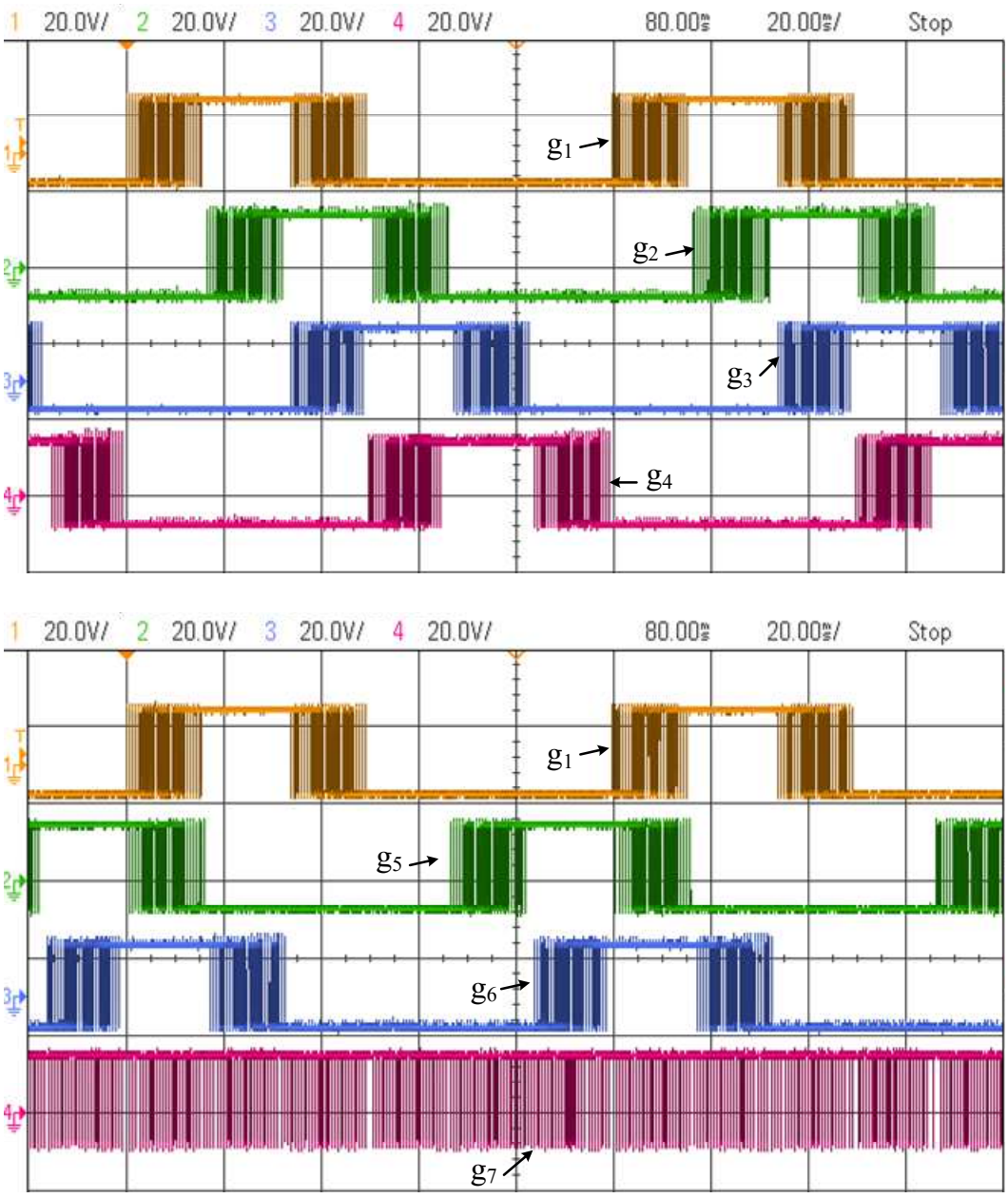
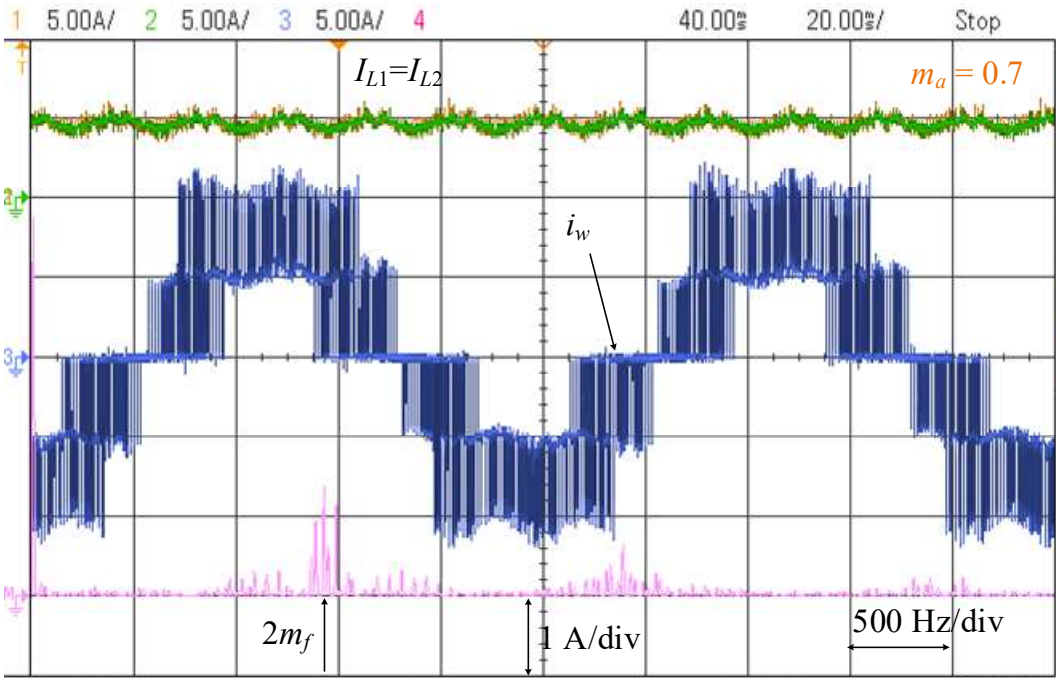
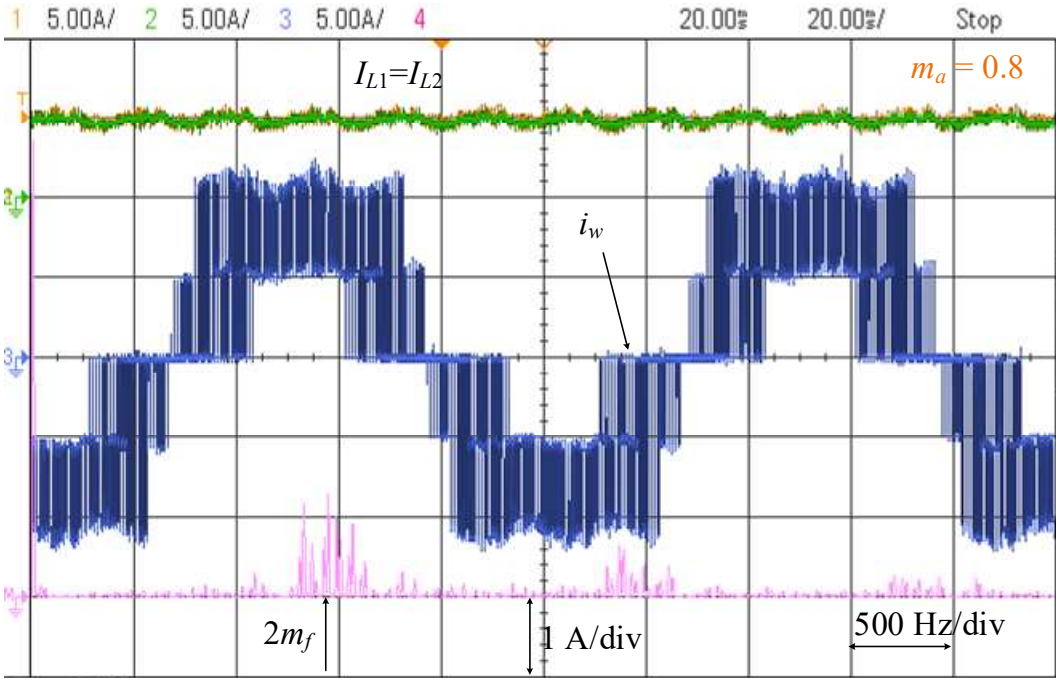


Fig. 3-16 Gating signals of the proposed inverter.


1 5.00A/ 2 5.00A/ 3 5.00A/ 4
40.00ms
20.00ms/
Stop
I_{L1}=I_{L2}
m_a = 0.7
i_w
$2m_f$
1 A/div
500 Hz/div


1 5.00A/ 2 5.00A/ 3 5.00A/ 4
20.00ms
20.00ms/
Stop
I_{L1}=I_{L2}
m_a = 0.8
i_w
$2m_f$
1 A/div
500 Hz/div

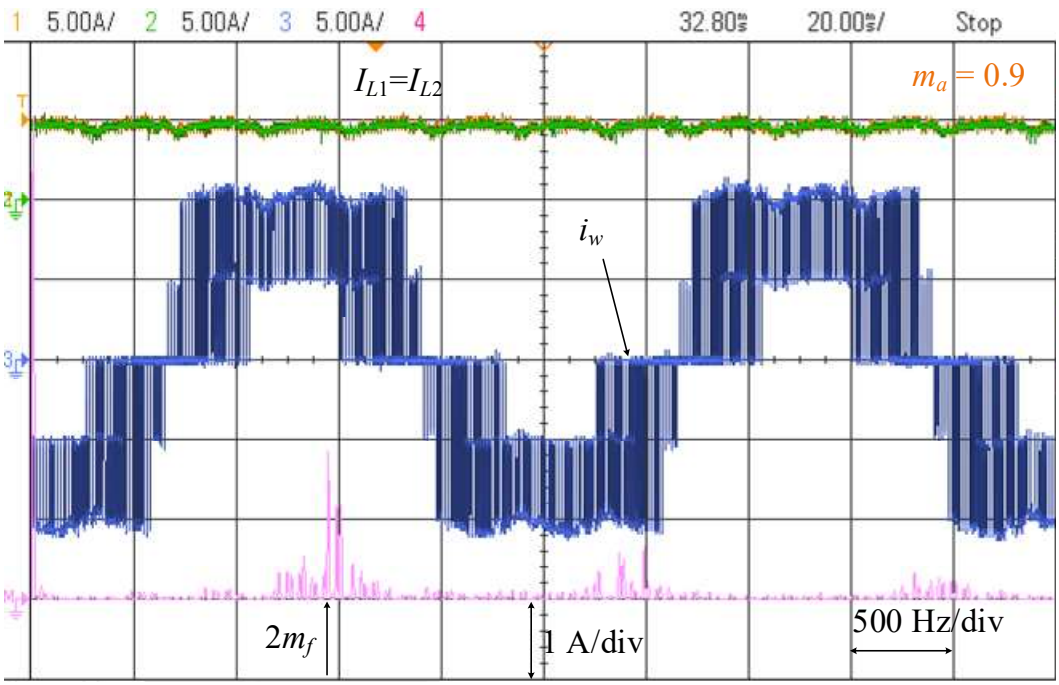


Fig. 3-17 Experimental waveforms under steady state.

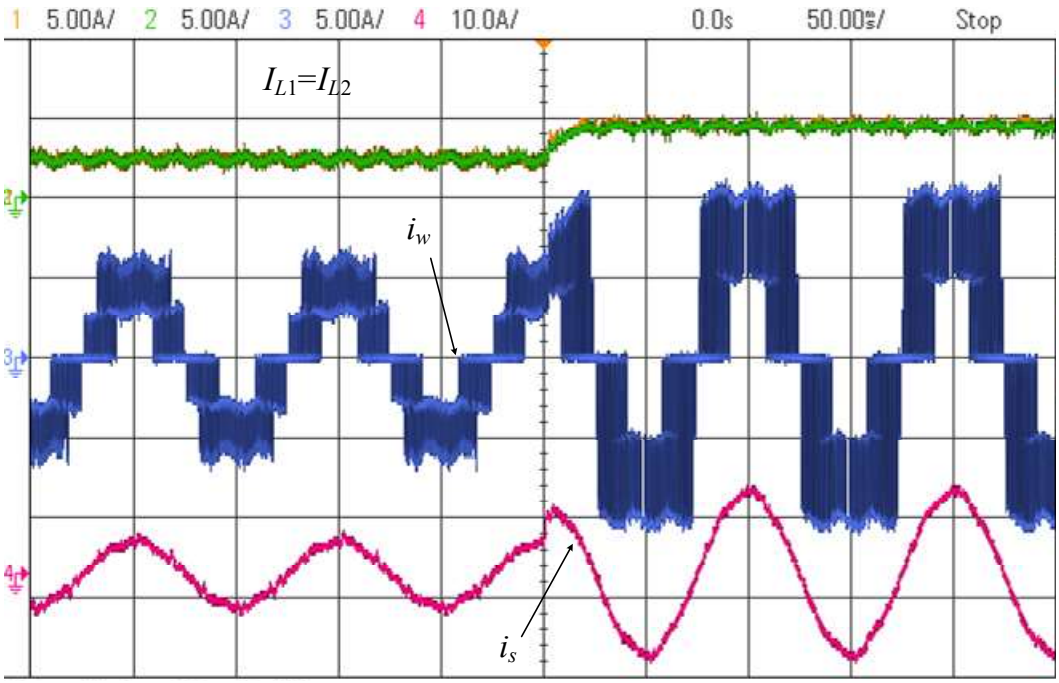


Fig. 3-17 Experimental waveforms under dynamic state.

Fig. 3-17 shows the waveforms under $I_{L1} = I_{L2} = 5$ A with different m_a. The current ripple of inductor current becomes larger when m_a increasing, indicating the larger L_{dc} required. The harmonic performance of i_w under different m_a is also shown in the figure, it has five current levels (-10A, -5A, 0, 5A, 10A) with excellent symmetry. The dominant harmonic orders are around $2m_f$ (around 1440Hz in the experiment).

Fig. 3-18 shows the waveforms of the proposed topology under dynamic state ($I_{L1} = I_{L2}$ increased from 3 A to 5 A). The inductor currents I_{L1} and I_{L2}, the PWM current i_w, and the sinusoidal output current i_s are obtained. It can be found that 5 levels at the output PWM current are generated; PWM current and sinusoidal output current are increased accordingly; I_{L1} and I_{L2} have the self-balancing capability in both cases.

3.4 Summary

In this chapter, a novel Γ-type five-level current source inverter (CSI) is introduced. Similar to the previously proposed X-type five-level CSI, it inherits the inductor current self-balancing feature, eliminating the need for complex balancing controls. This feature represents a significant advantage over conventional five-level CSI topologies.

Moreover, compared to the X-type CSI with similar inductor current self-balancing feature, the newly proposed Γ-type design demonstrates superior performance at high modulation indexes where the CSI-based topologies have better harmonic performance. It offers higher voltage gain, smaller DC inductors, and increased efficiency (due to less inductive losses). The chapter provides a comprehensive analysis and calculations covering inverter gain, passive components, transient voltage behavior, and efficiency. The effectiveness of the proposed inverter is validated through both simulations and laboratory-scale experiments.

However, the Γ-type CSI exhibits limited performance at low modulation indexes, where it has lower gain, requires larger DC inductors, and has reduced efficiency.

Additionally, due to the higher voltage stresses, the DC switches also require a series connection of switches, same as the previous proposed X-type five-level CSI. These drawbacks restrict the operation range of the Γ-type CSI.

Chapter 4 H-Type Five-Level Current Source Inverter[3]

In the previous chapter, a Γ-type five-level current source inverter was introduced. This inverter features self-balancing inductor currents, eliminating the need for complex and costly balancing control schemes. Compared to the X-type five-level CSI, the Γ-type offers higher gain and requires smaller DC inductors, resulting in better harmonic performance, cost savings, and increased efficiency. However, it performs poorly at low modulation indexes, with low gain and large DC inductors required. Additionally, due to large voltage stresses, the DC side switches need a series connection, which will add the total switch count, resulting in increased costs and losses.

This chapter introduces an H-type five-level CSI, which sets itself apart from conventional five-level CSIs by featuring self-balancing inductor currents without requiring additional balancing schemes. Compared to the previously proposed X- and Γ-type five-level CSIs, it requires significantly smaller DC inductors across the entire operational range, saving costs and increasing efficiency. Furthermore, the H-type CSI eliminates the need for a series connection of switches on the DC side. Therefore, the total switch count is reduced, further saving costs and improving the efficiency. The performance of this inverter has been validated through both simulations and laboratory-scale experiments.

4.1 Review of Γ-type five-level CSI

The Γ-type five-level CSI was introduced in the previous chapter. With its unique operation principle, it inherits the inductor current self-balancing feature, eliminating the need for additional current balancing control schemes.

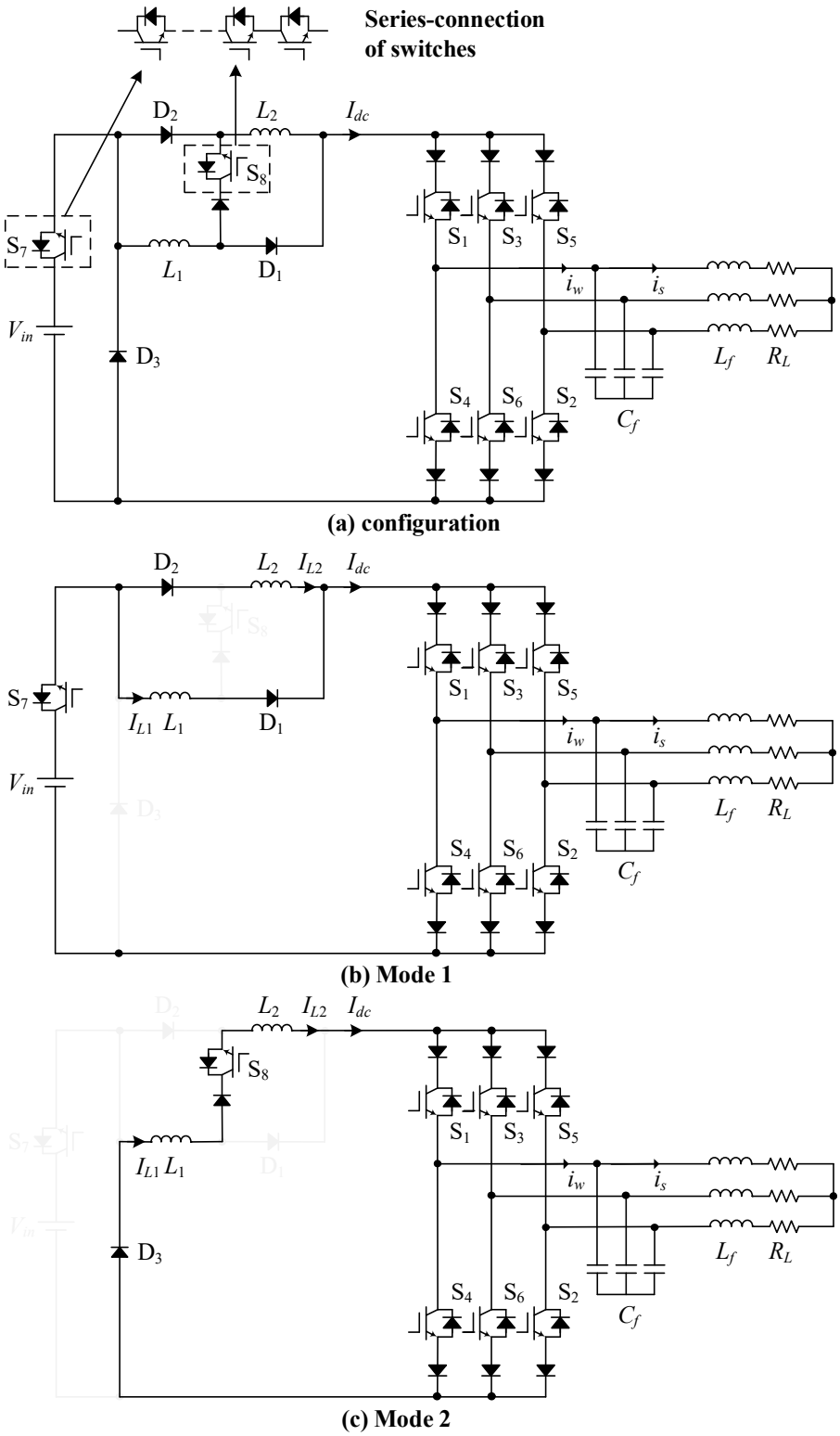


Fig. 4-1 Review of Γ-type five-level CSI.

Fig. 4-1 (a) illustrates the configuration of Γ-type five-level CSI, while Fig. 4-1 (b/c) depict the two operation modes, where inductors L_1 and L_2 are connected in parallel and series. In Mode 1, the DC current I_{dc} is twice the inductor current, and in Mode 2, it equals the inductor current. By alternating between these two modes, a five-level output can be achieved. Self-balancing of the inductor currents occurs in Mode 2, where L_1 and L_2 are connected in series, ensuring their currents are equal. Additionally, the gradual change in inductor voltages during mode transitions, facilitated by the additional diodes, prevents overvoltage.

The main improvement of the Γ-type five-level CSI compared to the X-type is its superior performance at high modulation indexes, where CSI-based topologies exhibit better harmonic performance. The Γ-type CSI offers high voltage gain and requires much smaller DC inductors, resulting in reduced cost, volume, and higher efficiency. This is because at high modulation indexes, X-type CSI is mostly working at the operation mode where the input source is disconnected, and the DC inductors are discharging and working as equivalent current sources. The Γ-type CSI, on the contrary, is working mostly at Mode 1 (Fig. 4-1 (b)) where the input source is connected and charging the inductors.

However, the Γ-type CSI shows limited performance at low modulation indexes, with lower gain, larger DC inductors, and reduced efficiency. Additionally, due to higher voltage stresses, the DC switches require a series connection of switches, as shown in Fig. 4-1 (a). These drawbacks restrict the operational range of the Γ-type CSI.

4.2 H-type five-level current source inverter

This section introduces a novel H-type five-level current source inverter. Unlike conventional five-level CSIs that suffer from imbalanced currents, the proposed inverter achieves self-balancing of inductor currents, eliminating the need for additional balancing controls. Compared to the previously proposed X- and Γ-type CSIs, this new inverter not

only retains the inductor current self-balancing feature but also offers improved performance by using smaller DC inductors. This results in a more compact and lightweight design, higher efficiency, and lower costs. Additionally, the series connection of DC switches is no longer needed, further reducing costs and losses.

4.2.1 Inverter structure

Fig. 4-2 illustrates the configuration of the proposed Γ-type five-level CSI.

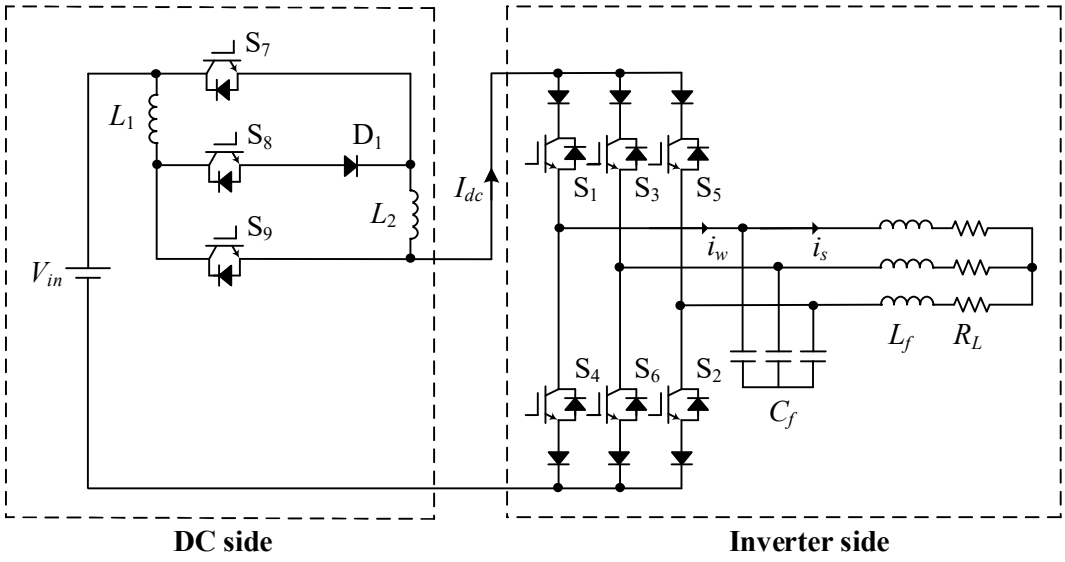


Fig. 4-2 Proposed H-type five-level CSI.

On the inverter side, the same single six-switch CSI as X- and Γ-type is used, featuring the following components:

1) Switching devices: S_1 to S_6 are power switches with reverse voltage blocking capabilities, such as gate turn-Off thyristors (GTO), symmetrical gate commutated thyristors (SGCT), or insulated gate bipolar transistors (IGBT)/metal-oxide-semiconductor field-effect transistors (MOSFET) in series with a diode.

2) Three-phase capacitor: Located at the inverter output, this capacitor C_f aids in the commutation of the switching devices. For example, when switch S_1 is turned off, the inverter PWM current i_w drops to zero rapidly. The capacitor provides a path for the energy trapped in the phase-A load inductance, preventing high voltage spikes that could damage the switching devices.

3) LC filter: The combination of C_f and load inductance L_f together form an LC filter. This filter removes most of the harmonics from the PWM current i_w, ensuring the sinusoidal current i_s meets specific output requirements (e.g. the current harmonics distortion criteria for the design of electrical systems in IEEE 519-2014).

4) Inverter output: As an example, the output is connected to an AC motor in Fig. 3-2, represented by load inductance L_f and load resistance R_L. Additionally, the output can be connected with grid, with power factor control being required.

On the DC side, a different DC-DC converter is used, featuring the following components:

1) Input source: The proposed inverter uses a single voltage source, akin to other topologies discussed in Section 1.2.1, the X-type five-level CSI in Section 2.2.1, and the Γ-type five-level CSI in Section 3.2.1.

2) DC inductors: The inductors L_1 and L_2 make the DC current I_{dc} smooth and continuous, while also facilitates the inverter's operational principles

3) Additional components: S_7-S_9 can be an IGBT or MOSFET, and D_1 is a power diode. These components are included to support the unique operations of the inverter.

4.2.2 Five-level output generation

Fig. 4-3 illustrates the two operation modes of the proposed inverter:

Mode 1: Illustrated in Fig. 4-3 (a), where S_7 and S_9 are activated while S_8 is deactivated. Identical inductors L_1 and L_2 are connected in parallel through S_9 and S_7, respectively. The currents in both inductors (I_{L1} and I_{L2}) equate to $0.5I_{dc}$. This configuration generates an output PWM current with three levels: $2I_L$, 0, and $-2I_L$.

Mode 2: Shown in Fig. 4-3 (b), involving S_7 and S_9 being turned off while S_8 is turned on. L_1 and L_2 are linked in parallel through S_8 and D_1, forcing the inductor currents to match and align with I_{dc}. Consequently, the CSI output produces I_L, 0, and $-I_L$.

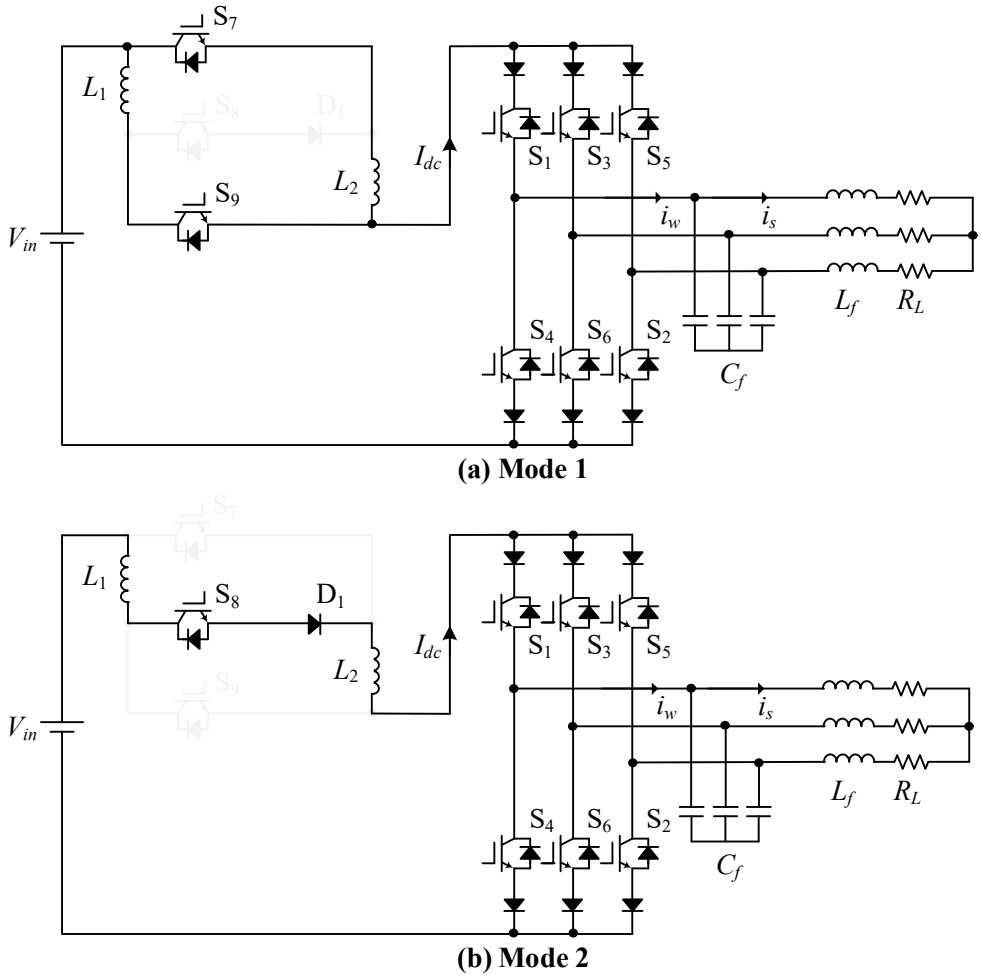


Fig. 4-3 Operation modes of the H-type five-level CSI.

Alternating between these two operation modes enables the attainment of a five-level output. For instance, activating switches S_1, S_2, and S_8 generates output currents i_{wa}, i_{wb},

and i_{wc} as I_L, 0, and -I_L, respectively. Meanwhile, when switches S_1, S_2, S_7, and S_9 are activated, i_{wa}, i_{wb}, and i_{wc} become $2I_L$, 0, and -$2I_L$, respectively.

4.2.3 Modulation design

A similar SVM-based scheme (designed in Section 2.2.3 and Section 3.2.3) can be used here with different switching states of the H-type five-level CSI applied:

Switching states: According to the two operation modes of the proposed inverter shown in the last section, the switching states and corresponding output PWM currents are shown in Table 4-1. There are a total of 18 switching states, including active and zero switching states. Similar to existing CSIs, the modulation scheme for the proposed CSI is not unique. Any CSI modulation scheme can be designed as long as the switching states in Table 4-1 are satisfied.

Table 4-1 Space vectors of the proposed inverter

Space vectors		On-state switches	Output currents		
			$i_{w\mathrm{A}}$	$i_{w\mathrm{B}}$	$i_{w\mathrm{C}}$
Large vectors	I_{L1}	{1279}	$2I_L$	0	-$2I_L$
	I_{L2}	{2379}	0	$2I_L$	-$2I_L$
	I_{L3}	{3479}	-$2I_L$	$2I_L$	0
	I_{L4}	{4579}	-$2I_L$	0	$2I_L$
	I_{L5}	{5679}	0	-$2I_L$	$2I_L$
	I_{L6}	{6179}	$2I_L$	-$2I_L$	0
Small vectors	I_{S1}	{128}	I_L	0	-I_L
	I_{S2}	{238}	0	I_L	-I_L
	I_{S3}	{348}	-I_L	I_L	0
	I_{S4}	{458}	-I_L	0	I_L
	I_{S5}	{568}	0	-I_L	I_L
	I_{S6}	{618}	I_L	-I_L	0
Zero Vectors	I_0	{148}{1479}	0	0	0
		{257}{2579}			
		{367}{3679}			

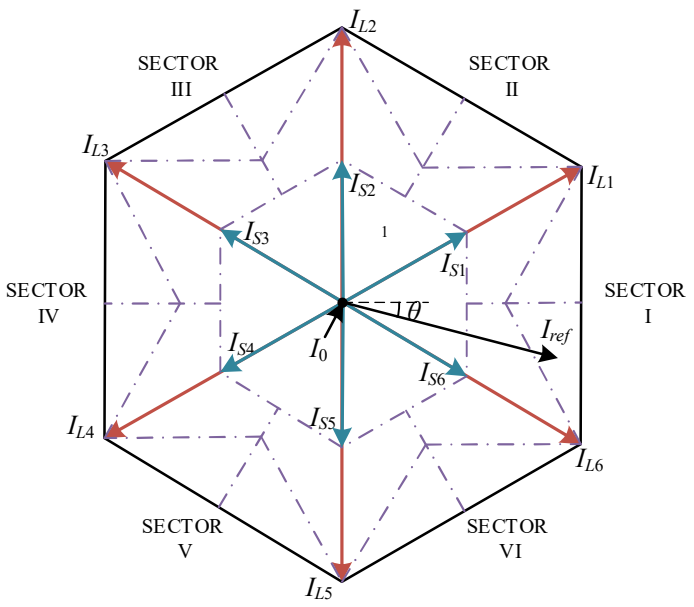


Fig. 4-4 Space vector diagrams of the proposed inverter.

Space vectors: The resultant space vectors for the switching states are shown in the space vector diagram in Fig. 4-4, where I_{L1} to I_{L6} are the large vectors, I_{S1} to I_{S6} are the small vectors, and I_0 is the zero vector. The large/small vectors form a hexagon with six equal sectors, while the zero vector lies at the center. Note that the transformation from switching states to space vectors is the same as the conventional CSIs, thus not repeated here, please refer to [1] for such details. To facilitate the dwell time calculation, the space vector diagram can be divided into six triangular sectors (I to VI), each of which can be further divided into five subsectors (1 to 5), as shown in Fig. 4-4. Eventually, there are 30 subsectors in total.

Dwell time calculation: The reference vector I_{ref} is synthesized by three vectors. Depending on the different sectors and subsectors I_{ref} falls into, the synthesized scheme is listed below:

1) one zero vector and two small vectors in Subsector 1.

2) two small vectors and one large vector in Subsector 2 and 4.

3) one small vector and two large vectors in Subsector 3 and 5.

For example, with I_{ref} falling into Subsector 3 in Sector I, as shown in Fig. 4-5, it is synthesized by one small vector (I_{S6}) and two large vectors (I_{L6} and I_{L1}).

By converting the three-phase (abc) current vectors into two-phase ($\alpha\beta$) based on the ampere-second balancing principle, the relationships between the vectors and dwell times can be derived:

$$\begin{cases} I_{ref}T_s = I_{ap}T_p + I_{aq}T_q + I_{ar}T_r \\ T_s = T_p + T_q + T_r \end{cases} \tag{4-1}$$

where the subscript a represents small (S), large (L), or zero (0) vectors; T_s the sampling period; T_p, T_q, and T_r represent the dwell times for the respective vectors.

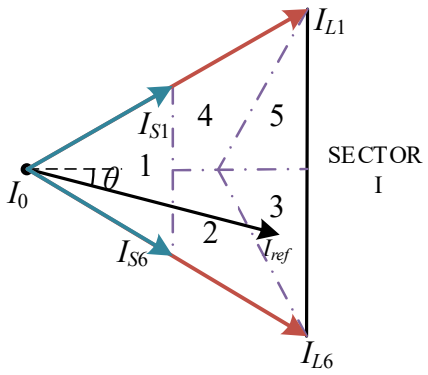


Fig. 4-5 Space vector diagrams in Sector 1.

Applying the example in Fig. 4-5 when I_{ref} falling into Subsector 3 in Sector I, equation (2-1) can be simplified as:

$$\begin{cases} I_{ref}T_s = I_{L1}T_4 + I_{S6}T_1 + I_{L6}T_2 \\ T_s = T_4 + T_1 + T_2 \end{cases} \tag{4-2}$$

Following the above procedure, each selected vector's dwell times under different subsectors and sectors can be calculated and summarized in Table 4-2, where m_a is the modulation index.

Table 4-2 Vector Dwell Times of Different Subsectors

Subsector	Vector	Dwell time	Dwell time calculation
1	I_0	T_0	$T_s - T_1 - T_3$
	I_{S6}	T_1	$(\cos\theta - \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L6}	T_2	0
	I_{S1}	T_3	$(\cos\theta + \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L1}	T_4	0
2	I_0	T_0	0
	I_{S6}	T_1	$T_s - T_2 - T_3$
	I_{L6}	T_2	$(2 * \cos\theta * m_a - 1) * T_s$
	I_{S1}	T_3	$(\cos\theta + \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L1}	T_4	0
3	I_0	T_0	0
	I_{S6}	T_1	$T_s - T_2 - T_4$
	I_{L6}	T_2	$((1.5 * \cos\theta - 0.5 * \sqrt{3}\sin\theta) * m_a - 1) * T_s$
	I_{S1}	T_3	0
	I_{L1}	T_4	$0.5 * (\cos\theta + \sqrt{3}\sin\theta) * T_s * m_a$
4	I_0	T_0	0
	I_{S6}	T_1	$(\cos\theta - \sqrt{3}\sin\theta) * T_s * m_a$
	I_{L6}	T_2	0
	I_{S1}	T_3	$T_s - T_1 - T_4$
	I_{L1}	T_4	$(2 * \cos\theta * m_a - 1) * T_s$
5	I_0	T_0	0
	I_{S6}	T_1	0
	I_{L6}	T_2	$0.5 * (\cos\theta - \sqrt{3}\sin\theta) * T_s * m_a$
	I_{S1}	T_3	$T_s - T_2 - T_4$
	I_{L1}	T_4	$((1.5 * \cos\theta + 0.5 * \sqrt{3}\sin\theta) * m_a - 1) * T_s$

Sequence sequences: Similar to the space vector modulation for the conventional CSI, the switching sequence design for the X-type CSI should also satisfy the following two requirements for the minimization of switching frequencies [1]:

1) The transition from one switching state to the next involves only two switches, one being switches on and one being switches off.

2) The transition for I_{ref} moving from one sector/subsector to the next requires the minimum number of switchings.

Table 4-3 Sequence design of the proposed inverter

	Sequence	Subsector 1	Subsector 2	Subsector 4	Subsector 1
$0.5 < m_a < 0.577$	SQ1	I_{S1}-I_0-I_{S6}	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{S1}-I_{L1}	I_{S1}-I_0-I_{S6}
	SQ2	I_{S1}-I_0-I_{S6}	I_{L6}-I_{S6}-I_{S1}	I_{L1}-I_{S1}-I_{S6}	I_{S1}-I_0-I_{S6}
	SQ3	I_{S1}-I_{S6}-I_0	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{S1}-I_{L1}	I_{S1}-I_{S6}-I_0
	SQ4	I_{S6}-I_{S1}-I_0	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{S1}-I_{L1}	I_{S6}-I_{S1}-I_0
	Sequence	Subsector 2	Subsector 3	Subsector 5	Subsector 4
$0.577 < m_a < 0.667$	SQ5	I_{L6}-I_{S6}-I_{S1}	N/A	N/A	I_{S6}-I_{S1}-I_{L1}
	SQ6	I_{L6}-I_{S6}-I_{S1}	N/A	N/A	I_{L1}-I_{S1}-I_{S6}
	SQ7	I_{S1}-I_{S6}-I_{L6}	N/A	N/A	I_{S6}-I_{S1}-I_{L1}
	SQ8	I_{S1}-I_{S6}-I_{L6}	N/A	N/A	I_{L1}-I_{S1}-I_{S6}
$m_a > 0.667$	SQ9	I_{L6}-I_{S6}-I_{S1}	I_{S6}-I_{L6}-I_{L1}	I_{L6}-I_{L1}-I_{S1}	I_{S6}-I_{S1}-I_{L1}
	SQ10	I_{L6}-I_{S6}-I_{S1}	I_{S6}-I_{L6}-I_{L1}	I_{S1}-I_{L1}-I_{L6}	I_{S6}-I_{S1}-I_{L1}
	SQ11	I_{L6}-I_{S6}-I_{S1}	I_{L1}-I_{L6}-I_{S6}	I_{L6}-I_{L1}-I_{S1}	I_{L1}-I_{S1}-I_{S6}
	SQ12	I_{L6}-I_{S6}-I_{S1}	I_{L1}-I_{L6}-I_{S6}	I_{S1}-I_{L1}-I_{L6}	I_{L1}-I_{S1}-I_{S6}
	SQ13	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{L6}-I_{L1}	I_{L6}-I_{L1}-I_{S1}	I_{S6}-I_{S1}-I_{L1}
	SQ14	I_{S1}-I_{S6}-I_{L6}	I_{S6}-I_{L6}-I_{L1}	I_{S1}-I_{L1}-I_{L6}	I_{S6}-I_{S1}-I_{L1}
	SQ15	I_{S1}-I_{S6}-I_{L6}	I_{L1}-I_{L6}-I_{S6}	I_{L6}-I_{L1}-I_{S1}	I_{L1}-I_{S1}-I_{S6}
	SQ16	I_{S1}-I_{S6}-I_{L6}	I_{L1}-I_{L6}-I_{S6}	I_{S1}-I_{L1}-I_{L6}	I_{L1}-I_{S1}-I_{S6}

In the X-type five-level CSI, varying m_a values result in I_{ref} traversing different subsectors, as illustrated in Fig. 2. The scenarios are as follows (in respective sector):

Case 1: for $m_a < 0.5$, I_{ref} stays in Subsector 1.

Case 2: for $0.5 < m_a < 0.577$, I_{ref} follows the path: Subsector 1 - Subsector 2 - Subsector 4 - Subsector 1.

Case 3: for $0.577 < m_a < 0.667$, I_{ref} follows the path: Subsector 2 - Subsector 4.

Case 4: for $0.667 < m_a < 1$, I_{ref} follows the path: Subsector 2 - Subsector 3 - Subsector 5 - Subsector 4.

When $m_a < 0.5$ (case 1), the X-type functions as a three-level CSI, therefore, this case will not be discussed. In the design, m_a should always be larger than 0.5. Table 4-3 presents the switching sequences meeting the specified design criteria (mentioned above) in case 2, case 3, and case 4.

4.2.4 Self-balancing mechanism

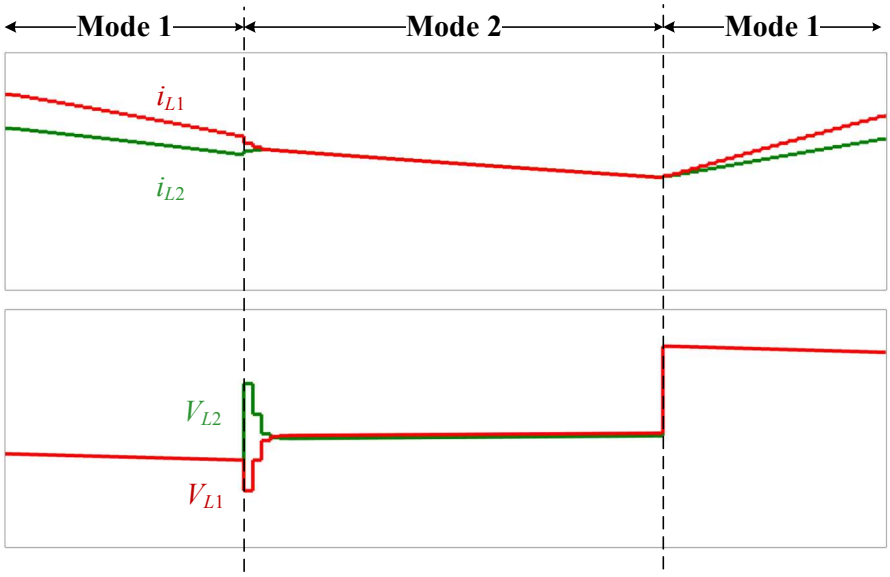


Fig. 4-6 Transient waveforms of the proposed inverter.

In mode 1, inductors L_1 and L_2 are connected in parallel. Due to factors such as the manufacturing tolerance in DC inductors mentioned in the introduction, the two inductors cannot be identical in practice, which will eventually lead to the difference between the inductor currents I_{L1} and I_{L2}. In mode 2, due to the series-connection, i_{L1} and i_{L2} keep identical, and the self-balancing feature is insured. V_{L1} and V_{L2} are different due to inductor mismatch. The transient waveforms of the inductor voltages (V_{L1} and V_{L2}) and currents (i_{L1} and i_{L2}) are shown in Fig. 4-6.

During the mode transition, since the switching between the operation modes is almost instantaneous (switches turn-on/turn-off time t_{on}/t_{off}), the instantaneous current change in the inductor may cause overvoltage on the inductor, which is also a common problem in DC-DC converters. However, due to the existence of freewheeling diodes in S_7 and S_9 (S_7 and S_9 are switches with a forward voltage blocking such as IGBT, MOSFET, etc.), the overvoltage problem does not occur in the proposed inverter. Fig. 4-7 shows the transient equivalent circuit when switching from mode 1 to mode 2. When inductor currents $I_{L1}>I_{L2}$, the voltage at the marked point $V_b>V_a$ in Fig. 4-7, the freewheeling diode of S_7 will then be forward-biased and turned on. As a result, I_{L1} decreases gradually until it equals I_{L2}. When inductor currents $I_{L1}<I_{L2}$, similarly, the freewheeling diode of S_9 will then be forward-biased and turned on. As a result, I_{L2} decreases gradually until it equals I_{L1}.

In summary, in practice where parameter mismatch exists, the proposed inverter has the inductor current self-balancing feature and no overvoltage due to the gradual change of the currents. Neither extra overvoltage clamping schemes nor overrated devices are needed.

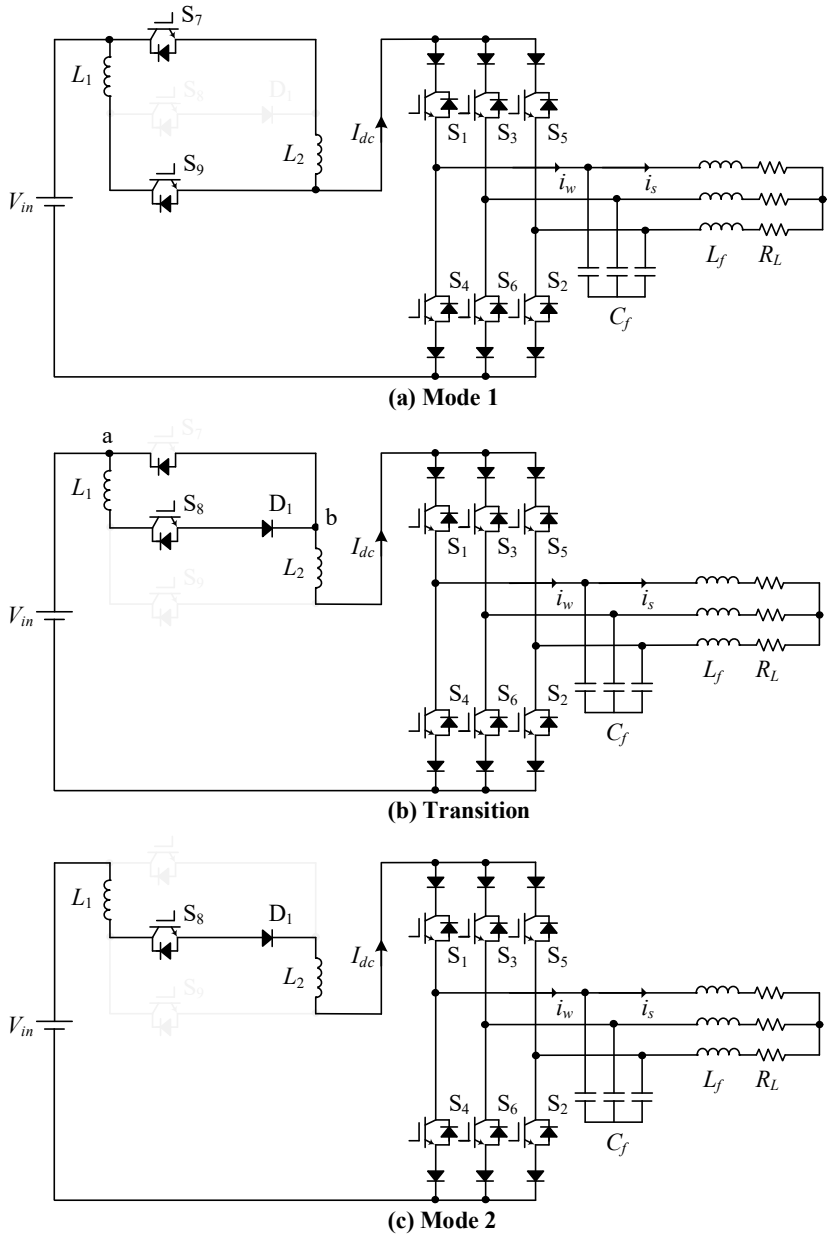


Fig. 4-7 Transient states of the proposed inverter.

4.2.5 Passive component sizes

The size of the passive components significantly impacts the cost and volume of the CSI system. This section addresses this aspect by examining the sizes of the DC inductor and the LC filter:

DC inductor size:

L_1 and L_2, the DC inductors in the proposed inverter, are the key components maintaining the operation modes of the proposed converter. At the same time, the size of the DC inductors also determines DC current ripple. For keeping the DC current ripple less than a certain value (12%, for example) to maintain the continuity and smoothness of the DC current, the minimum value of the dc inductors is shown in (4-3):

$$L_1 = L_2 = \frac{L_{total}}{2} = \frac{1}{2} * \frac{(V_{in} - V_{dc})\Delta t}{12\% I_L} \tag{4-3}$$

$$\begin{cases} [S_6, S_1] : V_{dc} = V_{ab} \\ [S_1, S_2] : V_{dc} = V_{ac} \\ [S_2, S_3] : V_{dc} = V_{bc} \\ [S_3, S_4] : V_{dc} = V_{ba} \\ [S_4, S_5] : V_{dc} = V_{ca} \\ [S_5, S_6] : V_{dc} = V_{cb} \end{cases} \tag{4-4}$$

where V_{in} represents the input voltage, V_{dc} signifies the DC voltage before the CSI module, and Δt is the dwell times shown in Table 4-2.

Fig. 4-8 illustrates the minimum L_{dc} for the five-level CSIs operating under identical conditions (utilizing the same modulation scheme). Same to the conventional five-level CSIs [1], the L_{dc} required by the H-type CSI exhibits a linear increase with m_a, reaching a peak of 0.6 pu at m_a = 1. In comparison, the X-type CSI requires a lot more at large modulation indexes (more than 10 pu at m_a = 0.95), and the Γ-type CSI requires a lot more at small modulation indexes (around 10 pu at m_a = 0.55). This disparity arises since the H-type CSI remains connected to the input source continually, lacking the X/Γ-type inductors to discharge and function as independent current sources during specific operation modes.

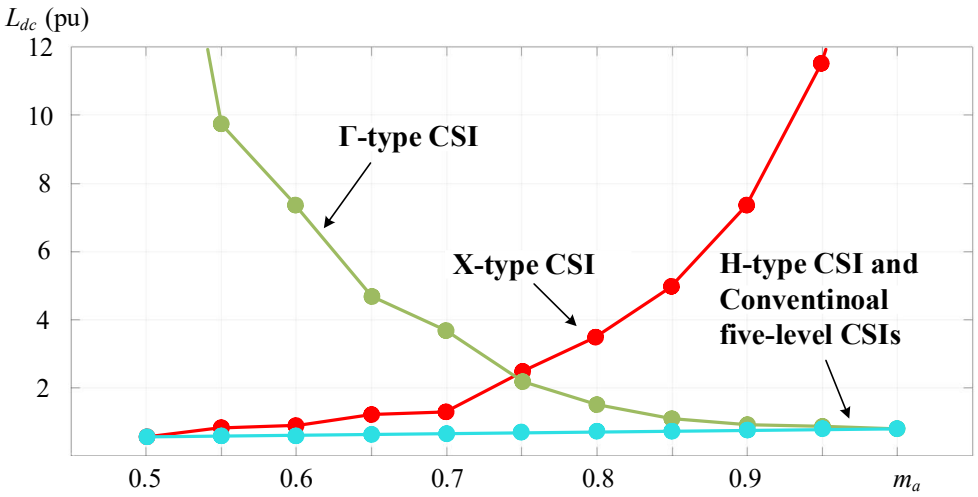


Fig. 4-8 Required input inductance at different modulation index.

The inductance reduction is achieved through the unique operation of Mode 2 in the proposed H-type CSI, where the DC inductors are connected to and powered by the input source. In contrast, the DC inductors of both X-type and Γ-type CSIs in Mode 2 are disconnected from the input source, resulting in the need for larger DC inductances. On the other hand, this is also the reason that the proposed H-type CSI has approximately the same DC inductance requirements as the conventional CSIs where the DC inductors are always connected to and fed by the input source in all operation modes.

The X-type CSI is taken as an example to illustrate the mechanism of the reduced DC inductor of the proposed H-type CSI. The general equation calculating the minimum required L_{dc} for CSI is shown in (4-3). Assuming both the X-type and the proposed H-type inverters have the same input, using the same modulation scheme, and working at the same modulation index m_a, Δt and V_{in} should be identical for both topologies. Therefore, in (4-3), there are two parts left to focus on, the I_{dc} in the denominator and the V_{dc} in the numerator.

I_{dc} in the denominator: Neglecting losses, I_{dc} is expressed as below, where V_{LL} is the output line to line voltage, R is the load resistance, and φ is the power factor angle.

$$I_{dc} = \frac{V_{LL}\cos\varphi}{\sqrt{6}m_a R} \tag{4-5}$$

The voltage gain of the X-type CSI is expressed as:

$$G_{v\_X-type} = \frac{V_{LL}}{V_{in}} = \frac{2 - \frac{6m_a}{\pi}}{\sqrt{6}m_a \cos\varphi} \tag{4-6}$$

The voltage gain of the H-type CSI is the same as that of traditional CSIs, as shown below:

$$G_{v\_H-type} = \frac{V_{LL}}{V_{in}} = \frac{1}{\sqrt{6}m_a \cos\varphi} \tag{4-7}$$

It becomes apparent that the voltage gain of the two topologies deviates by the factor $2\text{-}6m_a/\pi$. Substituting this value into (4-5) reveals that the discrepancy in I_{dc} between the two topologies fluctuates with m_a and peaks when m_a equals 1, with the I_{dc} in H-type approximately much greater than that in X-type. Since I_{dc} is in the denominator, this will cause the L_{dc} of H-type CSI to be smaller.

V_{dc} in the numerator: In CSIs, the voltage V_{dc} is clamped by the output line to line voltage (4-4). Therefore, the V_{dc} ratio between the H-type and X-type CSI is the same as their respective V_{LL} ratios. The voltage gains of respective inverters are given by (4-6) and (4-7), showing that the V_{dc} of H-type CSI is larger, and V_{in}-V_{dc} is smaller under fixed input V_{in}. Finally, Since V_{in}-V_{dc} is in the numerator, this will cause the L_{dc} of H-type CSI to be smaller.

In summary, the H-type CSI needs a smaller L_{dc} compared to X-type CSI. Moreover, as the m_a value increases, the difference of respective L_{dc} increases, reaching the peak at m_a = 1. A similar comparison between Γ-type and H-type can be conducted using the same methodology and will not be repeated.

LC filter size:

Same as other CSI-based topologies, the size of the LC filter is determined by the harmonic performance of i_w, and the transfer function of the filter can be shown as follows:

$$\frac{i_s(j\omega)}{i_w(j\omega)} = \frac{1}{(j\omega)^2 L_f C_f + (j\omega) R_f C_f + 1} \tag{4-8}$$

where R_f is the line resistance, i_s is the sinusoidal current after the filter, L_f is the line inductance, C_f is the filter capacitor, and w is the angular frequency.

The grid codes have requirements on both total harmonic distortion (THD) and individual harmonics of the grid-connected current. Therefore, the output filter should be sized so that all harmonics meet the grid codes (IEEE 519-2014) [53]. It is usually stipulated that the THD of i_s should be at most 5% for motor loads. Note that the LC filter design is a well-discussed topic [54], thus not detailed here.

In order to investigate the optimal operating range of the proposed inverter, the required C_f at different m_a is acquired, as shown in Table 4-4. With R_L and L_f both set to 0.1 pu, the required C_f is in the range of 0.219-0.244 pu. The required C_f decreases with m_a increasing, therefore the proposed inverter is suggested to be operated at high m_a ranges regarding the reduction of C_f.

Table 4-4 Minimum Filter Capacitor for the Proposed Converter

R=0.1 pu, L=0.1 pu									
m_a	0.55	0.6	0.65	0.7	0.75	0.8	0.85	0.9	0.95
i_w THD (%)	62.4	61.9	61.5	61.6	59.1	58.7	57.3	57.1	56.7
i_s THD (%)	5	5	5	5	5	5	5	5	5
C_{min} (pu)	0.244	0.240	0.236	0.237	0.230	0.225	0.223	0.221	0.219

In summary, the study of passive component sizes reveals differing trends for DC inductors and LC filters. As the modulation index increases, the proposed inverter requires smaller DC inductors and LC filters. This suggests that the H-type five-level CSI is better working at high modulation indexes.

4.2.6 Switch voltage stresses

Table 4-5 lists the stress ratio of the DC side switch compared to the CSI side switch for the proposed H-type five-level CSI. Unlike the previously proposed X- and Γ-type CSIs, the DC side switches in the H-type CSI experience lower voltage stresses than the CSI side switches. As a result, series connection of DC switches is unnecessary.

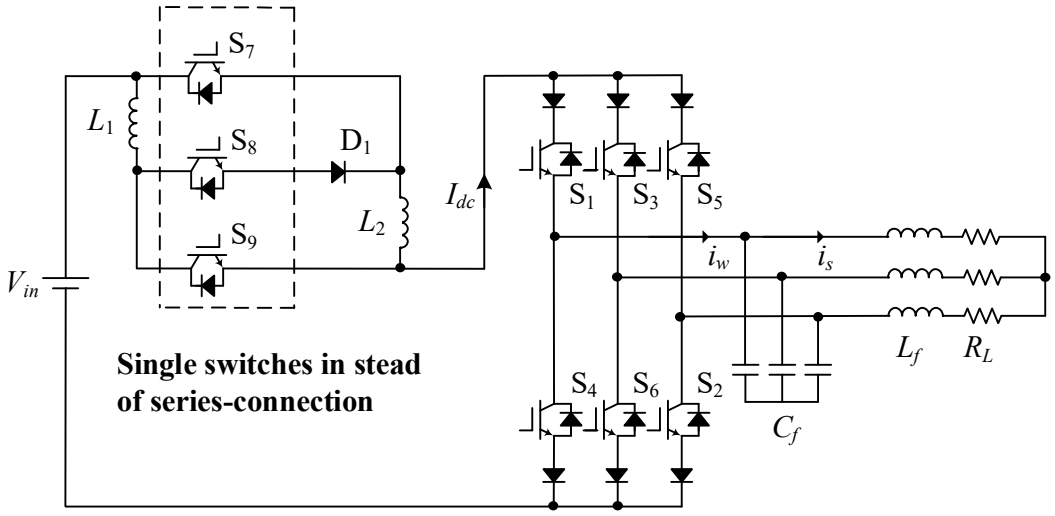


Fig. 4-9 Proposed H-type five-level CSI.

The proposed H-type CSI still requires 9 switches and 7 diodes, compared to 7 switches and 8 diodes for the X-type CSI, and 8 switches and 9 diodes for the Γ-type CSI. In medium-voltage applications, the X-type and Γ-type CSIs require more switches due to higher voltage stresses on certain switches (S_7 for the X-type CSI, and S_7 and S_8 for the Γ-type CSI), necessitating the use of series-connected switches.

In summary, the proposed H-type CSI offers a significant advantage: the voltage stress on the DC side is much lower than on the CSI side. This allows for the use of low-voltage switches, eliminates the need for series-connected switches (reduces the total switch count), reduces switching losses, and lowers costs.

Table 4-5 Voltage stresses of the switches

	V_{in} (pu)	Stress ratio S_7/S_1	Stress ratio S_8/S_1	Stress ratio S_9/S_1
m_a= 0.5	1	0.367	0.265	0.367
m_a = 0.6	1	0.302	0.395	0.302
m_a = 0.7	1	0.280	0.441	0.280
m_a = 0.8	1	0.335	0.530	0.335
m_a = 0.9	1	0.229	0.541	0.229
m_a = 1.0	1	0.215	0.571	0.215

4.2.7 Efficiency

As analyzed in Sections 2.2.8 and 3.2.8, the losses in the proposed converter primarily arise from semiconductor devices and inductors. The efficiency study methodology varies the DC inductor L_{dc} at different modulation indexes m_a to identify the inverter's optimal operating point, rather than displaying the efficiency profile using the same L_{dc} across the entire operating range (different m_a).

Fig. 4-10 shows the efficiency profiles of the H-type and X/Γ-type CSIs, with an input voltage set at 3000 V. Efficiency data, calculated and verified through PSIM, employ power switches FZ250R65KE3 and power diodes DD250S65K3. The modulation index spans from 0.5 to 1. Compared to the X- and Γ-type CSIs, which also have inherent DC current balance, the proposed H-type CSI achieves higher efficiency, reaching a maximum value of 93.6% at m_a = 1, while the X-type CSI reaches 87% and the Γ-type CSI reaches 92%.

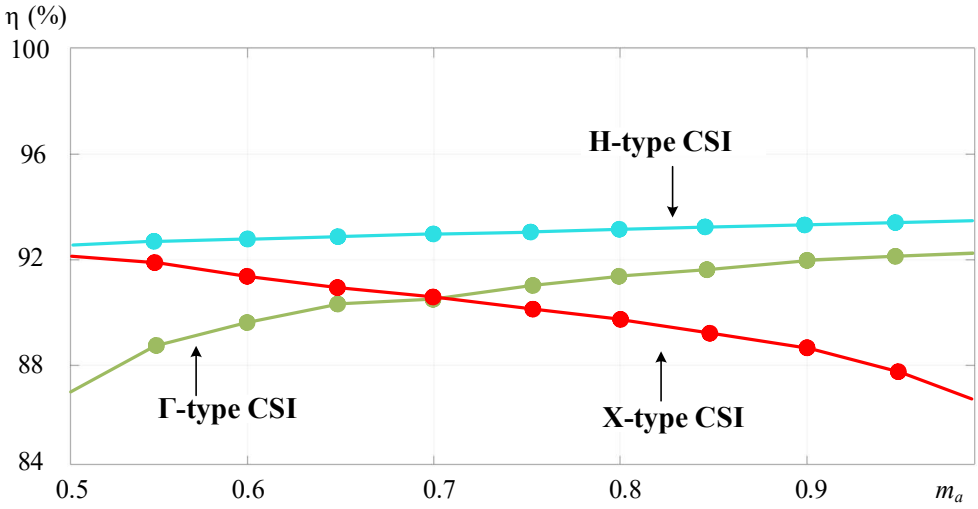


Fig. 4-10 Efficiency profile of the proposed inverter.

Two main factors contribute to the higher efficiency of the H-type CSI. First, it requires minimized DC inductance. Second, the switching losses of switches S_7, S_8, and S_9 are reduced due to their significantly lower voltage stress compared to the CSI side switches, as discussed in Section 4.2.6. This explains why the proposed H-type CSI has higher efficiency than the Γ-type CSI at m_a = 1, where both inverters use approximately the same DC inductance.

In summary, the H-type CSI has the highest total efficiency among the three new proposed inverters due to reduced inductive losses in the DC inductors and reduced switch losses on the DC side.

4.3 Performance verification

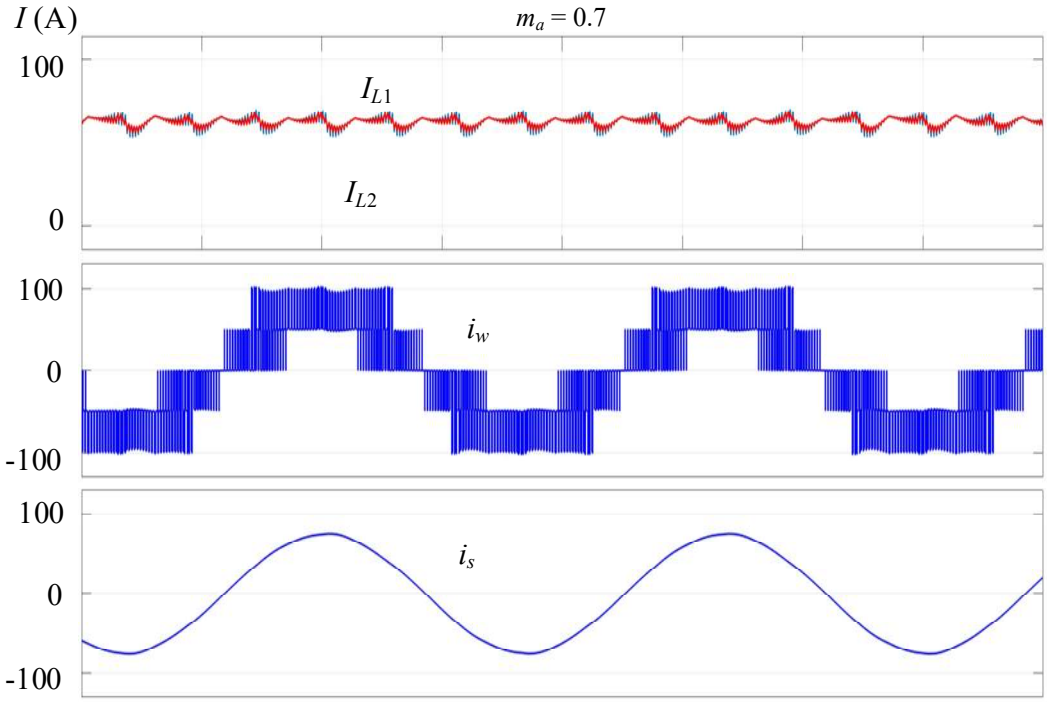
In this section, the performance of the proposed H-type CSI is verified through both simulation and experiment, where the parameters shown in Table 4-6. Two input inductors are intentionally set to different values (2/4 mH in simulation and 10/20 mH in experiment) to simulate the mismatches of DC inductors. In contrast to the parameters used in the X-type five-level CSI experiment, these input inductors are significantly

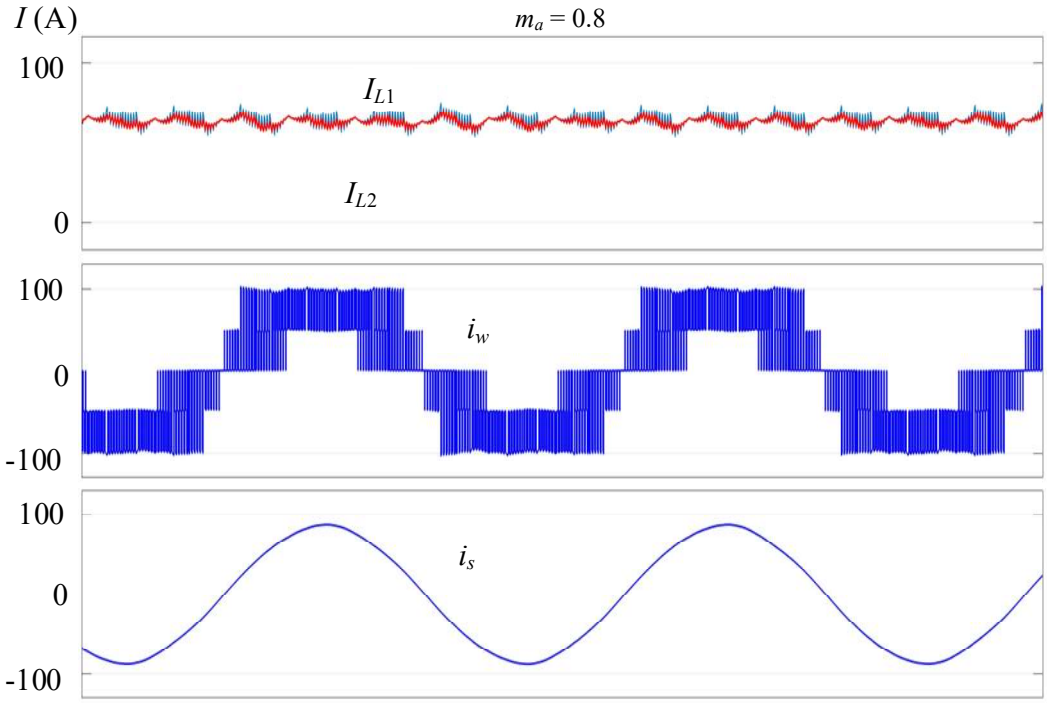
reduced (10/12 mH and 50/60 mH for X-type, 3/4 mH and 15/25 mH for Γ-type), while keeping other parameters constant. Note that due to the minimum overlap achieved by the dSPACE controller used in the experiments is too large at 2e-5, some narrow pulses are filtered out, leading to unexpectedly poor harmonics. To solve this issue while ensuring the experiment effectiveness, both the fundamental frequency (60 Hz reduced to 10 Hz) and the switching frequency (4320 Hz to 720 Hz) are reduced, while the frequency modulation index m_f remains the same before and after.

Table 4-6 Parameters in performance verification

Parameters	Simulation	Experiment
DC current	$I_{L1} = I_{L2} = 50$ A	$I_{L1} = I_{L2} = 5$ A
Fundamental frequency	60 Hz	10 Hz
Switching frequency	4320 Hz	720 Hz
Frequency modulation index m_f	72	72
Input inductance	2 mH, 4 mH	10 mH, 20 mH
Filter capacitance	55.7 uF	100 uF
Output load	10 Ω, 0.8 mH	1 Ω, 5 mH

A simulation model is built for the proposed converter through MATLAB/Simulink. A 3000 V voltage source is employed in the simulation with a power rating of 30 kW-0.4 MW. Fig. 4-11 demonstrates the waveforms of the proposed inverter under the selected parameters with modulation index m_a set to 0.7, 0.8, and 0.9. As expected, the inductor currents i_{L1} and i_{L2} have a self-balancing capability, and the output PWM current i_w has five current levels (-100A, -50A, 0, 50A, 100A) with excellent symmetry. The load current i_s increases as m_a increases, with expected sinusoidal waves acquired. The current ripple of inductor current becomes larger when m_a increasing, indicating the larger L_{dc} required.


I (A)
m_a = 0.7
100
I_{L1}
I_{L2}
0
100
i_w
0
-100
100
i_s
0
-100


I (A)
m_a = 0.8
100
I_{L1}
I_{L2}
0
100
i_w
0
-100
100
i_s
0
-100

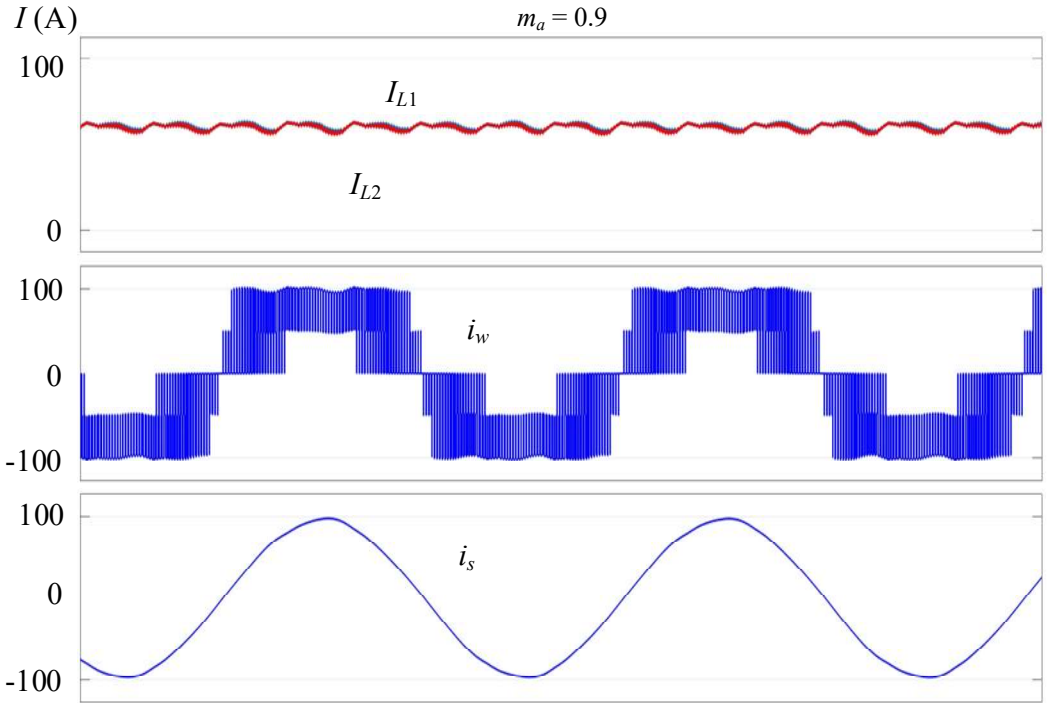


Fig. 4-11 Simulated waveforms of the proposed inverter.

The harmonic content of PWM current i_w for the inverter operating at a 60 Hz fundamental frequency with a 4320 Hz switching frequency is also shown in Fig. 4-10. The total harmonic distortion (THD) of i_w are 61.6%, 58.7%, and 57.1% for m_a set to 0.7, 0.8, and 0.9, respectively. The dominant harmonics are around 8640 Hz (144^{th}), with about 25% of the fundamental current. This is in line with the characteristic of the conventional SVM that the frequency of the dominant harmonic is about twice the switching frequency ($2m_f$) [1]. When m_a increased from 0.6 to 0.8, as we can see from Fig. 4-12, the percentage of fundamental for the dominant harmonics reduces from around 30% to 21%, this indicates the better harmonic performance at large modulation indexes.

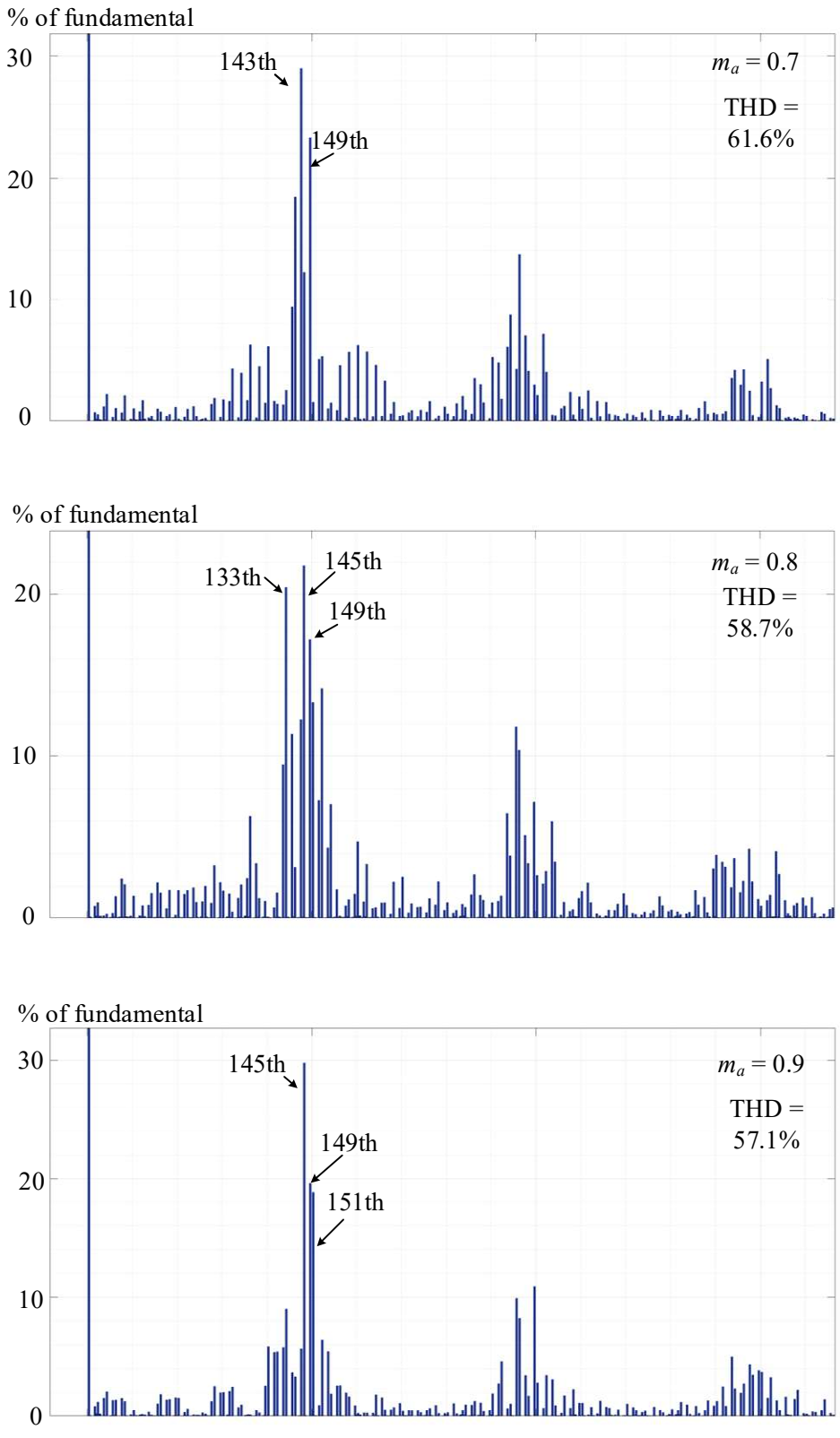


Fig. 4-12 Harmonic performance of the proposed inverter.

A down-scaled experiment is constructed using experimental setup. Fig. 4-13 shows the experimental waveforms of the two DC inductor currents. To verify the inherent current balancing feature, two different DC inductors as mentioned earlier are used: L_1 = 20 mH and L_2 = 10 mH. As shown in the figure, i_{L1} and i_{L2} are well balanced, and this is because of Mode 2, where the two inductors are charging in series, forcing the two DC inductors to be the same.

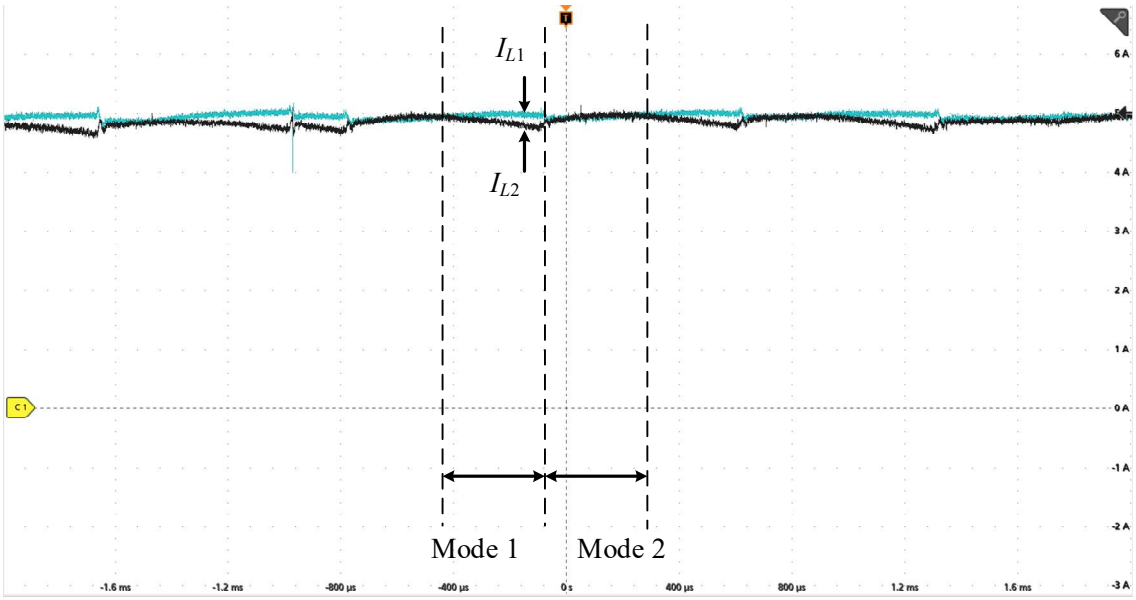
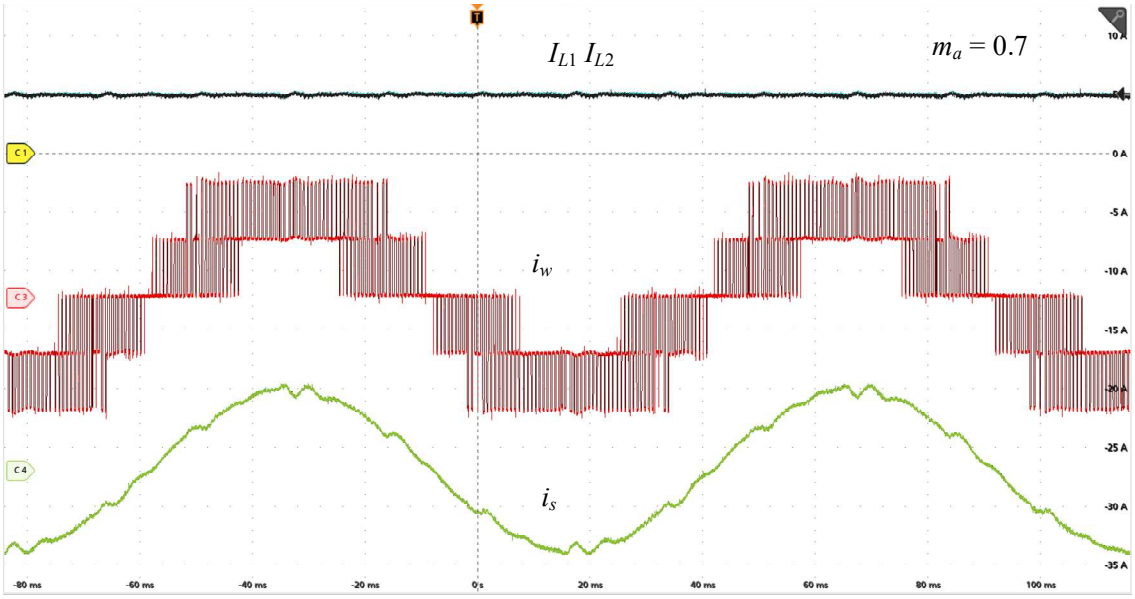


Fig. 4-9 DC inductor currents of the proposed inverter.



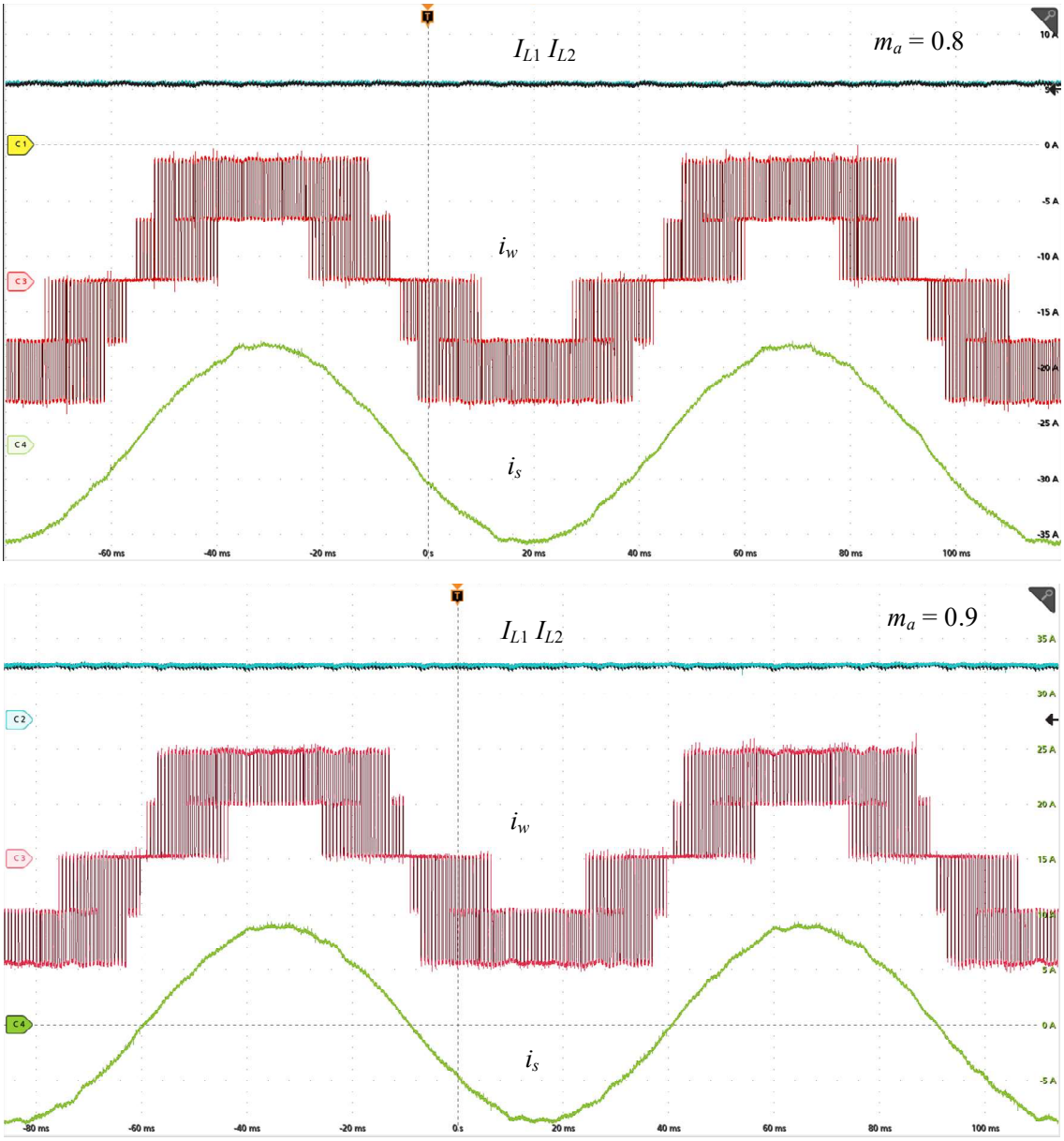


Fig. 4-10 Experimental waveforms under steady state.

Fig. 4-14 shows the waveforms under $I_{L1} = I_{L2} = 5$ A with different m_a. The current ripple of inductor current becomes larger when m_a increasing, indicating the larger L_{dc} required. The harmonic performance of i_w under different m_a is also shown in the figure, it has five current levels (-10A, -5A, 0, 5A, 10A) with excellent symmetry. The load current i_s increases as m_a increases, with expected sinusoidal waves acquired. The current

ripple of inductor current becomes larger when m_a increasing, indicating the larger L_{dc} required.

Fig. 4-15 shows the waveforms of the proposed topology under both dynamic state (I_{L1} = I_{L2} increased from 3 A to 5 A). The inductor currents I_{L1} and I_{L2}, the PWM current i_w, and the sinusoidal output current i_s are obtained. It can be found that five levels at the output PWM current are generated; PWM current and sinusoidal output current are increased accordingly; I_{L1} and I_{L2} have the self-balancing capability in both cases.

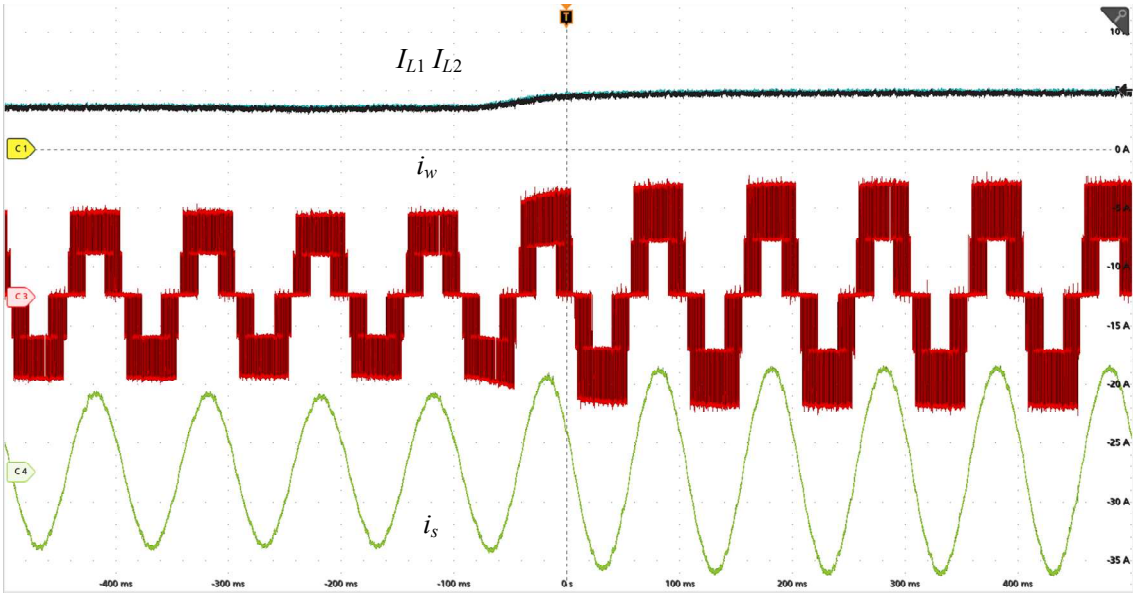


Fig. 4-11 Experimental waveforms under dynamic state.

4.4 Comparisons

The proposed five-level CSI topologies along with some existing ones are listed and compared in Table 4-7:

Device count and ratings: The proposed H-type CSI uses fewer switches than conventional five-level CSIs using two CSI modules. However, using fewer devices necessitates higher ratings for each device. The proposed H-type CSI requires nine switches and seven diodes, whereas the X-type CSI needs seven switches and eight diodes, and the Γ-type CSI requires eight switches and nine diodes. Nevertheless, under

medium-voltage applications, both X-type and Γ-type CSIs require more switches due to the higher voltage stress on certain switches (S_7 for X-type CSI, and S_7 and S_8 for Γ-type CSI), which necessitates the use of series-connected switches. As discussed earlier, the proposed H-type CSI offers a unique advantage: the voltage stress on all additional switches (S_7, S_8, and S_9) is small. This allows for the use of low-voltage switches, eliminates the need for series-connected switches, reduces switching losses and costs.

Total size of DC inductors: The H-type CSI requires the same size of DC inductors to maintain the continuous and smoothness of the DC current, compared to most of the conventional five-level CSI topologies, such as single-rating inductor five level CSI. The X-type and Γ-type CSIs, on the other hand, require much larger DC inductors. This is due to the disconnection of input source in certain operation mode while the DC inductors are discharging and act as equivalent current sources.

Efficiency: Compared with existing CSIs (X-type CSI and Γ-type CSI) that also have self-balancing inductor currents, the efficiency of the H-type CSI is higher, reaching the max value of 93.6% at $m_a = 1$, while it is 87% for the X-type CSI, and 92% for the Γ-type CSI. One contributor for the higher efficiency is the minimized DC inductance required by the H-type CSI. The second contributor is the reduced switching losses of the switches S_7–S_9. Compared with conventional CSIs that experience current imbalance issues, the proposed H-type CSI has similar performance in efficiency. For example, the parallel H-bridge five-level CSI has an efficiency of around 98.5% under a switching frequency of 540 Hz [36]. The calculated efficiency of this inverter under 4320 Hz is around 93.3%, where the DC inductor contributes 2%, the conduction loss contributes 1%, and the switching loss contributes 3.7%. The method used for efficiency calculation is a well-used one in industry [37].

DC current imbalance: Existing five-level CSIs come in two types: one experiences DC current imbalance issues, while the other features inherent DC current balance. The proposed X-, Γ-, and H-type CSIs feature inherent DC current balance, thus eliminating the need for additional current balancing schemes.

Table 4-7 Comparison of the existing five-level CSI topologies

Five-Level CSI Topology	With imbalanced currents (Conventional)			With self-balancing inductor currents		
	Single-rating inductor [30]	Multi-rating inductor [31]	Parallel H-bridge [37]	X-type	Γ-type	H-type
DC input count	1	1	2	1	1	1
Total switch count	12	12	12	7+	8+	9
Total diode count	12	12	12	8	9	7
Current stress (Same power rating)	I_L	I_L	I_L	I_L on DC side; $2I_L$ on CSI side	I_L on DC side; $2I_L$ on CSI side	I_L on DC side; $2I_L$ on CSI side
Total L_{dc}	Reference	Smaller	Same	Slightly larger under small m_a; significantly larger under large m_a	Slightly larger under small m_a; significantly larger under large m_a	Same
Efficiency	Reference	Similar	Similar	Slightly lower under small m_a; significantly lower under large m_a	Significantly lower under small m_a; slightly lower under large m_a	Similar (higher than X-type and Γ-type)
Current balance control	Needed	Needed	Needed	Not needed	Not needed	Not needed

4.5 Summary

In this chapter, an H-type five-level current source inverter is proposed. The proposed inverter inherits the self-balancing inductor current feature, eliminating the need for additional balancing controls. Compared to the previously proposed X- and Γ-type CSIs, the H-type CSI offers improved performance by utilizing smaller DC inductors across the entire operational range. This leads to a more compact and lightweight design, higher efficiency, and lower costs. Additionally, the series connection of DC switches is no longer required, further reducing both costs and losses.

Chapter 5 Conclusions

This dissertation studies five-level current source inverters, focusing on three novel topologies, their associated modulation schemes, and performance investigation. This chapter summarizes the main contributions of the research and outlines potential future work.

5.1 Contributions and conclusions

The main contributions and conclusions of this research are summarised as follows:

A novel X-type five-level CSI offering self-balancing inductor currents is proposed to eliminate the additional balancing controls.

The main technical challenge of conventional five-level CSIs is the current imbalance between the DC inductors/modules. The proposed X-type CSI is the first in the literature to feature self-balancing inductor currents, eliminating the need for complex and costly balancing control schemes. A new SVM-based modulation scheme has been designed for the X-type CSI, providing superior harmonic performance and overvoltage clamping capabilities. Other aspects, such as DC utilization, passive component sizes, and efficiency, have also been studied. The X-type CSI faces technical challenges, including the need for large DC inductors at high modulation indexes, which increases cost, volume, and losses. Additionally, series-connected switches are required on the DC side due to large voltage stresses. Therefore, the total switch count is increased, resulting in higher costs and losses. Calculations, analysis, and performance verification are provided.

A novel Γ-type five-level CSI offering self-balancing inductor currents is proposed to reduce the large DC inductors at high modulation indexes.

At high modulation indexes, where CSI-based topologies exhibit better harmonic performance, the X-type five-level CSI, despite its self-balancing inductor current feature, suffers from the need for large DC inductors. The proposed Γ-type five-level CSI retains the self-balancing inductor current feature while increasing the gain and significantly reducing the DC inductor size at high modulation indexes compared to the X-type CSI,

resulting in cost, volume, and loss savings. However, the drawbacks of the Γ-type CSI include reduced performance and the requirement for series-connected DC switches at low modulation indexes. Calculations, analysis, and performance verification are provided.

A novel H-type five-level CSI offering self-balancing inductor currents is proposed to further reduce the DC inductors and eliminate the need for series-connected switches on DC side.

The proposed X- and Γ-type CSIs eliminate the need for complex current balancing controls, but they require extremely large DC inductors in specific operating ranges (the X-type at high modulation indexes and the Γ-type at low modulation indexes). This significantly increases cost and losses, thereby limiting their operating range. The H-type five-level CSI also features self-balancing inductor current but requires significantly reduced DC inductance across the entire operating range, similar to traditional five-level CSIs. Additionally, the voltage stress on the DC side switch is greatly reduced throughout the full operating range, eliminating the need for series-connected switches and allowing the use of low-voltage switches, which further reduces costs and losses. Calculations, analysis, and performance verification are provided.

5.2 Future work

The following work is suggested for future research:

Modulation design of the proposed inverters.

The three proposed inverters use the similar SVM-based modulation scheme as an example, but this is not the optimal solution. Alternative SVM switching sequences can be employed, which could affect the performance of the inverters, including the required sizes of the DC inductors and harmonic performance. Additionally, other common CSI modulation schemes, such as SHE and TPWM, can be enhanced and applied to these inverters to further improve their performance.

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Related Publications

[1] **Z. Wang** and Q. Wei, "X-Type Five-Level Current Source Inverter," in *IEEE Transactions on Power Electronics*, vol. 38, no. 5, pp. 6283-6292, May 2023.

[2] **Z. Wang** and Q. Wei, "Γ-Type Five-Level Current Source Inverter," in *IEEE Transactions on Power Electronics*, vol. 39, no. 6, pp. 7206-7216, June 2024, doi: 10.1109/TPEL.2024.3380570.

[3] **Z. Wang**, Q. Wei and N. R. Zargari, "H-Type Five-Level Current Source Inverter," in *IEEE Transactions on Power Electronics*, vol. 39, no. 9, pp. 10682-10687, Sept. 2024, doi: 10.1109/TPEL.2024.3404822.