Ku Band Rotary Traveling-Wave Voltage Controlled Oscillator

by

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AUTHOR'S DECLARATION FOR ELECTRONIC SUBMISSION OF A DISSERTATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners. I understand that my thesis may be made electronically available to the public.

ABSTRACT

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Voltage-controlled oscillator (VCO) plays a key role in determination of the link budget of wireless communication, and consequently the performance of the transceiver. Lowering the noise contribution from the VCO to the entire system is always challenging and remains the active research area.

Motivated by high demands for the low-phase noise, low-power consumption VCO in the application of 5G, radar-sensing system, implantable device, to name a few, this research focused on the design of a rotary travelling-wave oscillator (RTWO). A power conscious RTWO with reliable direction control of the wave propagation was investigated. The phase noise was analyzed based on the proposed RTWO. The phase noise reduction technique was introduced by using tail current source filtering technique in which a figure-8 inductors were employed. Three RTWO were implemented based on GF 130 nm standard CMOS process and TSMC 130 nm standard CMOS process. The first design was achieving 16-GHz frequency with power consumption of 5.8-mW with 190.3 dBc/Hz FoM at 1 MHz offset. The second and third design were operating at 14-GHz with a power consumption range of 13-18.4mW and 14.6-20.5mW, respectively. The one with filtering technique achieved FoM of 184.8 dBc/Hz at 1 MHz whereas the one without inudctor filtering obtained FoM of 180.8 dBc/Hz at 1 MHz offset based on simulation.

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Table of Contents

List of Tables

List of Figures

List of Symbols

ADS	Advanced Design Systems
AC	Alternating Current
ADC	Analog-to-Digital Converter
ADE	Analog Design Environment
ADPLL	All-Digital Phase-Locked Loop

AM	Amplitude Modulation
CCW	Counter-Clockwise
CW	Clockwise
$CMOS$	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
DRC	Design Rule Checking
DLL	Delay-Locked Loop
DAC	Digital-to-Analog Converter
$DARPA$	Defense Advanced Research Projects Agency
DCO	Digital-Controlled Oscillator
DC	Direct Current
EM	Electro-magnetic
EDA	Electronic Design Automation
FET	Field-Effect Transistor
FF	(nMOS)Fast-(pMOS)Fast
FS	(nMOS)Fast-(pMOS)Slow
FoM	Figure-of-Merit
FoM_T	Figure-of-Merit with Tuning
GP	Geographic Programming
GF	GlobalFoundries
IF	Intermediate Frequency
LC	Inductor-Capacitor
LO	Local Oscillator

LVS	Layout Versus Schematic
LUT	Look-Up Table
LTI	Linear-Time-Invariant
$mm-Wave$	Millimeter Wave
$MIM(-cap)$	Metal-Insulator-Metal (Capacitor)
$MMIC$	Monolithic Microwave Integrated Circuit
MCU	Microcontroller Unit
$nMOS(NMOS)$	n-channel Metal-Oxide Semiconductor
$pMOS(PMOS)$	p-channel Metal-Oxide Semiconductor
PN	Phase Noise
PLL	Phase-Locked Loop
$PSRR$	Power Supply Rejection Ratio
PA	Power Amplifier
PVT	Process, Voltage and Temperature
PM	Phase Modulation
$Q(-factor)$	Quality Factor
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
$RFIC$	Radio-Frequency Integrated Circuit
$RFID$	Radio-Frequency Identification
$RTWO$	Rotary Traveling-Wave Oscillator
$ROAs$	Rotary Oscillator Arrays

RX	Receive
SF	(nMOS)Slow-(pMOS)Fast
SS	(nMOS)Slow-(pMOS)Slow
SNR	Signal-to-Noise Ratio
$SHRX$	Subharmonic Receiver
SWO	Standing-wave Oscillator
TT	(nMOS)Typical-(pMOS)Typical
TX	Transmit
TL	Transmission Line
TR	Tuning Range
$TSMC$	Taiwan Semiconductor Manufacturing Company
VCO	Voltage-Controlled Oscillator
$RLGC$	Resistor-Inductor-Conductance-Capacitor
SAW	Surface Acoustic Wave
SDR	Software Defined Radio
$SPICE$	Simulation Program with Integrated Circuit Emphasis
$1G$	First Generation Cellular Network
$2G$	Second Generation Cellular Network
$3G$	Third Generation of Wireless Mobile Telecommunications Technology
$4G$	Fourth Generation Technology Standard for Broadband Cellular Networks
$5G$	Fifth Generation Technology Standard for Broadband Cellular Networks
$6G$	Sixth Generation Technology Standard for Broadband Cellular Networks

Chapter 1

INTRODUCTION

1.1 Background

The modern electronic-based system relies on a frequency generator as its 'heart'. Timing references leads a system and its components on the right track. Fig. 1.1 shows some applications where the accuracy of the clock is of great interest in the radar system, 4G/5G

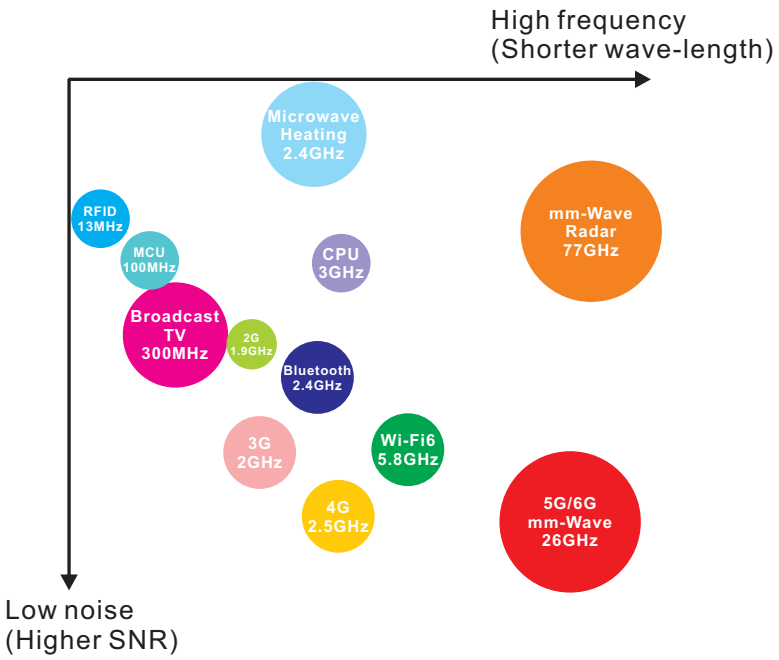
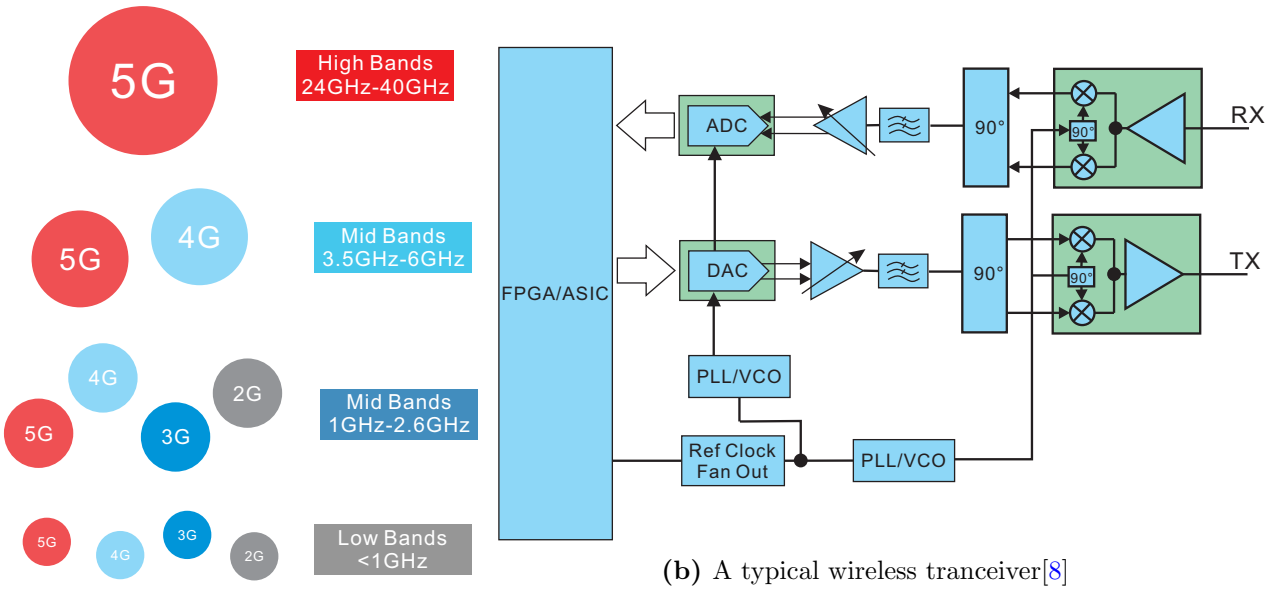


Figure 1.1: Applications of oscillator

mobile phone communication systems, and WiFi whereas such a requirement in RFID and MCU running at low frequency is much relaxed.

The first commercial mobile communication system at which only voice data was transferred was launched in 1979. After four decades, the fifth-generation (5G) mobile communication system started deploying in many countries, and the market of 5G were quickly growing since 2019. The frequency bands that were reserved for the mobile system has also changed dramatically. Fig. 1.2(a) illustrated the spectrum usage from the second-



(a) Cellular Spectrum[7]

(b) A typical wireless tranceiver[8]

Figure 1.2: 5G communication

generation (2G) to the fifth-generation (5G) telecommunication system[7]. Shannon–Hartley theorem defined that the maximum channel capacity is dictated by channel bandwidth and signal-to-noise ratio (SNR). With the increasing demands of the high-data transfer, the higher frequency bands is desirable. With the launching of 5G technology, the modulation method is close to Shannon–Hartley limitation. Expanding the bandwidth become the only effective option. Frequency bands ranging above a few of Gigahertz providing sufficient bandwidth lends themselves to obviating upper limit of data transfer in many applications. In particular, 5G communication system designed for mid-bands and high-bands [1.2(a)]

achieves data rate multiple times faster than 4G communication system. A RF transceiver in 5G system, composed of the key building blocks, e.g., RF front-end modules, ADC/DAC, frequency synthesizer and digital signal processor, is shown in Fig. 1.2(b). Since the frequency synthesizers are involved in both signal paths, the performance of the clock generation circuits heavily affects the overall performance of the transceiver. Especially, the accuracy of the clock, referring to the phase noise (PN) in the frequency domain and jitter in the time domain, plays one of the key roles in the design. In addition, the power consumption makes the frequency synthesizer become the most power hungry device in the receiver and second power hungry device in the transmitter shown in Fig. 1.3, e.g., 50% of in the RX and 20% in the TX[1, 9, 10]. Fig. 1.3 summarizes the power consumption of every component in a transceiver. The measurement result in Fig. 1.3 is from a low-power design. It only indicates the percentage of power consumption. With all the power consumption from each block being considered, it becomes evident that low-power design is preferable. Properly dealing with the power-dominant module is apparently the efficient and effective method, e.g., the clock generation circuit. Since the voltage-controlled-oscillator (VCO) is the core of the frequency synthesizer, dictating the PN and power consumption in general, the design of VCO is the focus of this research.

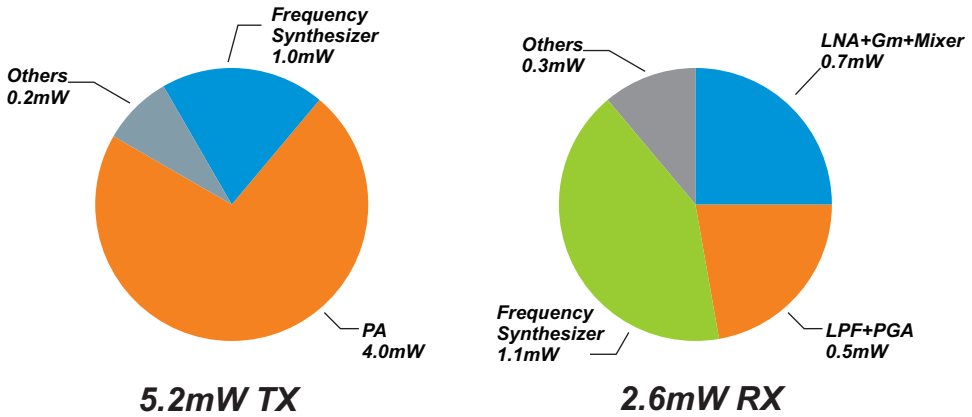


Figure 1.3: Measured power consumption in RF transceiver[1]

1.2 The History of VCO

1.2.1 VCO Technology

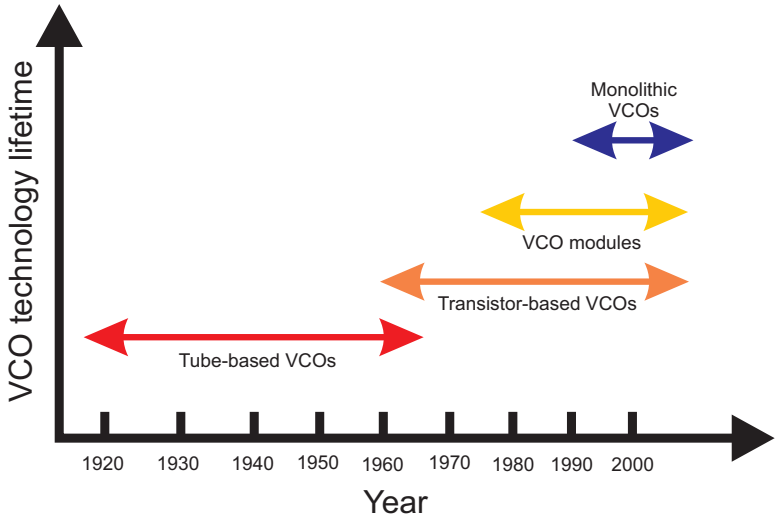


Figure 1.4: VCO lifetime as a function of time[2]

In 1912, E.H. Armstrong discovered that a vacuum tube could be configured to generate an oscillation. He effectively invented the first electronic oscillator. From Armstrong's invention in the 1910s to the modern era, VCOs progressed from vacuum-tube based to transistor-based to RFIC-based. The first bipolar transistor was born in the late 1940s at Bell Laboratories. Later it replaced vacuum tubes. In the modern era, VCOs are embedded as a critical component of complicated ICs[2]. In Fig. 1.4, the lifetime of certain types of VCOs is affected by technology. From tube-based VCOs to Monolithic VCOs, the VCO technology has passed four generations. Fig. 1.5 shows the size of VCO significantly reduced with time, dropping 30 times over two decades (1985-2005). The wavelength of the signal becomes shorter, and the size of the VCO is smaller. In addition, due to the development of integrated circuit, modern VCOs are embedded as a simple module of the system. The proposed VCOs in this thesis paper is smaller than $1mm^3$. The main reason for the shrinking of the size is driving force of the higher operating frequency and the advanced technology for

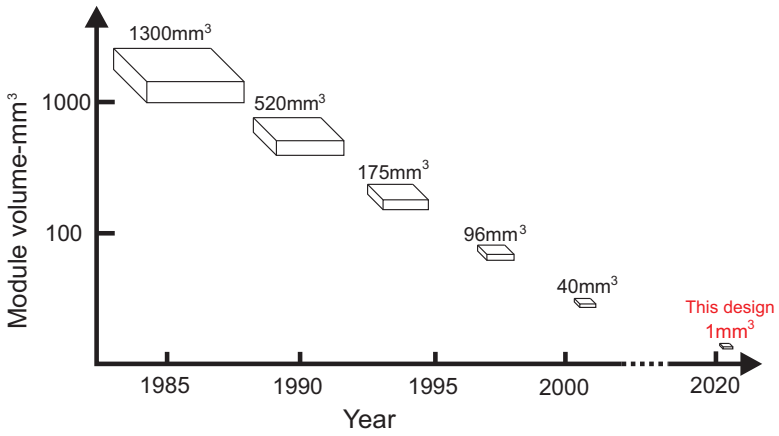
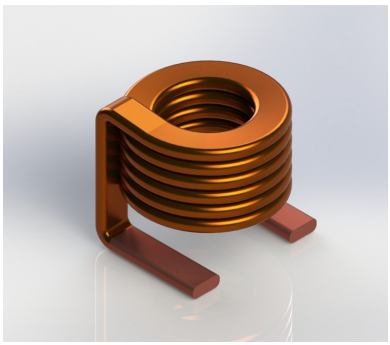


Figure 1.5: VCO size scale vs time

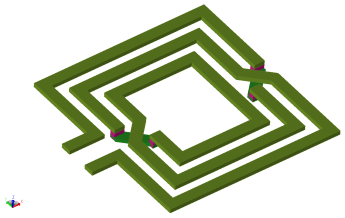
VCOs fabrication. Applications falling into several tens of gigahertz start drawing attentions from industry. Also, monolithic RFIC technology makes all-in-one design possible.

1.2.2 Monolithic VCO

The definition of a monolithic microwave integrated circuit is a type of microwave circuit that is fully embedded on a single chip. The first instance of monolithic VCOs was achieved by gallium-arsenide(GaAs) IC technology in the early 1980s. It is a part of the US DARPA MIMIC program[2]. Later in the 1990s, it was transplanted to silicon chips because silicon-based integrated circuits was efficient at high transition frequency(f_T), which allows cheaper silicon-based MMIC possible. An example of the traditional air-core inductor and



(a) Copper aircore inductor



(b) On-chip spiral inductor

Figure 1.6: Comparison of aircore and spiral inductors

on-chip inductor is shown in Fig. 1.6(a) and (b), respectively. It is noticed that the stacked structure is implemented in the aircore inductor whereas the planar form is applied to the on-chip inductor. The small footprint makes the on-chip inductor more attractive for the high-level integration and subsequently the more compact design. The IC process, however, has a limited number of metal layers that are suitable for inductors. More important, the inductance per unit area compared to the discrete inductor is significantly less. In addition, accurately modelling inductors on-chip is quite challenge when the design of inductor comes to the sub-μm process. It is essential to use modern EDA tools to verify the design at which finite element model in the analysis is used. Fig. 1.7 presents a mesh network in a microstrip line in a 3-D view. Note that the simulator breaks the electronic microwave network into small grid and numerically solves Maxwell equations for each grid. The results from simulation can be in the form of S, Y or Z parameters.

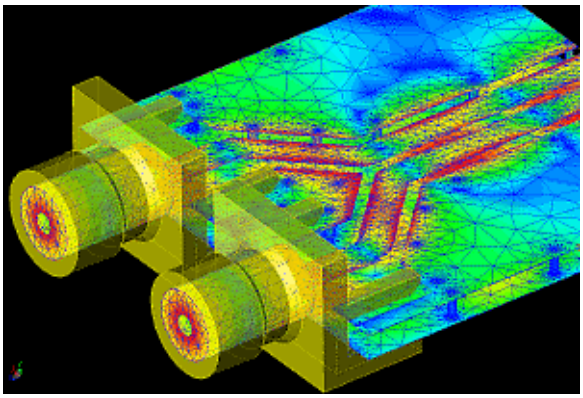


Figure 1.7: Mesh network of EM simulation[3]: The lines separate the grid, and the colour shows the magnetic field.

1.3 Types of Oscillator

Every type of oscillator has a different application scenario. Fig. 1.8 enumerated 3 major types of electronics oscillator. A ring oscillator is a system made up of an odd number of NOT gates whose output oscillates between true and false voltage levels. The NOT gates,

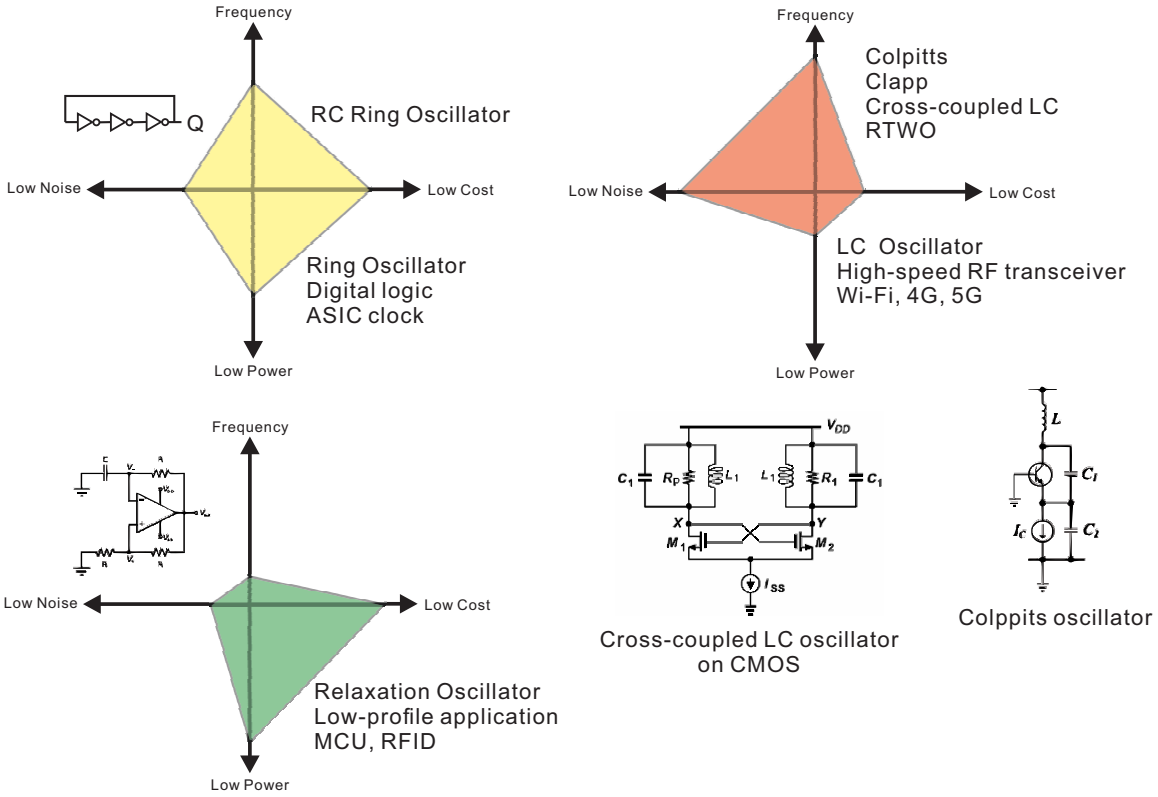


Figure 1.8: VCO types

also known as inverters, are connected in a chain, with the last inverter's output feeding back into the first. Since a single inverter computes the logical NOT of its input, it can be seen that the logical NOT of the first input is computed by the last output of a chain of an odd number of inverters. This final output is claimed after a finite amount of time has passed after the first input is asserted, oscillation is caused by the feedback of this last output to the input. Two methods may be used to increase oscillation frequency. First, the applied voltage can be increased, which increases the frequency of the oscillation and the amount of power consumed, which is then dissipated as heat. A relaxation oscillator is a nonlinear electronic oscillator circuit that generates a non-sinusoidal output, such as a triangle or square wave. The circuit consists of a feedback loop with a switching device, such as a transistor, comparator, relay, or amplifier, or a negative resistance device, such as a tunnel diode, that repeatedly charges and discharges a capacitor or inductor through a resistor until it reaches a threshold level. The time constant of the capacitor or inductor circuit determines the oscillator's duration. The active system suddenly transitions between charging and

discharging modes, resulting in a repetitive waveform that is constantly changing. The other kind of electronic oscillator is the harmonic or linear oscillator, which uses a feedback amplifier to excite resonant oscillations in a resonator, generating a sine wave. Relaxation oscillators are used in voltage-controlled oscillators (VCOs), inverters and switching power supplies, dual-slope analogue to digital converters, and signal generators to generate low-frequency signals for applications such as blinking lights (turn signals) and electronic beepers. The LC oscillator is a type of oscillator that uses an LC (inductor-capacitor) tank circuit to provide the necessary positive feedback to keep the oscillations going. The LC tank circuit is also known as the LC tuned circuit or the LC resonant circuit. A circuit can only withstand stable oscillations at frequencies where the loop gain of the device is equal to or greater than one and the phase shift between input and output is 0 according to the Barkhausen criterion for sustained oscillations. BJT, FET, MOSFET, op-amp, and other semiconductors may be used to create LC oscillators. RF signal generators, frequency mixers, tuners, sine wave generators, and RF modulators are examples of LC oscillator applications. At the same time, the LC oscillator has a higher cost and power.

1.4 Motivation and Objectives

To improve the battery life of a mobile device while meeting the phase noise requirements for a wide tuning range, the VCOs, which is the core of the phase-locked-loop (PLL), needs special treatment. The LC oscillator is noted for its superior phase noise performance compared to the ring oscillators, resulting in a wide deployment in the wireless transceiver. Since the concept of rotary travelling wave oscillator (RTWO) was proposed by Wood[11] in 2001, it has been proved an excellent overall performance and functionality. First, the RTWO inherently has multi-phase output. This feature allows RTWO to be applied in multi-phase applications, such as multi-phase ADC/DACs. Second, the RTWO has a square-like output waveform. A square-like output waveform is helpful in any digital circuits and some analogue circuits, such as VLSI clocking, switching mode mixers. On the other hand, designing RTWO has more challenges than LC Oscillators. In the first decade after the paper of Wood, RTWO has not been mentioned frequently. Subsequently, with EDA tools' evolution,

several design challenges of RTWO have been adequately addressed by electromagnetic field analysis. Electromagnetic field analysis tools enable designers to catch much more details of a distributed-element model. Significantly, it speeds up the designing of customized on-chip electromagnetic elements. A geometric programming(GP) method was introduced later to RTWO design[12]. After 2010, RTWO started drawing more attention from academia [5, 13, 14, 15]. Bai, *et al.*[4, 16, 17, 18] applied the injection-lock technique to RTWOs so as to enable RTWO for the use of VLSI while the total power consumption is lower than the clock distribution tree. Injection-locking has been studied extensively and has numerous application use[19, 20, 21, 22, 23, 24]. To further improve the performance, [25] applied filtering technique on RTWO, which was originally used in the LC oscillator[26].

In this research work, the main objectives are to: i) Design RTWOs with controlled wave propagation, which was not done properly before. ii) Examine the phase noise reduction technique without sacrificing the power consumption. iii) Make a comparative study of current-mode amplifier with filtering technique and the voltage-mode amplifier in RTWOs. The design will be verified based on two 130-nm technologies, e.g., GF 130-nm standard CMOS and TSMC 130-nm standard CMOS process.

1.5 Contributions

- **Fangzhou Sun**, Yushi Zhou, Zhanjun Bai and Yong Chen *"A 190.3-dBc/Hz FoM 16-GHz rotary travelling-wave oscillator with reliable direction control"* in IET Electronics Letters, 2021[27].

The original contributions of the dissertation are summarized in this section.

1.5.1 A 16-GHz RTWO

A 16-GHz RTWO design based on the Global Foundry 130-nm RF CMOS process was implemented. This RTWO includes a transmission line ring composed of 16 segments, 16 amplifiers, 16 varactors and a direction control circuit. As discussed before, the wave can be

randomly propagated in two directions, resulting in extra detection circuits to accommodate the uncertainty. In this research work, we presented a switching scheme on the controlling the power supply of each amplifiers in the RTWO for clockwise and counter clockwise propagation. The proposed direction control circuits were verified through simulations under corners, temperature and supply voltage variations. Monte-Carlo simulation with 200-runs with zero failure proved that the wave propagation can be controlled reliably. The same control scheme was applied to the next two designs, which were sent out for fabrication on April 26 through CMC Microsystem. Another contribution is the tunable power supply. A power tuning circuits is achieved combined with the direction control circuit at no extra cost. The 16-GHz RTWO design can be tuned with a range of 3 mW to 5.8 mW. The proposed RTWO achieved an FoM of 190.3 dBc/Hz at 1 MHz with frequency tuning of 11.2% (15.1 to 16.9 GHz).

1.5.2 Two 14-GHz RTWOs

We also designed two RTWOs based upon TSMC 130-nm RF CMOS process for fabrication and comparison purpose. The phase noise performance improvement technique was utilized in one oscillators by making use of the filtering technique while the other oscillator was designed in a way that can be used to compare PN if no filter was presented. The inductor was chosen in a so called figure-8 shape structure so as to increase the inductance and quality factor. Each of RTWOs consists of five blocks, e.g., transmission line ring, eight amplifiers with/without tail current filter, eight tuning banks, four output buffers and one direction control block. To make fair comparison the free-running frequency is the same and the power consumption was tuned to a similar level. The simulation result shows the RTWO with tail filtering has an Figure-of-merit (FoM) of 186 dBc/Hz at 1MHz, and the comparison group has an FoM of 184 dBc/Hz at1MHz. Both RTWOs have a frequency tuning range of 15%, achieved by the use of discrete capacitor banks and varactors.

1.6 Thesis Organization

The rest of the thesis is organized as follows:

- Chapter 2 briefly discusses the fundamental of the oscillators, followed by a systematic study on the theory of rotary travelling-wave oscillators. All components in RTWO and the operating frequency is mathematically demonstrated. A mathematical analysis of phase noise is demonstrated using the linear time-invariant(LTI) system and cyclo-stationary property theories. Some state-of-the-art designs will be given with details. In the meantime, the necessary tools will be introduced. In addition, the architecture and the design process of RTWO will be described.

- Chapter 3 presents a detailed 16-GHz RTWO design with simulation. This design is based on the Global Foundry 130-nm RF CMOS process.

- Chapter 4 presents two 14-GHz RTWO designs with simulated results. This instance of RTWO is based on the TSMC 130-nm RF CMOS process, and a detailed layout will be shown.

- Chapter 5 concludes this research and brings some future research directions.

Chapter 2

THEORETICAL STUDY OF RTWO

2.1 Fundamental of Oscillators

In this chapter, some of the key design parameters and considerations will be examined in order to fully understand the design challenge of the oscillators. More details can be found from [28, 29].

2.1.1 Key Performance Factors of an Oscillator

When it comes to the design of oscillator, especially when it is used for the RF transceivers, the trade-offs of the phase noise, the power consumption, the signal swing and the silicon area, etc., are adding significant design efforts. It is vital to know and understand what the principal theory are from circuit design point of view. The following lists the key design considerations:

Frequency Range An RF oscillator must be able to change its operating frequency within a specific range. For example, an IEEE 802.11b[30] transceiver requires a bandwidth coverage of 100-MHz from 2.4-GHz to 2.5-GHz, but the range must reserve an additional margin to cover the process, voltage, temperature(PVT) mismatch. If the designer assumes the additional margin is 5%, the target frequency tuning range of this VCO will be 2.205-GHz to 2.695-GHz(10%).

Output Voltage Swing An RF oscillator should provide a large enough output swing to drive the load circuit so as to either lower the on-resistance of the switch, e.g., switching mixer, or widen the lock range for the injection-locked frequency divider in the PLL. An example of a nominal voltage of 1.2 V in the 130-nm process, the single-ended output swing should be designed from 0.2 to 1.0 V_{pp} with $V_{ds,min} = 100$ mV. Also to isolate the load impact and to amplify the signal, output buffer is inserted between the oscillator and load circuit.

Phase Noise Among the design considerations, in the presence of the noise from the circuits and environmental, phase noise is sometimes considered with the highest priority in the design. We take LC oscillator for example, if the oscillator is ideal, and the output is in the form of sinusoidal waveform, leading to an impulse in the frequency domain. In practice, however, the filter is not ideal, and the active devices utilized in the design contributing noise to the output and subsequently reshape the single pulse to a "skirt" around the carrier. The larger offset from the carrier, the more noise suppression introduced by the LC tank can be expected. The quantity of the PN is the measurement of the suppression as compared with the carrier power spectrum at the offset frequency. The noise resources will be discussed in details in the following chapters to demonstrate the approach used in this research work to lower the noise contribution from the active devices.

Output Waveform What waveform is desired by the circuit? For example, a switch-mode mixer needs a 50% or 25% duty cycle square wave signal. The output buffer transfers a sinusoidal LC tank VCO wave output into a square wave output. On the other hand, for an active mixer, to lower the power consumption, the square wave is not required. The signal waveform is dictated by the load circuit.

Power Consumption Power dissipated by the VCO varies with the power supply voltage. The power consumption is not a single design parameter. In fact, the power is usually traded with other design parameters, e.g., frequency, PN and output swing.

2.1.2 Barkhausen's Criteria

In 1921, H.Barkhausen(1881–1956) developed a mathematical stability condition theory known as Barkhausen's criteria. To maintain a stable-state oscillation, two conditions are needed to meet in a feedback system. The two conditions at a frequency: (1) the phase shift of loop gain is 360 degrees, (2) the loop gain of the system is unity. A general feedback system is shown in Fig. 2.1, where the input $\varphi_i(s)$ is feeding to the system with the forward

Figure 2.1: Barkhausen Criteria

path and feedback network, represented by $H(s)$. The transfer function is given by:

$$\frac{\varphi_o}{\varphi_i}(s) = \frac{H(s)}{1 + H(s)}. \tag{2.1}$$

Assume the forward network is implemented by a CS amplifier of which has 180 degree phase shift between the input and the output, i.e., $H(s = j\omega_1) = -1$. At the frequency ω_1, the feedback network. We can obtain the following:

$$\angle H(s = j\omega_1) = 180^\circ,$$

$$|H(s = j\omega_1)| = 1. \tag{2.2}$$

Eq. (2.2) is used to describe the Barkhausen Criteria. If a system satisfies both conditions, it steadily oscillates at ω_1 with a stable amplitude.

2.1.3 Voltage Controlled Oscillator

Most applications need an oscillator with adjustable frequency. If the frequency of the oscillator is tuned through voltage incident, we define this type of oscillators as "Voltage-controlled oscillators(VCOs)". The frequency varies from f_{min} to f_{max} with the control voltage. The slope of the frequency versus voltage is defined as the gain of the oscillator, denoted by K_{VCO}. Thus, the output frequency of the oscillator is given by

$$f_{out} = K_{VCO}\Delta V_{tune} + f_c, \tag{2.3}$$

where f_c is the centre frequency of the tuning range, ΔV_{tune} is the offset of the tuning voltage, f_{out} is the output frequency.

2.1.4 Phase Noise

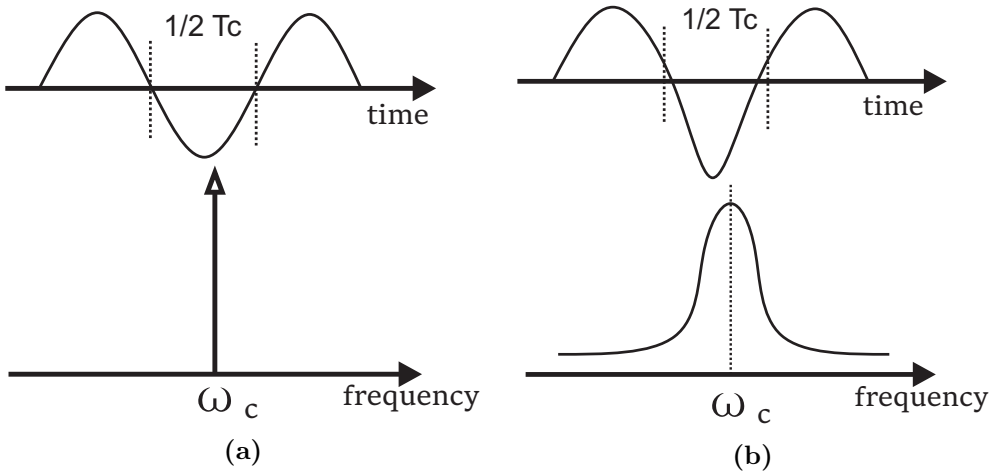


Figure 2.2: (a)Noiseless signal, (b)Noisy signal

Assuming the output of the oscillator is a sinusoidal voltage signal, it therefore can be described as $x(t) = A\cos(\omega_c t)$, which is a single impulse on the frequency domain, as Fig. 2.2(a). However, a real oscillator always dressed up with a 'noise skirt', as Fig. 2.2(b). The noise of the oscillator devices continuously perturbs the zero-crossing point of the sinu-

soidal wave[28]. The function with phase noise can be written as

$$\begin{aligned} x(t) &= A\cos[\omega_c t + \phi_n(t)] \\ &\approx A\cos(\omega_c t) - A\sin(\omega_c t)\sin[\phi_n(t)] \\ &\approx A\cos(\omega_c t) - A\phi_n(t)\sin(\omega_c t), \end{aligned} \tag{2.4}$$

where $\phi_n(t)$ is a small signal that changes the position of the zero-crossing points. Since $\phi_n(t) << 1$, Eq. (2.4) is simplified to the last expression. It shows the output signal has two components: an impulse at ω_c and a noise skirt around ω_c. Commonly, a 1-Hz bandwidth window at a certain offset frequency is used to denote the phase noise. The carrier power is the reference in the representation of PN. Fig. 2.3 shows how the PN is measured in the lab and simulations.

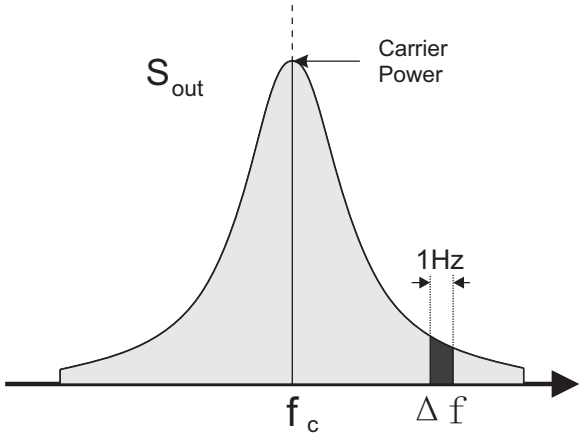


Figure 2.3: Specification of phase noise.

Measure the signal power of 1-Hz windows at Δf and normalize it to the carrier power. The unit of phase noise is called "dB per Hz with respect to the carrier", dBc/Hz. In addition, the phase noise drops down a fixed noise floor at a few hundred megahertz. Even there is not a clear 'border' between 'close-in and 'far-out' areas, the close-in phase noise usually defined within 100 MHz offset, is of great interest. Phase noise is usually measured in a single side-band form. Considering the simplest ideal oscillator[29] shown in Fig. 2.4.

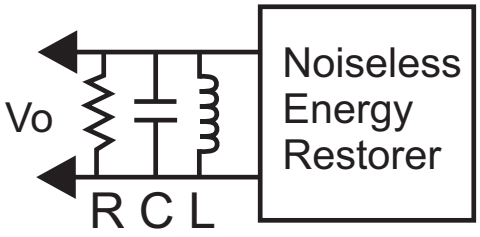


Figure 2.4: Ideal RLC oscillator

This oscillator includes a lossy tank with a noiseless energy restorer. The energy restorer perfectly compensates for the energy loss of the tank resistor R. Consequently, the tank resistance is the only noise source in this oscillator. Now, calculate the energy stored in the RLC tank, and we have

$$E_{stored} = \frac{1}{2} C V_{pk}^2, \tag{2.5}$$

where V_{pk} is the peak voltage of the capacitor. At the moment of voltage peak, all energy of the tank is stored on the capacitor. Assume the waveform of Vo is sinusoidal. Therefore, The mean-square voltage is

$$\overline{V_{sig}^2} = \frac{E_{stored}}{C}. \tag{2.6}$$

To compute the total mean-square noise voltage, we integrate the thermal noise density over the noise bandwidth, and Eq. (2.7) can be written as

$$\overline{V_n^2} = 4kTR \int_0^\infty |\frac{Z(f)}{R}|^2 \, df = 4kTR \cdot \frac{1}{4RC} = \frac{kT}{C}, \tag{2.7}$$

where the thermal noise voltage of the resistor is 4kTR and the transfer function of the RLC network is $|\frac{Z(f)}{R}|^2$. Combining Eq. (2.6) and Eq. (2.7), the noise-to-signal ratio is obtained as

$$\frac{N}{S} = \frac{kT}{E_{stored}}. \tag{2.8}$$

Q-factor is used to describe the capability of storing energy in a system, as shown in Eq. (2.9). It is defined by the ratio of stored energy and dissipated energy on the resonator during each

cycle. An ideal resonator has zero power dissipation($P_{diss} = 0$), and Q=∞.

$$Q = \frac{\omega E_{stored}}{P_{diss}} \tag{2.9}$$

Combining Eq. (2.8) and Eq. (2.9), there is

$$\frac{N}{S} = \frac{\omega kT}{QP_{diss}}, \tag{2.10}$$

where P_{diss} is the power consumed by the tank resistor. This simple equation provides some intuitives from design point of view. It shows that: i) The higher Q-factor from the tank, the less noise corrupts the oscillation signal. In a practical design, the Q-factor is dominated by the inductor due to the fact that the inferior performance of CMOS process limits the implementation of high-Q on-chip inductor. ii) The more current pump into the oscillator, the less noise at the output. It is of great interest that the trade-off between the PN and the power consumption makes the design of oscillator so challenging as one hand, the large power consumption reduces the life-time of the device, and the other hand, the PN requires large power consumption.

2.1.5 Figure of Merit

We summarize the foregoing discussion into Fig. 2.5 to include the main considerations in the research work, in which the trade-offs are clearly labelled by the arrow lines.

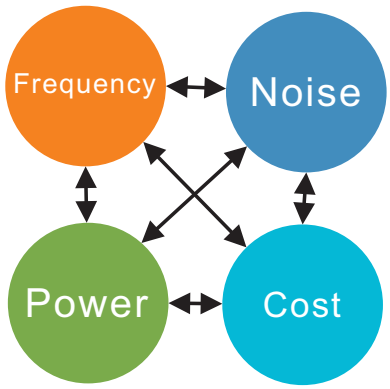


Figure 2.5: trade-offs

While one of them is getting promoted, the others are being downgraded. In VCO design, the standard form of Figure-of-Merit and Figure-of-Merit with tuning are shown below:

$$FoM(\Delta f) = -PN(\Delta f) + 20\log_{10}(\frac{f_0}{\Delta f}) - 10\log_{10}(\frac{P_{DC}}{1mW}), \tag{2.11}$$

$$FoM_T(\Delta f) = FoM(\Delta f) + 20\log_{10}(TR/10\%), \tag{2.12}$$

where FoM is the figure of merit in general, and FoM_T includes the tuning range. PN is the phase noise in dBc/Hz at the specific offset. Δf is offset frequency from carrier. f_0 is the operating frequency. P_{DC}, Power consumption is relative to 1 mW. TR is frequency tuning range relative to 10% as 10% tuning range is commonly accepted in the design of oscillator.

2.1.6 PVT and Monte-Carlo Simulation

The acronym PVT stands for Process, Voltage, and Temperature. To ensure that our chip works in all possible environments, such as the winter time in high latitude areas could be at -40°C and the Sahara Desert at 60°C, we simulate it under a variety of process, voltage, and temperature conditions that the IC may encounter after fabrication. These are referred to as corners. All three of these parameters have an effect on the cell's delay. We will examine each parameter in depth and its impact on delay. The term "process variance" refers to the deviation in the characteristics of a transistor during fabrication. During the manufacturing phase of a die, the area of center and boundary will exhibit varying degrees of process variance. This occurs because the layers that will be manufactured cannot be identical in the die. As we move away from the die's core, the sizes of the layers will vary. Variation in the process occurs gradually. It cannot be hasty. Process variation varies by technology but is more pronounced in smaller node technologies($\leq$65nm). The following are a few critical factors that can result in process variation: i)UV light wavelength; ii)Manufacturing defects. The following are the effects of process variation: i)Variation in oxide thickness, ii)Variation in dopant and mobility, and iii)Variation in transistor width, weight, and other dimensions. Nowadays, a chip's supply voltage is extremely low. Assume the chip is running at 1 volt. As a result, there is a possibility that at any point in time, this voltage will fluctuate. It is

capable of reaching 1.1V or 0.9V. We assume voltage variance to account for this scenario. IR drop is a significant cause of supply voltage fluctuations. The IR drop is caused by the current flowing over the power grid's parasitic resistance. The IR drop lowers the supply voltage below the appropriate level. The second significant cause of voltage variance is supply noise caused by parasitic inductance, resistance, and capacitance. The voltage bounce is caused by the current flowing through parasitic inductance. Both of these effects, when combined, can result in voltage drops as well as voltage overshoot. Any chip operates on an external supply voltage. It may originate from a direct current source or a voltage regulator. Voltage regulators may not maintain the same voltage over time. It may go above or below the predicted voltage, causing current to shift and the circuit to run slower or faster than it did previously. As a result of all of these considerations, we must consider voltage variance. Temperature variance is measured in relation to the junction, not the ambient temperature. Temperatures at the chip's junction can differ widely, which is why temperature variation must be considered. The delay of a cell increases as the temperature rises. However, this is not valid for all nodes in technology. This is not the case for deep sub-micron technologies. This is referred to as temperature inversion.

The foundation of a Monte Carlo simulation is the inability to calculate the likelihood of different outcomes due to random variable intervention. As a result, a Monte Carlo simulation is based on continuously repeating random samples in order to obtain desired results. Monte Carlo simulations take an unknown variable and assign it a random value. After that, the model is run and a result is returned. This procedure is repeated indefinitely in order to assign the attribute in question a large number of different values. After the simulation is completed, the results are summed to obtain an estimation. The Monte Carlo analysis is similar to the sweep analysis in that it is a swept analysis with related child analyses. Monte Carlo analysis makes use of "statistics blocks," which specify the statistical distributions and correlations of netlist parameters. Each iteration of the Monte Carlo analysis generates new pseudo-random values for the specified netlist parameters (according to their specified distributions), and then the list of child analyses (such as DC gain, unity gain frequency, or amplifier slew rate) is performed. Child analyses are correlated with expressions. These expressions, which the user creates as scalar calculator expressions during

Monte Carlo analysis setup, can be used to determine circuit metrics such as an op-amp's slew rate. These expression results can differ during a Monte Carlo analysis as the netlist parameters vary for each Monte Carlo iteration. Thus, Monte Carlo analysis becomes a method for examining and forecasting circuit output variations that affect yield. You may define batch-to-batch (process) and per-instance (mismatch) variations for netlist parameters using the statistics blocks. These statistically varying netlist parameters can be referenced in the main netlist through models or instances and may reflect IC manufacturing process variation or part variation for board-level designs, for example.

2.2 Rotary Travelling-Wave Oscillator

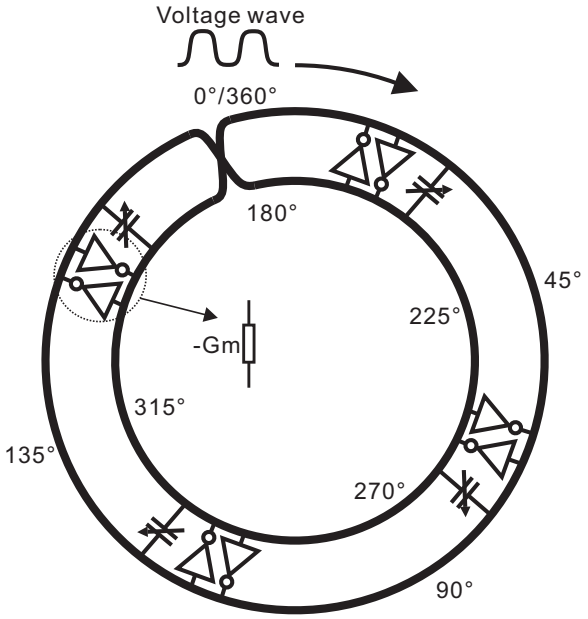


Figure 2.6: A typical RTWO

Fig. 2.6 is a typical RTWO. A Möbius loop transmission line ring is constructed as the foundation. Back-to-back connected inverter pairs are working as amplifiers to compensate for the energy loss. In this example, RTWO has four nodes. The varactors can tune the operating frequency. A voltage travelling wave travels on the Möbius loop with round trips.

Any two points on the ring always have a fixed phase difference. Every two round trips are one cycle of output signal because of the cross-connection(180°). RTWO outputs a square signal because odd mode harmonics exist on the loop. The number of nodes can be as low as two or as many as possible depending on the design.

2.2.1 Cross-coupled Pair

In RTWO, cross-coupled inverter pairs restore energy to compensate for the energy loss in circuits. The balance between the energy loss and power supply is what keeps RTWO running.

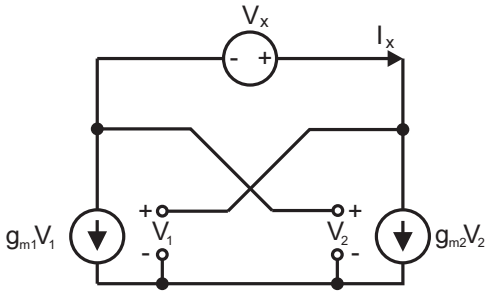


Figure 2.7: Equivalent of cross coupled pair

The equivalent circuit of a nMOS cross-coupled pair is shown in Fig. 2.7, where $V_1 - V_2 = V_X$ and $I_X = -g_{m1}V_1 = g_{m2}V_2$. Then, the impedance seen by V_X is

$$\frac{V_X}{I_X} = -(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}). \tag{2.13}$$

If $g_{m1} = g_{m2} = g_m$, Eq. (2.13) can be simplified as

$$\frac{V_X}{I_X} = -\frac{2}{g_m}. \tag{2.14}$$

In addition, for nMOS and pMOS cross-coupled pair connected together, g_{mp} and g_{mn} are the trans-conductance of pMOS and nMOS. As nMOS and pMOS are connected with a

parallel connection. The the total negative trans-conductance is expressed as

$$\frac{V_X}{I_X} = -\frac{2}{g_{mp} + g_{mn}}. \tag{2.15}$$

Fig. 2.8 shows the negative transconductance from cross-coupled pair. When $V_a = V_b$, the negative transconductance is the maximum which is -20mS in this example. When $|V_a - V_b| = VDD$, the negative transconductance drops down to a small number, $-G_m$ is non-linear.

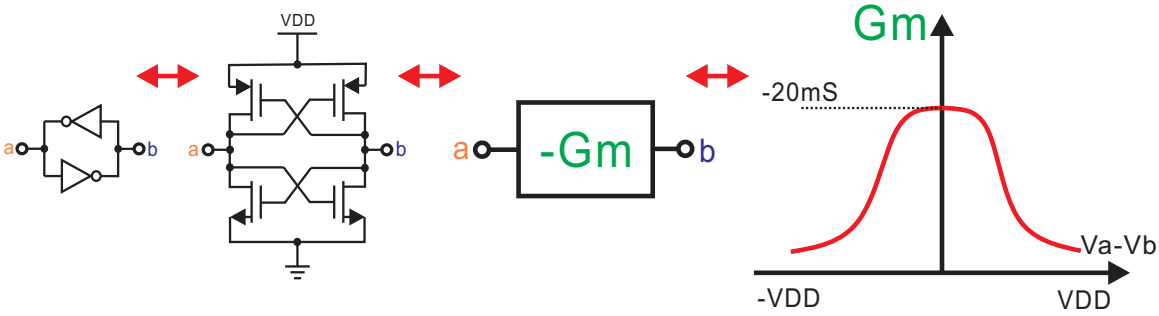


Figure 2.8: Cross-coupled pair and -Gm

2.2.2 Transmission Line

As the whole ring is composed of transmission line (TL) segments, in this section, the transmission line will be discussed briefly. Shown in Fig. 2.9, a coplanar transmission line is represented by a set of RCLG lumped model.

RLGC model shows that TL's electronic and magnetic field are described as resistors, capacitors, and inductors network. Owing to the interaction of electromagnetic fields between two unshielded transmission lines in near proximity, power may be coupled from one line to the other. Coupled transmission lines are often thought to run in the TEM mode, strictly accurate for coaxial lines and striplines but only roughly true for microstrip lines, coplanar waveguides, and slotlines. Coupled transmission lines can accommodate two different propagating modes, which can be used to create a range of useful directional couplers,

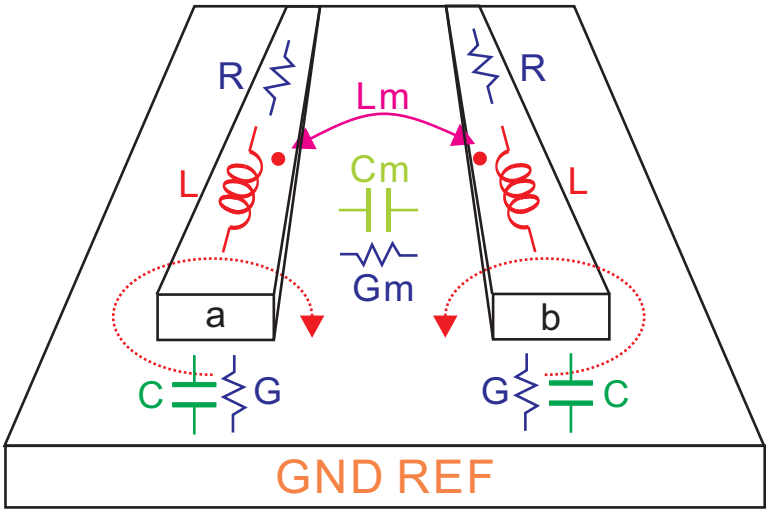


Figure 2.9: Transmission line RLGC model

hybrids, and filters. The coupled lines are symmetric, which means the two conducting strips are the same width and closed to each other, making the analysis of their activities easier. The transmission line model is simplified to a lossless TL model in Fig. 2.10.

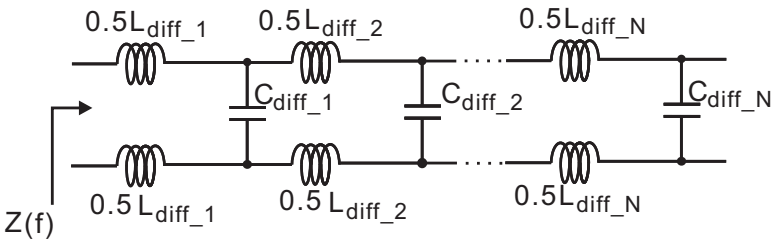


Figure 2.10: Lumped model of transmission line

The phase velocity of wave propagation in coplanar transmission line is defined as [31]:

$$v_p = \frac{1}{\sqrt{L_0 C_0}} \tag{2.16}$$

L_0**(H/m)** : parasitic inductance per unit length.

C_0**(F/m)** : parasitic capacitance per unit length.

v_p**(m/s)** : phase velocity.

As the RTWO is made of several transmission line, which is defined as transmission line segments. The phase velocity of the travelling wave can be obtained from following. Now, define:

N : number of nodes(same as segments).

l_{seg}**(m)** : length per segment.

f_{op}**(Hz)** : operating frequency.

$l_{ring} = Nl_{seg}$**(m)** : total length of the ring.

$L_{ring} = Nl_{seg}L_0$**(H)** : total parasitic inductance.

$C_{ring} = Nl_{seg}C_0$**(F)** : total parasitic capacitance.

Because every two circular travellings is one period of the output signal, phase velocity divided by twice the total length is the operating frequency. Thus, the operation frequency can be obtained as

$$f_c = \frac{v_p}{2l_{ring}} = \frac{v_p}{2Nl_{seg}} = \frac{\frac{1}{\sqrt{L_0C_0}}}{2Nl_{seg}} = \frac{1}{2\sqrt{Nl_{seg}L_0Nl_{seg}C_0}}. \tag{2.17}$$

Defining $L_{ring} = Nl_{seg}L_0$ and $C_{ring} = Nl_{seg}C_0$. Eq. (2.17) can be simplified as:

$$f_{op} = \frac{1}{2\sqrt{L_{ring}C_{ring}}}. \tag{2.18}$$

However, in a practical RTWO design, C_{ring} also includes the capacitance from latches, tuners, and output buffers. Defined as (2.19):

$$C_{ring} = NC_{tlseg} + NC_{latch} + N_{buffers}C_{buffer} + N\Delta C_{tuner}. \tag{2.19}$$

It follows that

$$f_{op} = \frac{1}{2\sqrt{L_{ring}(NC_{tlseg} + NC_{latch} + N_{buffers}C_{buffer} + N\Delta C_{tuner})}}, \tag{2.20}$$

When ΔC_{tuner} is minimum, f_{op} is maximum vice versa. The average phase velocity can also be calculated as following:

$$v_{p(avg)} = 2l_{ring}f_{op} = 2Nl_{seg}f_{op}. \tag{2.21}$$

For example, in the RTWO design[27], $v_{p(avg)} = 16.4GHz \times 2 \times 16segs \times 90um/seg \approx 0.16c$ (c is v_p of light in vacuum)

2.2.3 Idealized Model of RTWO

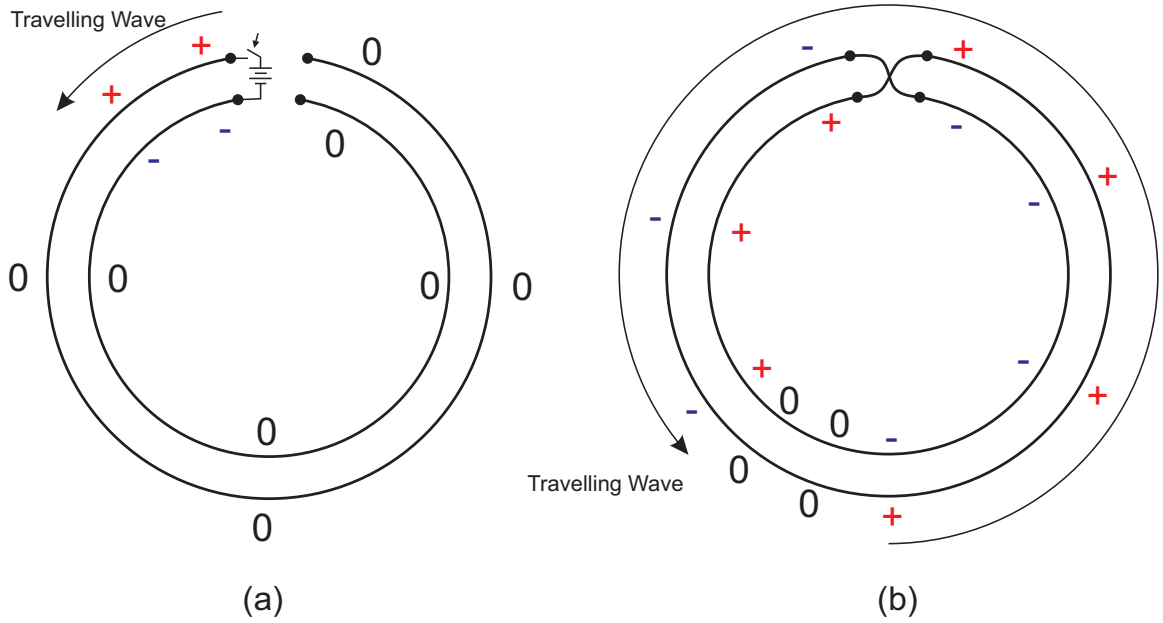


Figure 2.11: (a) An open loop differential TL gets energy from a battery via a switch, (b) The open circuit been replaced by a cross-connection

Fig. 2.11 reveals the operation of RTWO. Fig. 2.11(a) shows an open-loop differential TL drives by a battery through an ideal switch. A voltage wave started propagation immediately after the switch closed. Now, replace the open terminal with a cross-connection, as shown in Fig. 2.11(b). Assume the differential transmission line is lossless, which means the amplitude of the travelling wave is constant. After a while, the wave keeps running on the

Möbius loop cycle by cycle. Every two rounds, trips provide a full clock cycle. In practice, the battery and switch in Fig. 2.11(a) is replaced by multiple back-to-back connected inverter pairs. These amplifiers work as energy restorer to compensate for the TL energy losses.

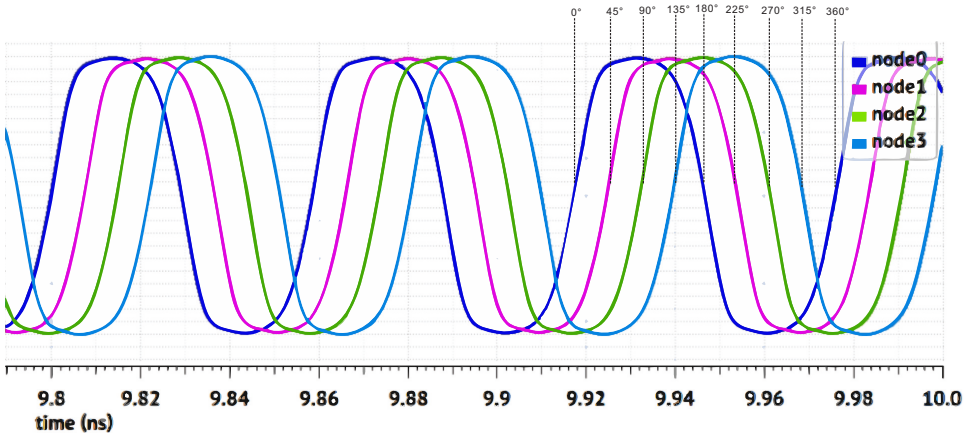


Figure 2.12: Time domain waveform of a 4-nodes RTWO.

Fig. 2.12 shows the time-domain waveform of a four nodes RTWO. This RTWO has a square-like waveform. Because this output is caught every four nodes, the phase shift is 45° between each of them. The waveform is similar to square wave because differential transmission lines pass broadband signal. The odd harmonics sharpen the rising and falling edges of the signal.

2.3 Literature Review

In this section, four previous researches of RTWO will be discussed and reviewed.

Wood(2001)[11] released the first paper of RTWO. In this paper, first, the author illustrated the theory behind the Möbius loop. He used a circular transmission line as an example. When one terminal of the transmission line is driven by a voltage source, the energy of the voltage source propagates on the transmission in the form of a travelling wave. Changing this transmission line into a closed-loop with a Möbius connection, the voltage wave generates a rotational waveform because of the Möbius effect, but real TLs are lossy.

The author added energy restoring inverter pairs on the transmission line ring. Second, the author mentioned a concept called "Rotary Oscillator Arrays(ROAs)". Once multiple RTWO couples each other in a way that is similar to injection-locking, phase-locking can be expected. All the points in the ROAs have a known phase shift. Phase locking can be used to distribute a clock signal over a larger die area with low clock skew. The author did not actually verify large scale ROAs on CMOS, but a small scale ROA with 5 RTWOs were verified. Third, he discussed the field and current near the transmission line. The current in parallel coplanar lines is inverted to each other and having the same strength. Because two same strength currents are inverted in coplanar lines, the H-field is cancelled on the outside of the coplanar lines. In the middle of two lines, the H-field is doubled. It is evidence that the magnetic field created by the TLs are relatively strong. It is really necessary to consider other devices' placement because other devices might be affected by the H-field. Fourth, the prototype uses $1-\mu$ m Al/Cu top metal, M5, for making the transmission line because this metal layer has the lowest resistivity. The RTWO segment was also modelled

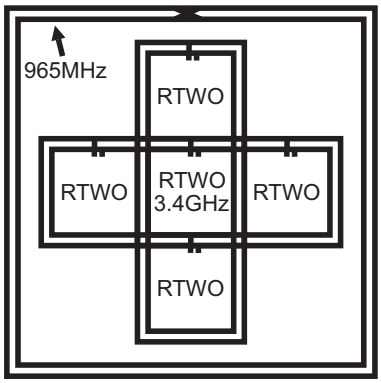


Figure 2.13: The scheme of the design.

by using a lumped circuit, where an RLC network was utilized to provide a great deal of intuition for the design of RTWOs. At each RLC segment, an inverter-based amplifier was inserted to compensate the loss, and to provide the start-up condition. A 0.25-μm CMOS test chip were designed, consisting of five small rings and one large ring with 3.4-GHz and 965-MHz, respectively. Fig. 2.13 shows the structure of the design. The outer ring used

12000 μm with 60 μm width on a 120 μm pitch with 128 62.5 μm PMOS and 25 μm NMOS inverter pairs distributed along the ring. On the other hand, the length of the small ring was 3200 μm with width of 20 μm and pitch of 40 μm. The total chanel widths for the small ring was 2000 μm for NFET and 5000 μm for PFET evenly distributed through 40 pairs of inverters. 5.5-ps jitter and 34-dB power supply rejection ratio (PSRR) was measured. Lastly, it is noticed that ROAs is suitable for clock distribution through a large chip while the total power consumption can be managed as lower than using a traditional clock distribution tree. Unfortunately, the large silicon area was one drawback.

Followed by Bai(2016)[4], another RTWO based on GF 130-nm CMOS process was proposed, where there were significant improvements. First, the proposed on-chip microstrip line resonator was characterized through ADS, presenting a high Q-factor at the high frequency. From the simulation, the Q-factor of the microstrip line can be as high as 20 at several gigahertz. In comparison with on-chip inudctor, the Q-factor of microstrip line is visibly higher than spiral inductor. In the forgoing discussion, it is preferable to having low loss resonator such that the PN can be reduced. The second contribution in this work was the use of injection-locking technique to further improve the PN performance. One of the properties of the injection-locking is pull the PN of the oscillator which is under injection-locked to the level of the incident which is from a "clean" source. Though featuring the PN improvement, this phenomenon is weakened with the increase of the deviation from the free-running frequency of the oscillator. The worst case is injection-pulling instead of injection-locking happens in the oscillator, leading to additional beat signals at the output and subsequently higher PN. Injection locking and pulling effects can be seen in a variety of physical systems, but they are most often associated with electronic oscillators and laser resonators. Injection locking has been used in the design of early television sets and oscilloscopes in a beneficial and clever way, enabling the equipment to be synchronized to external signals at a low cost. Injection locking has also been used in frequency doubling circuits with high performance. Injection locking and pulling, on the other hand, can degrade the output of phase-locked loops and RF integrated circuits if it is done incorrectly. Third, the author introduced a tuning control strategy to tune every node separately. RTWO can be treated as a lossless transmission line loop with a tunable phase velocity. This technique

not only slows down the phase velocity at a section of the ring but also speeds up the phase velocity at some other sections. The design diagram is shown in Fig. 2.14. The RTWO

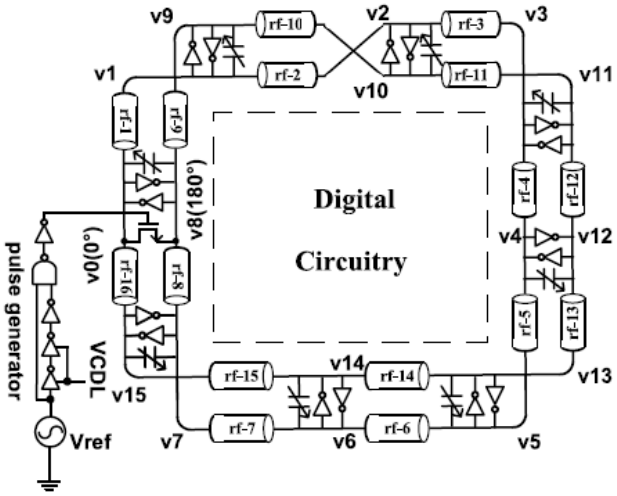


Figure 2.14: RTWO with pulse injector [4].

has eight nodes from N1 to N8(N1,2,3,4,5,6,7,8). The tuning bank at N1-4 is tuned bigger capacitance, and the tuning bank at N5-8 is tuned smaller capacitance. At the same time, the average phase velocity stays at the same number. This can also be called 'unsymmetric tuning'. The proposed RTWO uses a 7-bits binary-controlled high-Q switched MIM cap for course tuning. It is worth noting that the binary-weighted MIM caps provide the majority of the loading capacitance, while the thermometer weighted complementary varactor pairs are only used for medium and fine frequency tunings, resulting in a higher tank Q from 1.7 to 2.0 GHz range. Complementary varactor pairs are used to ensure monotonicity by allowing frequency overlaps. MIM caps are usually less sensitive to temperature fluctuations, resulting in better frequency-tuning efficiency with fewer varactors and more MIM caps. Fourth, this RTWO is controlled by a microprocessor. the RTWO free-running frequency can be calibrated using an on-chip microprocessor (μP). A subsampling switch is used to mix the free-running frequency down to a low frequency, which is then measured with an ADC. The mixed down signal is at dc, while the free-running frequency is an exact harmonic of the crystal frequency. The ADC output is used to calculate the free-running frequency, and

(μP) then changes the free-running frequency by adjusting the oscillator's varactors. Fifth, this method only necessitates a simple switch, a low-resolution ADC, and a basic 8-bit μP, all of which can be built in a small amount of space using an advanced CMOS process. At initialization, the free-running frequency is tuned, removing any process differences from chip to chip. A temperature sensor and a supply voltage sensor can be mounted on the chip and read by the μP, which can then change the oscillator's varactors using frequency readings taken during production testing or the tuning circuit. In this scenario, injection locking will need to be temporarily disabled in order to tune the free-running frequency. The RTWO can be biased at a minimum of 1.14-V supply voltage in free-running mode, with the oscillator core drawing 24.9 mA. The injection signal was produced by a signal generator. With a square wave of 12 dBm, the RTWO can be injection-locked. The range of pulse injection-locked RTWO synchronization was determined and simulated at 27 °C and measured at 0 °C, 27 °C, and 70 °C. The RTWO outputs are connected to 50-Ohm off-chip transmission lines via on-chip buffers. Mismatches in the on-chip buffers and mismatches in the on-chip and off-chip traces create an output amplitude discrepancy. When designing a circuit layout, all structures should be symmetric if possible.

Takinami(2011)[5] built a phase-to-digital converter based on all-digital PLL driven by using of RTWO. Because RTWO has an ambiguous start-up direction issue, the multi-phase output is unsure. A direction detector and a look-up table(LUT) were designed to determine the direction of the wave propagation and map the corresponding node signal to LUT so as to find out the proper phase of the output, as shown in Fig. 2.15. Thermometer

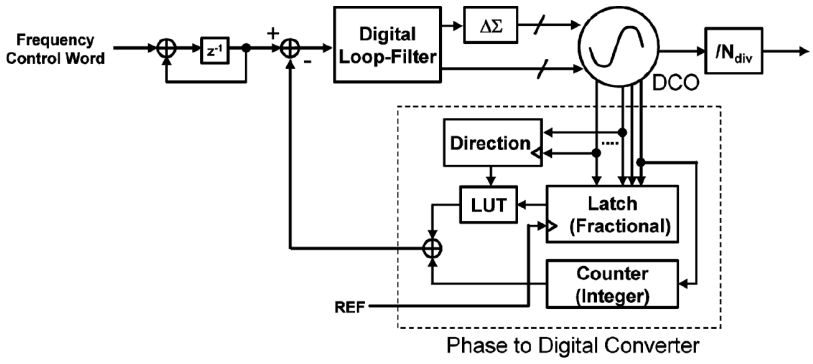


Figure 2.15: Simplified block diagram of the proposed ADPLL [5].

code is similar to the output of a thermometer. In thermometer code, a value representing the number 'N' has the lowest 'N' bits set to '1' and the remaining 'N' bits set to 0. Thus, to shift from N to 'N+1', simply replace the rightmost '0' to a '1'. This is how the term "thermometer code" originated. Thermometer code is used in a variety of circuits, including flash ADCs and time-to-digital converters (TDC). In Takinami's design, the latch output has the digital codeword [1,1,1,1,1,0,0,0] at the rising edge of the reference clock. This pseudo-thermometer code can be used to decipher the fractional phase since it reflects the instantaneous phase of the oscillation. By comparing the phase of non-adjacent taps, the direction of the oscillation can be calculated. To decode the pseudo-thermometer code into binary code, either a clockwise or counter-clockwise look-up table (LUT) is used, depending on the direction. Counting the number of oscillation cycles with a high-speed counter is a simple way to get the integer step. The writer did not address the ambiguous startup direction by modifying the RTWO, but he chose to modify it by configuring digital logics. The LUT solution is only possible to use in some situation, such as digital logic. However, it is not a solution that inherently manipulates the travelling wave to run in a fixed direction. The design was implemented on a 65-nm CMOS process. The active area is $780 \times 780 \mu m^2$. The digital logic is housed within the resonator, which takes up just 10% of the space in the prototype. A 64-pin open cavity package houses the chip. Die-bonding for the secure ground is done with the additional 24 pads. With a 1.5 V supply, the the digital-controlled oscillator (DCO) was tuned from 2.6 to 4.5 GHz, consuming 22 mA. At a 20 MHz offset, the phase noise of the free-running DCO is -148 dBc/Hz. The quality factor deterioration caused by unaccounted parasitics in the layout is the main cause of this discrepancy. The resonator's quality factor is calculated to be 4, as determined by lowering DCO core currents before oscillation stops, which is roughly half of what we predicted by design. Based on the post-analysis using the electromagnetic (EM) simulator, it was discovered that closed metal loops under the resonator, such as guard rings for active systems, degrade the quality factor of the transmission lines by more than 25%. Since the DCO core is running in the current region due to the low-quality factor of the tank, a 1.2 V power supply is preferred to minimize overall power consumption. Unfortunately, since the transistors' size in the DCO has been designed for 1.5 V operation, the oscillation cannot be maintained at a lower supply voltage.

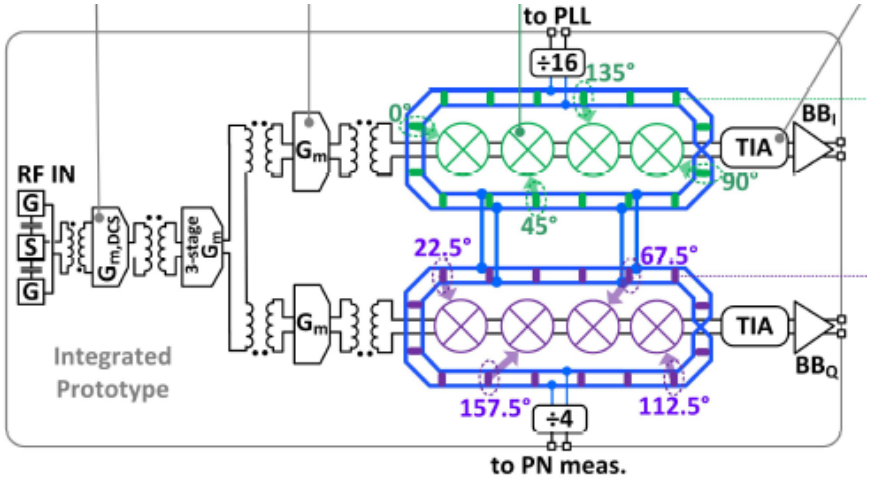


Figure 2.16: Block diagram of the proposed coupled-RTWO-based SHRX [32].

At the conclusion, the author concludes that applying the RTWO architecture simplifies the ADPLL.

Vigilante(2018)[32] developed a RTWO based 5G E-Band receiver front-end, shown in Fig. 2.16. This RF receiver works at a centre frequency of 75.1 GHz with a 20.5% frequency tuning range. To maintain a constant bit error rate, higher order quadrature amplitude modulation (QAM) signals need a higher signal-to-noise ratio(SNR). Consequently, phase noise(PN) in the local oscillator(LO) is becoming a major limiting factor in the system's maximum spectral performance, a crucial specification for 5G. A case study for a direct conversion E-band receiver (RX) that targets 10^{-6} BER with 64-QAM was presented in a study. To achieve an acceptable SNR, a LO solution with a PN of -119-dBc/Hz at a 10-MHz offset from the carrier is needed. This is a difficult number, particularly when combined with the wide tuning range (TR) required for this application (over 19 %). Direct-conversion subharmonic receivers (SHRXs) was employed in this design. SHRX architecture provides several benefits. First, main mm-Wave direct-conversion transceiver limitations like LO feedthrough and power amplifier (PA) pulling are greatly reduced. Second, there is no need for image rejection filters or IF gain stages. Third, the LO distribution network operates at a lower frequency, resulting in considerable power savings for the LO buffers that drive the mixers. The LO operates at a fraction of the input RF frequency, which is the fourth and most critical feature. As a result, the separation between LO and RF signals

improves dramatically. Furthermore, for a given TR and technology, the oscillator PN and FoM were boosted. When a relatively high Q LC tank is used, and the active devices of the oscillator core do not reach the triode field. However, for a given fractional TR, integrated mm-Wave oscillators display a substantial degradation of the measured FoM. The following are the main explanations. First, the lower quality factor of the capacitive tuning elements degrades the tank Q for a given TR, resulting in a 6-dB PN penalty for every halving. Second, the active devices' parasitic capacitance becomes a significant portion of the overall tank capacitance, necessitating the use of even more lossy tuning elements to achieve the same TR. Third, the negative impact of transistor gate resistance becomes more apparent, necessitating a higher transconductance to ensure stable startup conditions and, in turn, a higher parasitic capacitance. Fourth, when active devices reach the triode region in the absence of a second-harmonic resonance in typical mode, their current efficiency drops, and their noise contribution rises. At last, the 5G receiver front end achieved the requirement of the modulation under the 28-nm CMOS process. This study shows the potential of RTWO in high-speed mm-Wave transceivers by a real application.

2.4 Design Procedures

In this section, all tools used in the design and the design procedure will be introduced.

2.4.1 Design Tools

Cadence Virtuoso is a well-known IC design software suite in the IC industry. Virtuoso provides schematic, layout, and simulator for all semiconductor devices. Analog Design Environment(ADE) is part of Virtuoso. Spectre RF is its built-in simulation software. In both the time and frequency domains, the Cadence® Spectre® RF offers various RF analyses based on silicon-proven simulation engines. Mixers, transceivers, power amplifiers, dividers, switched capacitors, filters, and phase-locked loops are among the many RFIC varieties that can be checked using a wide range of analyses (PLLs). The Spectre RF includes a variety of

noise and distortion analysis tools. It also offers application-specific analysis, such as wireless analysis, for evaluating system-level output with standard-compliant signal sources. The Cadence Virtuoso® ADE Product Suite's close integration allows for exhaustive simulation and the setup of multiple tests for multiple conditions.

The EM simulator of this project is Momentum as a part of Keysight ADS. Momentum is a component of Advanced Design System, assisting design and test modern communications systems devices. Momentum is an electromagnetic simulator that calculates S-parameters for microstrip, slot-line, stripline, coplanar waveguide, and other planar circuit typologies. Typologies are connected between layers using vias and air-bridges, allowing you to simulate multi-layer RF/microwave printed circuit boards, hybrids, multi-chip modules, and integrated circuits. Momentum provides a comprehensive range of tools for predicting the performance of high-frequency circuit boards, antennas, and integrated circuits. Momentum Optimization turns Momentum into a full-fledged design automation method. The Momentum Optimization method automatically adjusts geometry parameters to help you find the best structure that meets your circuit or device's output goals. You can also perform Momentum optimizations from the schematic page by using (parameterized) layout components. Momentum Visualization is a feature that allows users to see and animate current flow in conductors and slots, as well as display both 2D and 3D representations of far-field radiation patterns in simulation performance.

TSMC 130-nm RF CMOS process has one thick metal layers and seven thin metal layers. The thick top metal layer is generally used for making inductors, and the other layers are generally used for power and signals. The design kit provides the substrate definition needed by the EM simulator. TSMC has long provided foundry-qualified design-rule check (DRC), layout-vs.-schematic (LVS), and parasitic-extraction rule decks, as well as Spice models for Mentor's Eldo Spice simulator. TSMC supports custom/mixed-signal IC design flow, starting with this latest release of the 130-nm mixed-mode process. This package contains a symbol library for Design Architect-IC schematic capture as well as parameterized layout generators for the IC Station layout editor.

Global Foundry 130-nm RF CMOS process has two thick metal layers and six thin metal layers. Two thick top metal layers are generally used for making inductors, and the other layers are generally used for power and signals. This design was implemented on 1.2V supply voltage.

2.4.2 A Step-by-step Design Procedure

Building a model of a microwave network is challenging work because manually solving Maxwell equations is not always possible. However, with finite element analysis, a complicated microwave network can be numerically calculated. A visualized design procedure is shown in Fig. 2.17. The following description is the co-design procedure based the tools

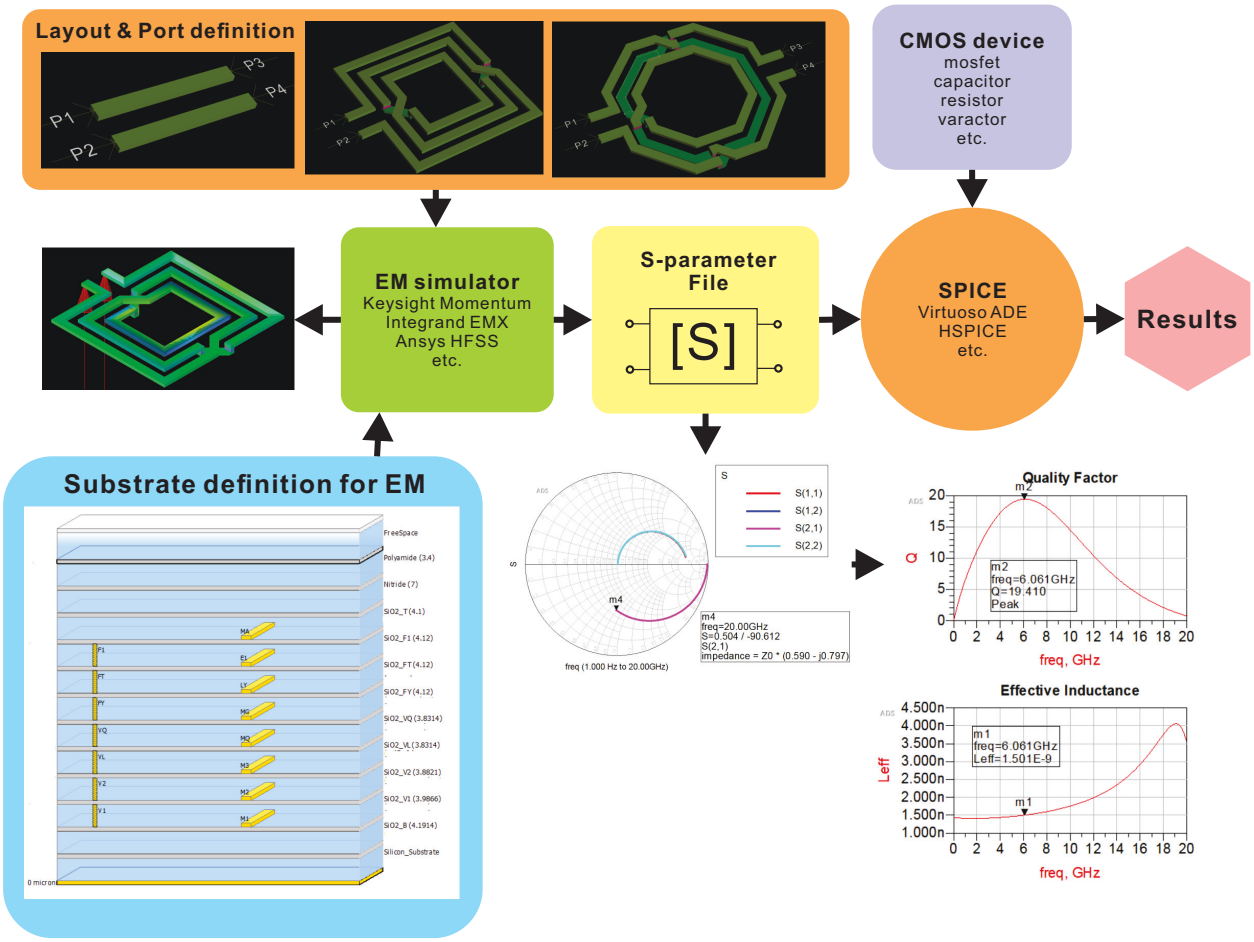


Figure 2.17: Design process with EM simulator

which are used in this research.(same as Fig. 2.17):

Create a physical design The physical dimensions of a planar design, such as a patch antenna or the traces on a multilayer printed circuit board, are the first thing to consider. A specification can be entered into Advanced Design System in three ways: Create a physical structure from a diagram. The layout is used to create the template. Import a layout from another design framework or simulator. Files in a range of formats can be imported into the simulator configuration.

Define the substrate characteristics A substrate is a material that the circuit is built on. A CMOS IC process, for example, is made up of metal layers, insulating or dielectric material. Covers or open designs that radiate into the air are examples of other designs. To simulate a design, you will need a complete substrate specification. The number of layers in the substrate and the composition of each layer is included in the substrate description. This is also where you determine the metal properties of your physical design layers and where you place them within the substrate.

Assign port properties Ports allow you to inject energy into a circuit, which is needed for circuit analysis. When you build a circuit, you apply ports to it and then allocate port properties in Momentum. Depending on your application, you can use a variety of different types of ports in your circuit.

Set up and generate a circuit mesh A mesh is a pattern of rectangles and triangles applied to a template to break it down into small cells. To effectively simulate the pattern, you will need a mesh. You can configure the mesh with a number of mesh parameters, or you can leave the default values and let Momentum create an ideal mesh for you.

Simulate the circuit You create a simulation by defining the parameters of a frequency plan, such as the simulation's frequency range and sweep form. You run the simulation once the setup is complete. The currents in the design are determined using Green's functions computed for the substrate, as well as the mesh pattern. The currents are

then used to calculate S-parameters. If the Adaptive Frequency Sample sweep form is selected, a fast, accurate simulation based on a rational fit model is developed.

View the results S-parameters or fields are used to save data from a Momentum simulation. To see S-parameters and far-field radiation patterns, use the Data Display or Visualization. S-parameters, currents, far-fields, antenna parameters, and transmission line data can all be viewed and analyzed using momentum visualization. A number of 2D and 3D plot formats are available for data analysis. Some data is presented in a tabular format.

Analyse the results ADS provides templates in its data browser.

Import S-parameter file into Virtuoso design Virtuoso provides an n-port component that offers S-parameter files as its input. Using the n-port component to replace the passive devices simulated in ADS, the n-port component will act as the components, such as inductors, TL or transformer.

Setting up ADE environment In VCO design, several simulation methods are usually used, such as transient(trans), periodic steady-state(pss), phase noise(pnoise), alternative current(ac) analysis, etc. 'pss' and 'pnoise' simulation are used to measure phase noise. transient simulation is used to measure power, current, waveform and operating frequency.

Run SPICE simulation Run SPICE simulations and do more analysis on the co-design, such as transient, dc, ac and noise.

2.4.3 Wafer Testing Platform

When it comes to the test, there are multiple options. A common practice widely appreciated in academia is wafer testing, which is also adopted in this research work.

A mechanical probe station is used to physically acquire signals from a semiconductor device's internal nodes. The probe station makes use of manipulators to precisely position thin needles on the surface of a semiconductor chip. If the device is electrically activated, the

mechanical probe acquires the signal and displays it on an oscilloscope. Mechanical probe stations are often used in the study of semiconductor system failures. Mechanical probes are classified into two types: active and passive. Passive probes are usually made of a fine tungsten needle. Active probes incorporate a FET system on the probe tip to greatly minimize circuit processing. In academic research on electronics and materials science, mechanical probe stations are often used. Testing a new electronic product or sample with a probe station is often quicker and more flexible than wire bonding and packaging the device prior to testing. In Fig. 2.18, a probe station is depicted.

Figure 2.18: A probe station[6]

A probe station is made up of a few fundamental components. To begin with, a stage is the central component of a probe station. It is a system used to position the wafer or die. This is typically accomplished by the use of a "Stage" that pushes the device along three axes (X, Y, and Z) and provides a mechanism for rotating the device (Theta). Second, the station must have a means of securely holding the unit, which is typically done with a very smooth, metal surface called a "Chuck." The chuck secures the unit mechanically with clamps or with a light vacuum. If individual dies or stretched, saw wafers are being probed, accessories such as chip trays or frame slides can be added. Thirdly, manipulator or manipulators, probe stations make use of manipulators to precisely place probes on the

device under tested (DUT). Manipulators are typically mounted on a flat surface referred to as a "Platen" and feature a mechanism for quickly positioning and securing probes. Magnets or a vacuum are often used by manipulators to secure them in their proper position. Once secured, the manipulator will precisely place the probe tip in the X, Y, and Z directions, as well as rotate it in some cases. Fourth, a probe tip or tips, alternatively referred to as probe needles, are inserted into a single probe arm and attached to a manipulator. The size and material of the probe tip are determined by the size of the feature being probed and the type of measurement required. Probe tips should make direct contact with the DUT, and probe arms should fit the probe tip. Fifth, a mechanism for visually magnifying the device and probe tip, the final component of the probe station is a mechanism for visually magnifying the device and probe tip, which is sometimes referred to as the system's 'Optics.' This allows the user to position the probe tips precisely and accurately on the DUT. The majority of probe stations employ either a stereozoom microscope or a digital camera, or a combination of the two.

A wafer probe is a device used in the semiconductor production and manufacturing processes to perform electrical tests on wafers. Electrical tests include the transmission of test signals from a measuring instrument or tester to individual devices on a wafer through probe needles or a probe card and the subsequent return of the signals from the device. A wafer probe is used to manipulate the wafer in order to make contact with the device's assigned location. A wafer probe is primarily used in semiconductor development to evaluate the characteristics of prototype integrated circuits, their durability, and defect analysis. When testing devices and processes, a highly precise calculation and evaluation of a test element group (TEG), which consists of transistors, interconnections, and other element devices for an integrated circuit (IC), is performed. This requires the elimination of electrical noise and signal leakage. Additionally, a temperature control feature is necessary to verify operation at extreme temperatures and to evaluate reliability. When evaluating high-power devices, a measurement path with a high voltage and low impedance is also needed. In the semiconductor mass production phase, wafer testing entails TEG testing for the process monitor and a go/no-go test with electrical testing of integrated circuits (ICs).

Chapter 3

A 16-GHz RTWO DESIGN

3.1 Design Objectives

This design targets a Ku-band(16-GHz) frequency rotary traveling-wave voltage-controlled oscillator with a tuning range(TR) larger than 10%. The main task of this design is to verify the idea of the direction controller. Also, the RTWO design offers a very low-noise level and low-power consumption. This RTWO consists of 16 segments. The original RTWO architecture ambiguously decides its direction due to the random noise and PVT mismatches. A customized switch-on sequence determine the direction control. Switching 'ON' or 'OFF' the latches affects the $-G_m$. As the right side Fig. 3.1 shows, time 1, only the latch on the left-top is on. This node creates two travelling waves in both directions. At this point, the amplitude is tiny. Time 2, the latch on top is turned on. The top latch restores the energy to the TL. However, the bottom latch is off, and the travelling wave to the bottom is halted. Time 3, the right-bottom latch is turned on. This latch keeps amplifying the clockwise travelling wave. Finally, all four latches are turned on. As a result, the wave is propagating in the clockwise. The same applies to the counter clockwise wave propagation.

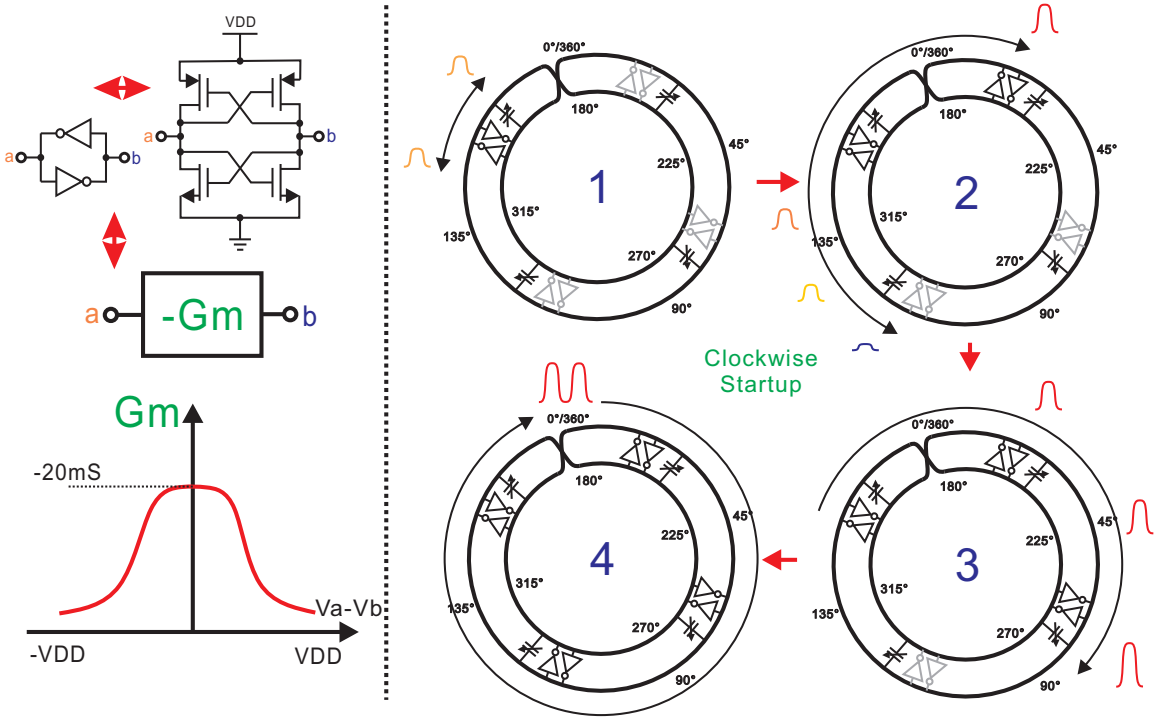


Figure 3.1: Direction control strategy

3.2 The Proposed Circuits

3.2.1 Circuit Topology

The proposed RTWO, as shown in Fig. 3.2, is made up of a differential transmission line (TL) with a cross-connection to form a Möbius loop, with no termination or matching needed. As a result, the load impedance mismatch and signal bandwidth limits are significantly reduced. Unlike the LC oscillator, the RTWO signal holds not only the fundamental harmonic but also the odd harmonic elements, resulting in a square-like waveform. Gain stages are implemented by complementary latches, similar to the simple RTWO, to compensate for resonator loss, sharpening the signal transition while maintaining symmetric waveform to further reduce 1/f noise up-conversion degrading the close-in phase noise. Another way to look at the latch is to use the negative transconductance cell $-G_m$ to reflect the cross-coupled pair's impedance. The $-G_m$ cell compensates the transmission line loss on a periodic basis to keep the wave propagating through the loop. The TL is divided into N segments (N=16) to achieve multiple phases, low phase noise, and low flicker noise cor-

ner frequency. The differential TL stages are mainly responsible for phase noise, according to Chen(2011)[33]. The increased number of amplifiers, on the other hand, has an effect on overall power consumption. Two mechanisms are implemented to balance the power consumption and the PN: i) The amplifiers are inserted once every two TL segments. ii) Binary-weighted switches are used to tune the gated-pair. Varactors are inserted at each TL segment for tuning. The rotary wave will propagate in both clockwise (CW) and counter-clockwise (CCW) directions.

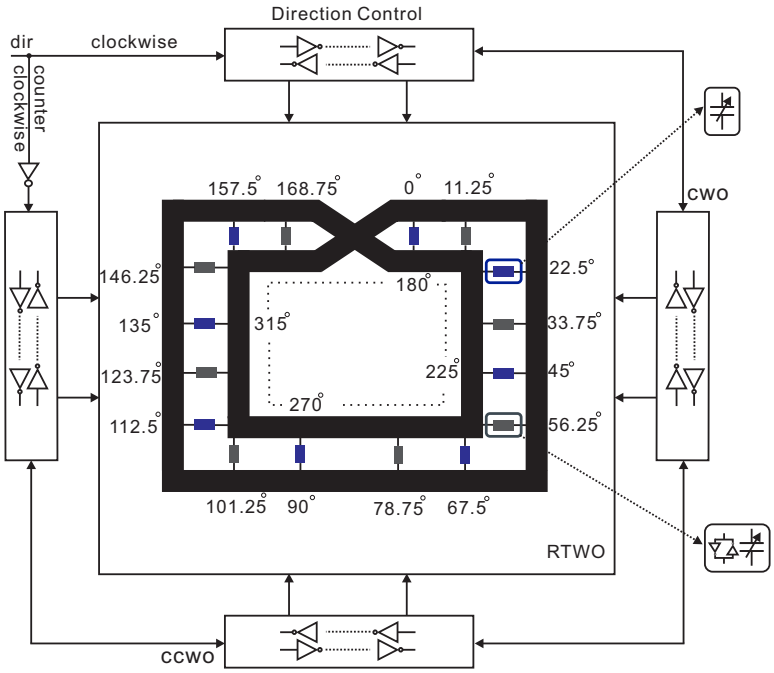


Figure 3.2: Proposed RTWO with direction control circuit

3.2.2 Transmission Line Ring

Fig. 3.3 is a 3-D picture of the TL ring with both sides shielding. The side shielding is also used as power supply wires. To maximize the quality factor(Q) of the resonator, the resonator is made by two thickest top layers. The thickness of the top layer is $4\mu m$, and the second top(used for cross-connection) thick metal layer is $3\mu m$. All segments at the four corners are also cross-connected. The purpose of cross-connection at corners is to reduce

the mismatch of two wires. Because the length of two coupled lines cannot be the same at the turning segments, the crossing connection is used to fix this problem. As the number of cross-connection is an odd number, the loop is a Möbius loop. The inside ring and the outside ring connects to V_{DD} network and ground network. Every pair of the pink points is the vias with latches and varactor connection. This ring takes a $460\mu m \times 460\mu m$ area in total. In Fig. 3.4, three bigger pictures indicate more detailed structures of different

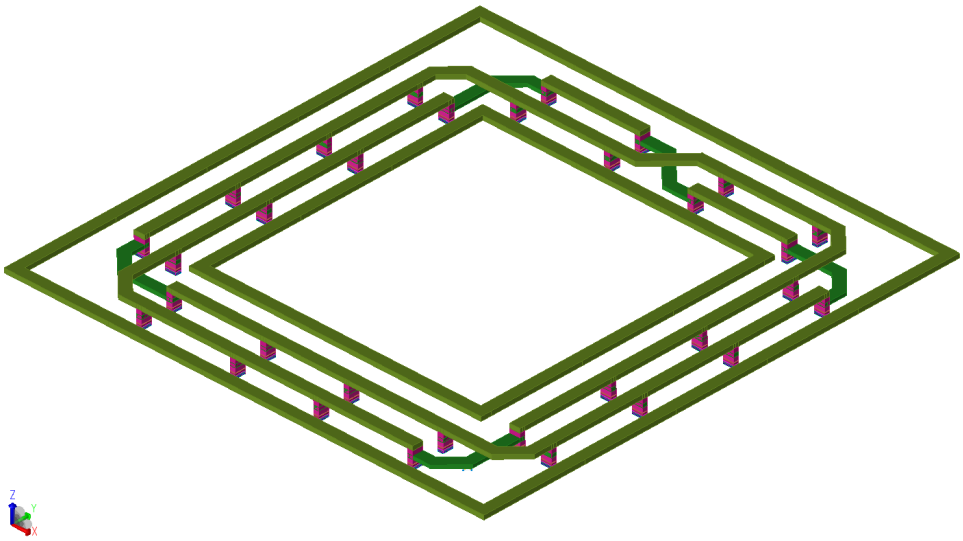
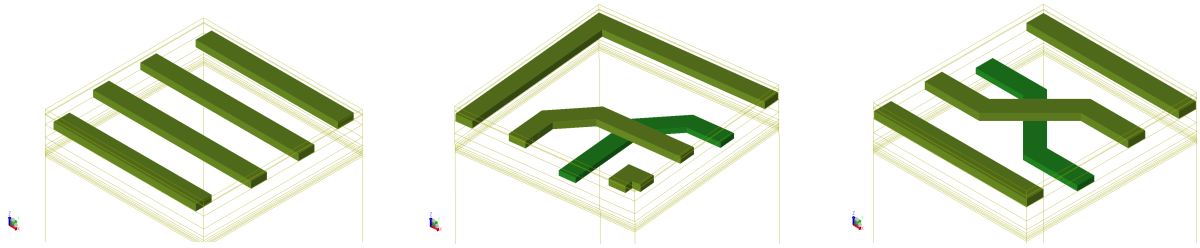


Figure 3.3: 3-D view of the ring

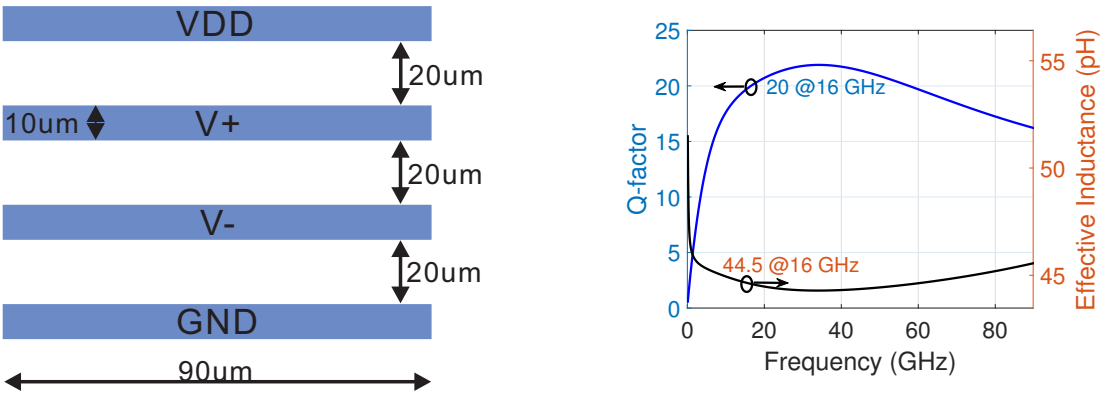


(a) Straight lines **(b)** Turning lines **(c)** Cross-connected lines

Figure 3.4: Pictures of 3 types of segments

segments. Fig. 3.5(a) and (b) are the size, Q-factor and effective inductance of a single TL

segment. At 16GHz, the Q-factor is 20, and the effective inductance of the segment is 44.5pH. Turning segments and cross-coupled lines has lower Q-factor(Q=18) with a similar effective inductance. The low Q in the corners is mainly due to the more parasitic capacitance from the vias.



(a) Size of parallel TL

(b) Q-factor

Figure 3.5: Size of parallel lines and Quality factor

3.2.3 TL Segment Optimization

The optimization work is aided by EM simulations. In this section, three sets of the physical size of coupled transmission lines will be compared. All the number is based on the value at 16-GHz frequency, which is the target frequency of the proposed design. Note, this width is only the best in this process because it depends on the metal thickness, insulator dialectic, and substrate.

The width of the coupled lines is parameterized. As shown in Fig. 3.6, three groups of coupled lines are set to $W = 5\mu m, 10\mu m, 15\mu m$. The blue area is made by top thick metal M8. Transmission line theory can explain the reason. First, the group of $W = 15\mu m$ has a $Q = 19.8$(lower than the group of $W = 10\mu m$) because wider wire brings more parasitic capacitance between the wire and the substrate. The group has more energy loss because of more leaking current to the substrate. Second, the group of $W = 5\mu m$ has the lowest Q

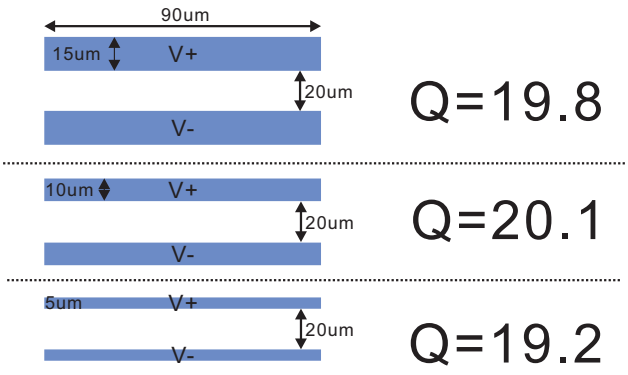


Figure 3.6: Compare the couple TLs with different wire width

because narrow wire has high trace resistance. According to basic knowledge, a large serial resistance results in more energy loss. In summary, $W = 10\mu m$ group offers the highest quality factor, and it is best to choose this width as the first candidate.

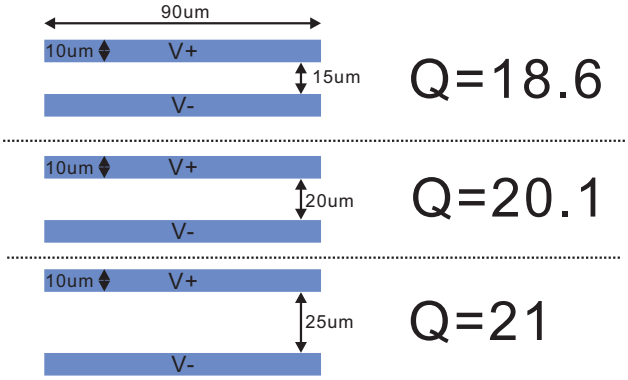


Figure 3.7: Compare the couple TLs with different gaping distance

The spacing of the lines also affect the performance of TL. Three groups of distance setting are shown as Fig. 3.7. The wires in all three groups have the same length and width, but they have different gap space. First, the group on the top shows $Q = 18.6$ when the distance is set to $D_{gap} = 15\mu m$. This is the lowest Q among all three groups. A short distance between two wires increases the parasitic capacitance. A bigger parasitic capacitance decreases the effective inductance. As a result, the Q-factor drops down due to small inductance. Second, the group of $D_{gap} = 25\mu m$ has a $Q = 21$, and this group is received the highest Q among all three groups. However, due to consideration of layout

spacing/area, this gap distance is too wide for the design. Third, the group of $D_{gap} = 20\mu m$ has the best overall result because it balanced the chip area and quality factor. As a result, the gap distance $D_{gap} = 20\mu m$ is chosen in this design.

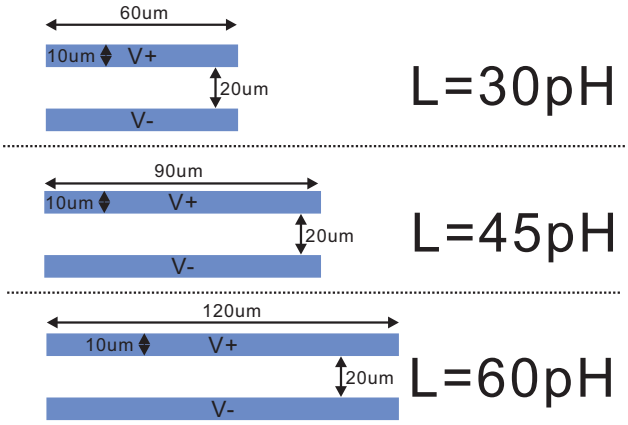


Figure 3.8: Compare the couple TLs with different wire length

The length of a segment significantly influences the inductance. According to [11], the longer length of the wire provides more inductance, which result a lower operating frequency. As discussed in previous chapter, Eq. (2.20) shows that all components on the ring is a part of loading capacitance. As a result, the transmission line must leave a margin for other components in the circuit. Three groups in Fig. 3.8 are being tested. After knowing the capacitance of other components, the second group is chosen because it allows the RTWO running at 16-GHz with a tuning range over 10%.

3.2.4 Circuit Design

Two transmission line segments are shown in Fig. 3.9. The length of all transistors in this section has been chosen to be the shortest possible. The gain stages change power consumption and monitor rotation directions. During start-up, the direction control bit, "dir" and an activate signal, "en" decide the traveling-wave direction. Via a series of inverters, either the clockwise or counterclockwise control of each direction control module is delayed by approximately 1 ns. The direction control signal, when combined with 4-bits

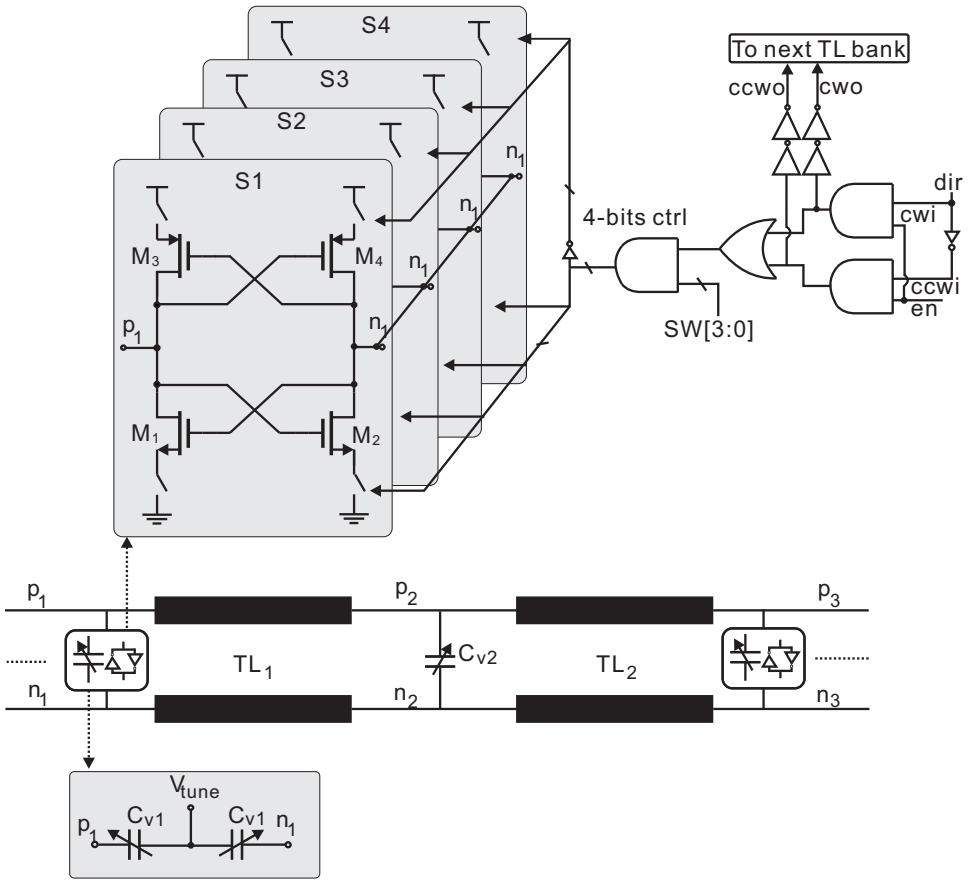


Figure 3.9: Two transmission line segments. S1: W_N = 2.24 μm, W_P = 8.32 μm, S2: W_N = 1.12 μm, W_P = 4.16 μm, S3: W_N = 0.56 μm, W_P = 2.08μm, S4: W_N = 0.28μm, W_P = 1.04 μm, C_{v1}: W/L = 25.6 μm/6.5 μm, C_{v2}: W/L = 12.8 μm/6.5 μm, V_{tune} = 0 to -3 V.

power control signals, sets NMOS/PMOS switches of cross-coupled pairs "ON/OFF" in a sequential manner, allowing the NMOS/PMOS pairs to be switched ON/OFF under the direction control signals and 4-bits power control signals. When the RTWO is oscillating, the direction control bits store the value before the next start-up, and the power control signals decide power consumption. The oscillation's maximum power usage indicates that all four bits are "1" while the minimum power setting keeps the oscillation running. It is worth noting that setting the delay time at random will result in direction control failure. For two gain stages in each transmission line bank to be switched on, the delay cell must be correctly sized to provide 1 ns delay. Monte Carlo simulations revealed that the effective rate of direction control is affected by the delay window. At 15.1 GHz, the minimum delay window is 600 ps, while at 16.9 GHz, it is 200 ps. It has been determined that a 1 ns delay

is necessary for direction control. The tuning is accomplished by the use of an implanted junction varactor. When compared to NMOS varactors, the junction varactor has a twofold Q-factor, which improves phase noise efficiency.

3.2.5 Noise Analysis of the Proposed Design

According to Takinami(2010)[34][35], RTWO can be treated as a superposition of multiple standing-wave oscillators(SWOs). The Möbius structure used in the RTWO can

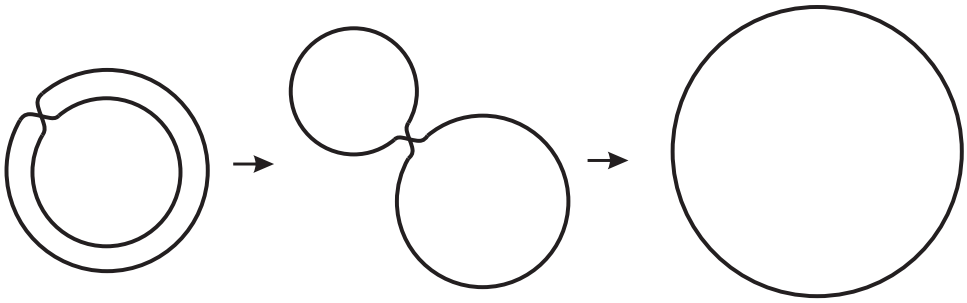


Figure 3.10: Transformation of a Möbius loop to a single loop

be transformed into a single closed loop by unfolding and untwisting its crossover, as shown in Fig. 3.10. We can then recast differential nodes to diagonally opposite nodes on the single closed loop where cells are bound at even spacings, as shown in Fig. 3.11. This simplification provided insight into how to build a phase-noise analysis model. The RTWO can be decomposed into multiple SWOs with even spacing between their $-Gm$ cells, as shown in Fig. 3.12. The $-Gm$ cells of adjacent SWOs should have a timing offset of $T_0/(2N)$, where T_0 is the oscillation period, and a location offset of $\lambda/2N$, assuming we have N segments and the $-Gm$ cells inject current clockwise.

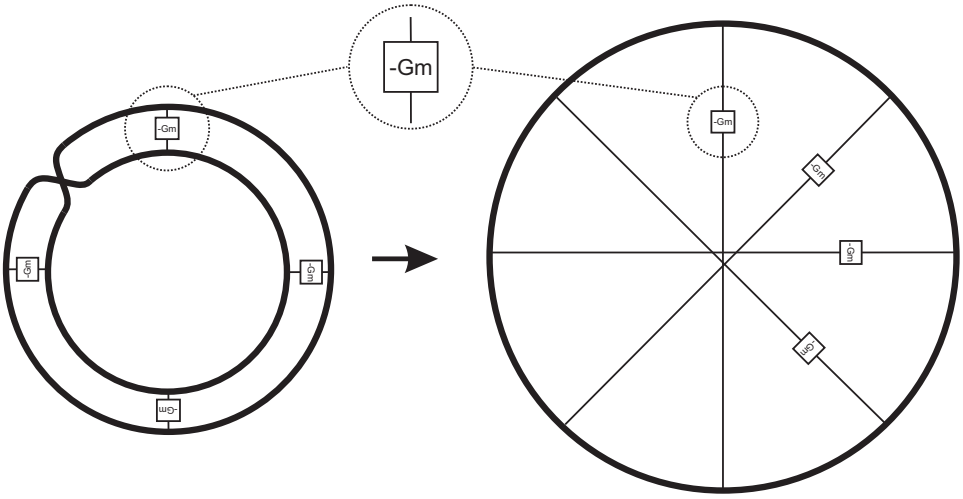


Figure 3.11: Untwisted Möbius loop with -Gm

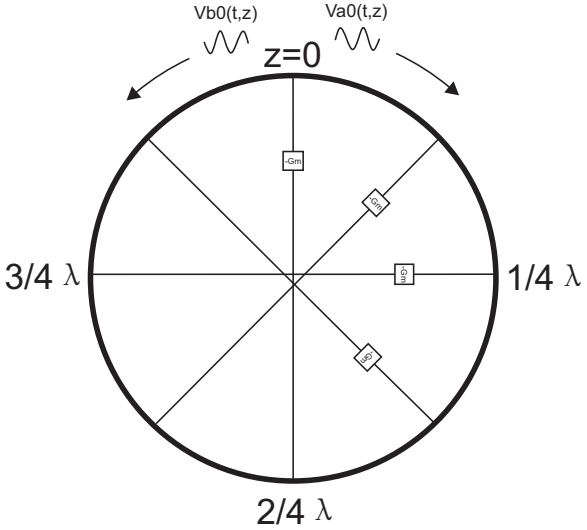


Figure 3.12: N=4 untwisted RTWO

As the circuit is totally symmetrical, superposition of N SWOs is given by

$$\begin{aligned} V_0(t,z) &= \sum_{n=0}^{N-1}[2B_0\cos\omega_0(t-\frac{nT_0}{2N})\cos\beta(z-\frac{n\lambda}{2N})] \\ &= \sum_{n=0}^{N-1} B_0\cos(\omega_0 t-\beta z). \end{aligned} \tag{3.1}$$

Looking at Eq. (3.1), the clockwise travelling wave is the only one. The RTWO can be viewed as a superposition of multiple SWOs, as shown by Eq. (3.1). Thermally induced phase noise can be classified into three types: 1) resonator noise, 2) tail current noise, and 3) differential pair noise. The following research is based this, but it can be applied to a distributed resonator with minor changes.

Any resonator can lose energy and produce thermal noise. If we concentrate on the noise near the oscillation frequency, the noise current produced by the resonator can be represented by a single resistor with the impedance R_p at the resonant frequency. The noise current flows into a lossless resonator modeled with an LC ladder circuit, which is similar to a $\lambda/4$ shorted transmission line, in the steady state, since the $-G_m$ cell compensates for the resonator's loss. The PM component will be formed inversely with offset frequency, resulting in phase noise, while the AM component will be reduced by the $-G_m$ cell's limiting action.

A lossless shorted transmission line's input impedance is given by

$$\begin{aligned} Z(\omega_0+\omega_m) &= +jZ_0\tan(\beta l_q) \\ &= +jZ_0\tan(\frac{2\pi}{\lambda_m}\frac{\lambda}{4}) \\ &= +jZ_0\tan(\frac{2\pi(\omega_0+\omega_m)}{2\pi v_p}\frac{2\pi v_p}{4\omega_0}) \\ &= -jZ_0\cot(\frac{\pi}{2}\frac{\omega_m}{\omega_0}) \\ &\approx -j\sqrt{\frac{L}{C}}\frac{2\omega_0}{\pi\omega_m}, \end{aligned} \tag{3.2}$$

where $Z_0=\sqrt{L/C}$ is the characteristic impedance of TL, l_q is the quarter of wave-length. The magnitude of the input impedance is

$$|Z(\omega_0+\omega_m)| = \frac{4\omega_0^2 L}{\pi^2\omega_m}. \tag{3.3}$$

The parallel resistance R_p and $Z(\omega_0 + \omega_m)$ compose the resonator. The Q-factor can be expressed as

$$Q = \frac{\omega_0}{2\omega_{3dB}} = \frac{\pi^2 R_p}{8L\omega_0}. \tag{3.4}$$

It's worth noting that the distributed resonator's consistency factor differs from the LC resonator's $Q = R_p/(\omega_0 L)$. Another distinction is that the distributed resonator's input impedance is high not just at its fundamental frequency but also at its harmonics, as seen in Eq. (3.2). As a result, a square-wave current pumped into the resonator produces a voltage that is close to square-wave. Assuming that the $-G_m$ cell has a complementary differential pair, the differential voltage amplitude at the fundamental frequency is $V_0 = 4IR_p/\pi$, where I is the VCO's tail current. This area is known as the current confined region since the amplitude is equal to the tail current. The amplitude rises in lockstep with the tail current until it exceeds the supply voltage V_{DD}, which is referred to as the voltage confined field. In practice, the maximum voltage is limited by the voltage headroom available for the current source. Assuming that half of the noise contributes to PM (another half noise is as AM) and that the present noise's power spectral density is $\overline{i_n^2} = 4kT/R_p$, where k is the Boltzmann's constant and T is the ambient absolute temperature, phase noise($\mathcal{L}_{tank}$) at offset frequency ω_m is calculated using Eq. (3.3) and (3.4)

$$\begin{aligned} \mathcal{L}_{tank}(\omega_m) &= |Z(\omega_0 + \omega_m)|^2 \frac{\overline{i_n^2}}{2} / (\frac{V_0^2}{2}) \\ &= (\frac{4\omega_0^2 L}{\pi^2 \omega_m})^2 \frac{4kT}{R_p} \frac{1}{2} / (\frac{V_0^2}{2}) \\ &= \frac{4kTR_p}{V_0^2} (\frac{\omega_0}{2\omega_m Q})^2. \end{aligned} \tag{3.5}$$

The differential pair allows noise from the tail current to enter the resonator. By switching the polarity at twice the oscillation frequency, the differential pair functions as a mixer and commutates the noise. Since the noise is uncorrelated with time, the commutation results in a white output range. The current noise spectral density of a field-effect transistor

(FET) is given by

$$\overline{i_n^2} = 4kT\gamma_{bias}g_{m,bias}, \tag{3.6}$$

where γ_{bias} is the FET's channel noise coefficient and $g_{m,bias}$ is the current source's transconductance. The phase noise induced by the tail current noise can be calculated by replacing the thermal noise in Eq. (3.5) and (3.6) and using $g_{m,bias} = 2I/V_{eff}$, where V_{eff} is the effective gate voltage,

$$\begin{aligned} \mathcal{L}_{tail}(\omega_m) &= \frac{4kTR_p}{V_0^2}(\frac{\omega_0}{2\omega_m Q})^2\gamma_{bias}g_{m,bias}R_p \\ &= \frac{4kTR_p}{V_0^2}(\frac{\omega_0}{2\omega_m Q})^2\frac{\gamma_{bias}\pi V_0}{2V_{eff}}. \end{aligned} \tag{3.7}$$

At a differential zero crossover, which is twice the oscillation frequency, the noise from the differential pair is sampled by the finite width window. Although the sampled noise is cyclostationary, it has a white spectrum. We now use the fast-switching approximation, in which the differential pair flips the output current between I and $-I$ in a short period of time, $T_s = \Delta v/S$, where S is the slope of the differential waveform at zero crossing and Δv is the voltage needed to completely turn the differential pair. A series of square pulses with a height of $-2I/\Delta v$ and width of $T_s = \Delta v/S$ will approximate the transconductance G_m in time. Since the spectral density of the differential pair's current noise is given by $\overline{i_n^2} = 4kT\gamma Gm$, the sampled noise current from both nMOS and pMOS is given as

$$4kT\gamma G_m\frac{2T_s}{T_0} = 4kT\gamma(\frac{2I}{\Delta v})\frac{2\Delta v}{S}\frac{\omega_0}{2\pi} = 4kT\gamma\frac{2I\omega_0}{\pi S}. \tag{3.8}$$

The channel noise coefficients of nMOS and pMOS are γ_N and γ_P, respectively, and $\gamma = (\gamma_N + \gamma_P)/2$. Although the noise around the zero crossing is pure phase noise, the phase noise due to the differential pair is derived from Eq. (3.5) and Eq. (3.8) as

$$\mathcal{L}_{diff}(\omega_m) = \frac{4kTR_p}{V_0^2}(\frac{\omega_0}{2\omega_m Q})^2\gamma\frac{4IR_p\omega_0}{\pi S}. \tag{3.9}$$

Similar to [35], Linear-Time-Invariant (LTI) system and cyclostationary property are adopted to analyze RTWO noise. To simplify analysis and provide more intuitive understanding of noise behavior, a inverter latch is treated as two differential pairs. The noises are categorized into two sources: i) Thermally induced resonator noise due to the loss of transmission line; and ii) Thermally induced differential pair noise.

Noise in the RTWO is analysed through the noise in standing-wave oscillator(SWO). The SWO is first viewed as a $\lambda/4$ TL. Modeling LC ladder as $\lambda/4$ transmission line, the input impedance $Z(f_0+\Delta f)$ of $\lambda/4$ can be expressed as $-jZ_0\frac{2}{\pi}\frac{f_0}{\Delta f}$, where $Z_0=\sqrt{L/C}$. The loss of the resonator is denoted by R_p. Assuming half noise from R_p contributes to the phase noise, for example, $\overline{i_n^2}=\frac{1}{2}4kT/R_p$. The expression of PN due to thermal noise of resonator at the offset frequency Δf in the SWO is the same as the cross-coupled LC oscillator:

$$\begin{aligned}\mathcal{L}(\Delta f)_{tank} &= \frac{|Z(f_0+\Delta f)|^2\overline{i_n^2}}{\frac{V_0^2}{2}} \\ &= 4kT\frac{R_p}{V_0^2}\Big(\frac{f_0}{2Q\Delta f}\Big)^2,\end{aligned} \tag{3.10}$$

where $Q=\pi^2R_p/8L\omega_0$, and $V_0=4/\pi I_D R_p$ attributed to the differential property. I_D is the drain currents with $V_{GS}=V_{DD}$, and $V_{DS}=V_{DD}/2$.

The noise current injected from differential pairs become strongest at which the drain voltage of two NMOS transistors are the same. However it becomes weaker when this equilibrium cannot be held. This results in two strongest noise injection period, i.e. around zero-crossing point, in every cycle of the clock. In the presence of this periodical noise injection, the thermally induced noise from differential pair is cyclostationary. [35] proved this type of noise spectrum is still white. Its spectral density is scaled by a ratio of total injection time and the time period.

The total injection time is $4\Delta t$ in one cycle, T_0, if each side of the noise conduction time at the zero-crossing point is denoted by Δt, which is given by $\Delta t=\frac{\sqrt{2}V_{od}}{V_0}\frac{1}{2\pi}T_0$, where V_{od} is the overdrive voltage when the differential pair is in equilibrium. Since the spectral density of the current noise of the differential pair is given by $\overline{i_n^2}=4kT\gamma g_m$, where $g_m=\frac{I_D}{V_{od}}$,

γ is the noise coefficient. Assuming $g_{m,N} = g_{m,P} = 1/2g_m$, the total noise current is

$$\begin{aligned} \overline{i^2_{n,diff}} &= \frac{8kT\gamma(2g_m)}{4}\frac{4\Delta t}{T_0} \\ &= 4kT\gamma\frac{\sqrt{2}}{2R_p}. \end{aligned} \tag{3.11}$$

In analogous to (3.10), phase noise due to the differential pair is derived as

$$\begin{aligned} \mathcal{L}(\Delta f)_{diff} &= \frac{|Z(f_0+\Delta f)|^2\frac{1}{2}\overline{i^2_{n,diff}}}{\frac{V_0^2}{2}} \\ &= 4kT\gamma\frac{\sqrt{2}}{2}\frac{R_p}{V_0^2}\big(\frac{f_0}{2Q\Delta f}\big)^2. \end{aligned} \tag{3.12}$$

Underestimating Δt due to approximating transition smoothly will not affect the phase noise estimation as injected noise strength is over estimated. Eqs. (3.10) and (3.12) yield the total phase noise, given by

$$\mathcal{L}(\Delta f)_{total} = \frac{4kTR_p}{V_0^2}\big(1+\frac{\sqrt{2}}{2}\gamma\big)\big(\frac{f_0}{2Q\Delta f}\big)^2. \tag{3.13}$$

Eq. (3.13) is the total phase noise in a $\lambda/4$ SWO. The RTWO is modeled as a superposition of multiple $\lambda/2$ SWOs [35]. It is necessary to modify the quality factor in $\lambda/4$ SWO by replacing L with $L/4$, resulting in $Q' = \pi^2 R_p/2L\omega_0$. The amplitude of RTWO is also reduced by a factor of 2, giving rise to total noise as

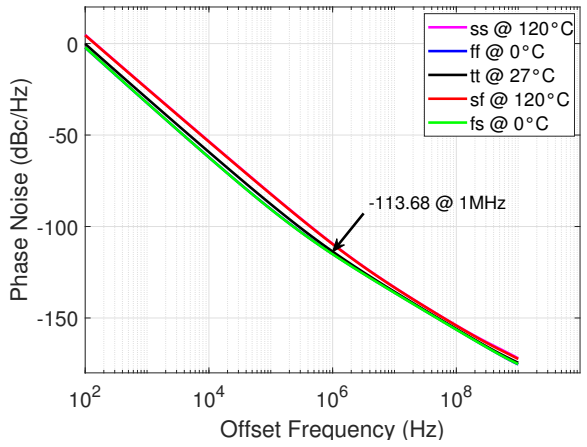
$$\mathcal{L}'(\Delta f)_{total} = \frac{2kTR_p}{V_0'^2}\big(1+\frac{\sqrt{2}}{2}\gamma\big)\big(\frac{f_0}{2Q'\Delta f}\big)^2, \tag{3.14}$$

where $V_0' = 2/\pi I_D R_p$. Eq. (3.14) suggests that i) The larger outputs, the less PN from the circuit. ii) The quality factor of the TL segments also play a critical role in the PN. In addition, (3.14) yields that the sharper transition of the transistor pair is beneficial to reduce the PN due to the thermal noise.

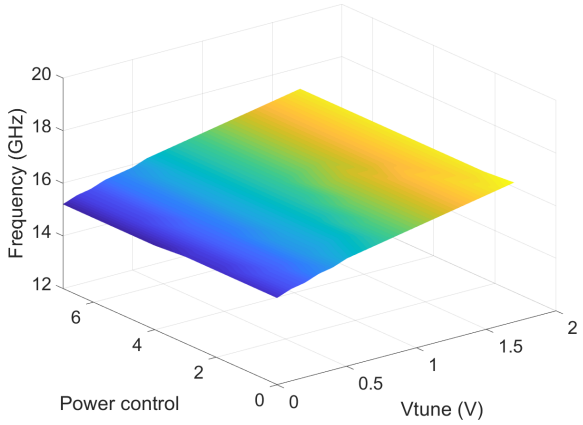
3.3 Simulation Result

3.3.1 Phase Noise and Power Control

The proposed RTWO was implemented in a standard 0.13 μm CMOS process with a supply voltage of 1.2 V. EM tools were used to extract the S-parameter file describing the transmission line segments. The tuning range is simulated to be between 15.1 and 16.9 GHz. Maximum power consumption at 1 MHz offset is 5.8 mW with a FoM of 190.3 dBc/Hz; minimum power consumption is 3 mW with a FoM of 185.5 dBc/Hz. Due to the slight signal swing at the minimum power setting, the PN at 1 MHz offset increases by 7 dB. The simulated PNs from a 16 GHz carrier with a 5.8 mW setting are shown in Fig. 3.13(a). The



(a) Simulated PN at 16GHz in five corners

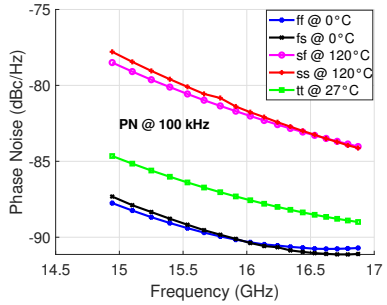


(b) Frequency versus V_{tune} versus power control setting

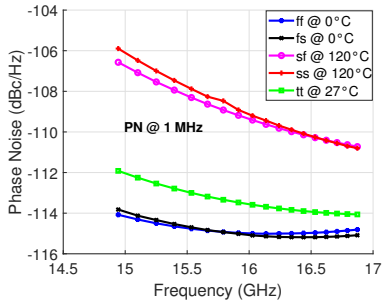
Figure 3.13: Simulation result

temperatures for the process corners "ss", "ff", "tt", "fs", and "sf" were set to 120°C, 0°C, 27°C, 0°C, and 120°C, respectively. 120°C, 0°C, 27°C are commonly used temperature corners in the industry. 'ss' corner is the worst process corner with 120°C which is the worst temperature. 'ff' corner is the best process corner with 0°C which is the best temperature of noise performance. The phase noise versus tuned frequency in process corners is summarized in Fig. 3.13(a). The phase noise difference between two directions of propagation is negligible. Fig. 3.14(a) to (c) illustrate the simulated PN operating at 100 kHz, 1 MHz, and 10 MHz

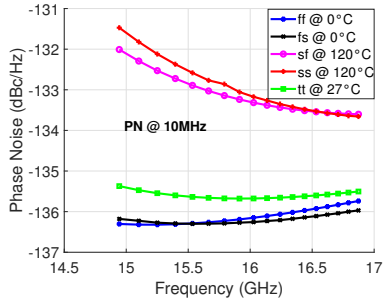
with a 5.8 mW power consumption. The FoM at 1 MHz versus tuned frequency is shown in Fig. 3.14(d).



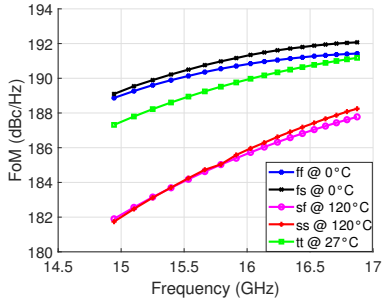
(a) PN at 100kHz versus tuning frequency



(b) PN at 1MHz versus tuning frequency



(c) PN at 10MHz versus tuning frequency

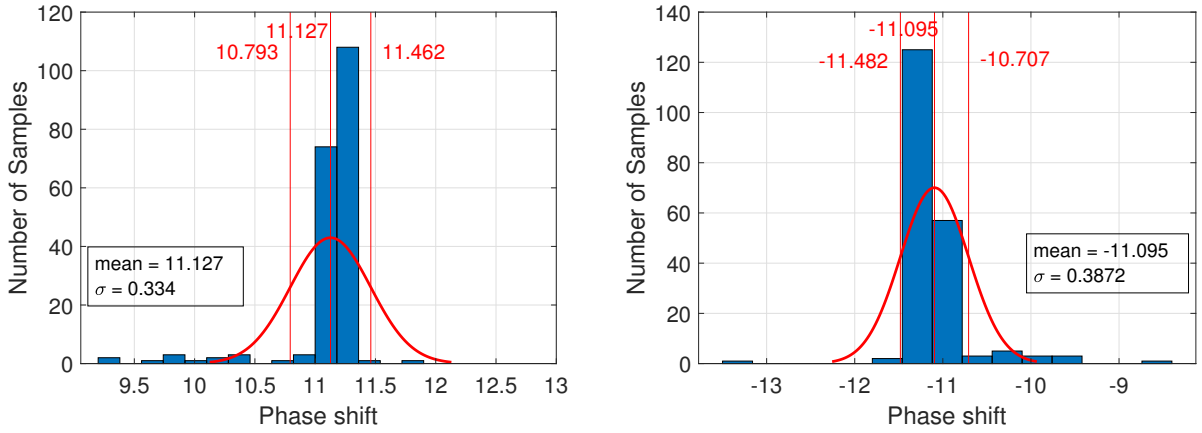


(d) FoM at 1MHz offset versus tuning frequency

Figure 3.14: Frequency and phase noise simulation result

3.3.2 Monte-Carlo Simulation

To verify the direction control, the phase difference between two signals, e.g. 157.5° and 168.75° (Fig. 3.2), was calculated. The ideal phase difference for clockwise and counterclockwise wave propagation is 11.15° and -11.15°, respectively. In Fig. 3.15(a) and (b), a Monte Carlo simulation of 200 cases for each directions(400 cases in total) demonstrates the robust direction control. The majority falls into a single σ. Take note that the delay deviates from ideal due to transmission line mismatch and undesirable parasitics, lowering the signal-to-noise ratio if RTWO is used in phase array transceivers. Phase mismatches can be alleviated using an effective phase tuning technique as illustrated in [17].



(a) (b)

Figure 3.15: Two hundred points Monte Carlo simulations for both directions control. (a)Clockwise control, and (b)Counterclockwise control

3.4 Summary

Table 3.1: Comparison with State-of-the-art RTWO design

References	**This work**	[36]	[32]	[4]	[25]
Technology(nm)	130	22	28	130	28
Supply Voltage(V)	1.2	0.8	1.3	1.2	-
Power(mW)	5.8	21	75	28.4	16.2
Frequency(GHz)	16.2	30	19.8	2	37.7
Tuning(%)	11.2	13.5	20.6	16	12
PN@1MHz(dBc/Hz)	-113.7	-107	-101.2	-141	-
PN@10MHz(dBc/Hz)	-135.7	-128.1	-131.2	-	-121.2
FoM@1MHz(dBc/Hz)	190.3	183.5	168.4	190	-
FoM@10MHz(dBc/Hz)	192.3	184.6	178.4	-	180.6

In conclusion, the proposed RTWO design basically satisfied the design objectives. It achieved an 11.2% tuning range at the 16-GHz operating frequency. A 5.8mW power consumption is remarkable. An FoM of 190.3dBc/Hz is excellent compare to other designs. Also, the direction control circuit was verified by the Monte-Carlo simulation, and the result shows the strong reliability of it. However, this design is not verified by fabricated IC measurement due to terminated supporting of this CMOS IC process. As a result, our

research group decides to achieve a measurement result by using an available IC process. In the next chapter, a transplanted design with available RF CMOS process will be presented.

Chapter 4

TWO 14-GHz RTWO DESIGNS

4.1 Design Objectives

In order to further lower the phase noise and for fabrication purpose, two RTWOs are designed in a TSMC 130-nm CMOS process. Both RTWOs targets Ku-band frequency(13-GHz). To save the power, the TL segments are reduced to eight from sixteen of the last design. The differential amplifiers are revised to the current-mode amplifiers, in which the tail current source is inserted to provide better linearity and constant bias current. One RTWO use tail-current filtering technique to suppress the even harmonics of the oscillator to improve the PN performance. To make a fair comparison, the second RTWO is designed to use voltage-mode amplifier. A 15% frequency tuning is achieved through coarse and fine tuning by introducing capacitor banks and varactors at each nodes. In addition, the direction control logic is revised to accommodate the current-mode amplifier.

4.2 The Proposed Designs

4.2.1 Circuit Topology

The proposed RTWO displayed in Fig. 4.1 consists of a Möbius loop, a current distributor with direction control, current mode latches and tuning banks. The TL ring is divided into 8 segments.

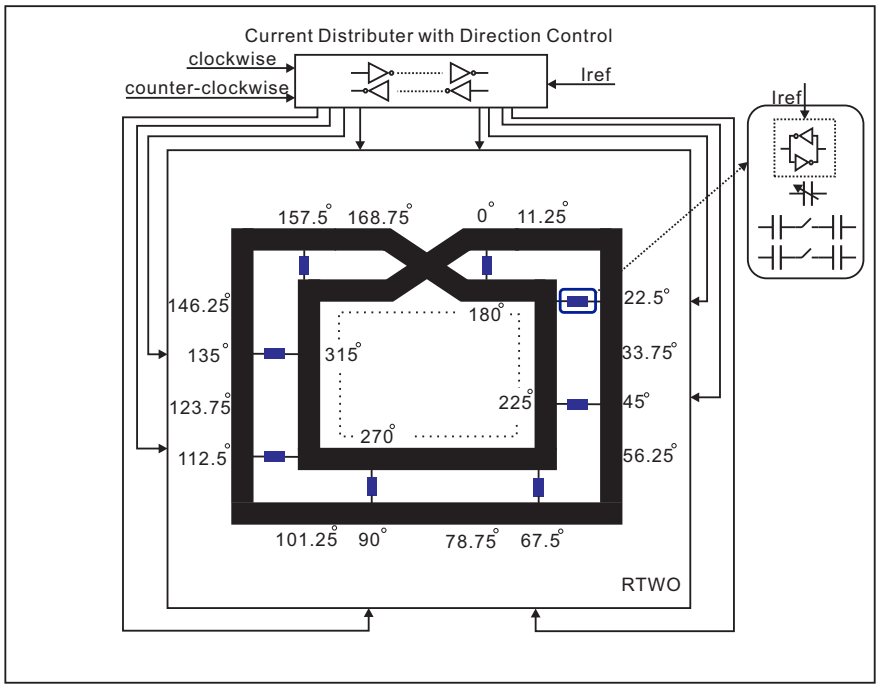


Figure 4.1: Circuit Topology of Both RTWO designs

4.2.2 Möbius Loop Design

Unlike the design in Ch. 3, this Möbius loop uses top thick metal for most of parts. Because the process only provides one thick metal layer, this design does not use the second top layer to make the corners. The only part that used Metal 7 is the cross-connection segment. This helps the transmission line to have the highest possible Q-factor. As a result, the two transmission lines are slightly unbalanced due to length mismatch at the corners, leading to phase discrepancy. The direction control circuit is still used in both designs. In both designs, the direction controller outputs 8 signals into each of the latches correspondingly. A current signal is provided in RTWO(a), and a voltage signal is provided in RTWO(b). A current reference signal is injected into the direction controller component in RTWO(a). The control strategy is the same as the design introduced in Ch. 3. Each segment is 200μm long, and the space between two-wire is 10μm, as shown in Fig. 4.3(a). The Q-factor is $Q = 15$ for the TL segment, Fig. 4.3(b) and (c). The optimization process which was used in this design is same with Ch. 3.2.3. The perimeter of TL loop is $200\mu m/seg \times 8segs = 1600\mu m$.

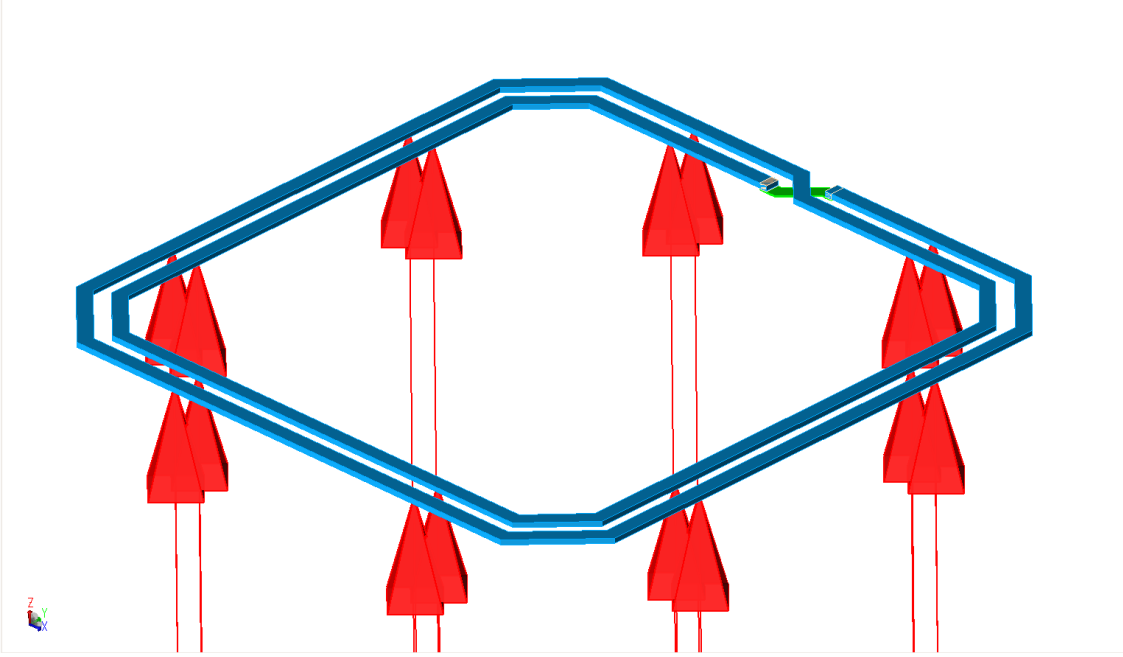
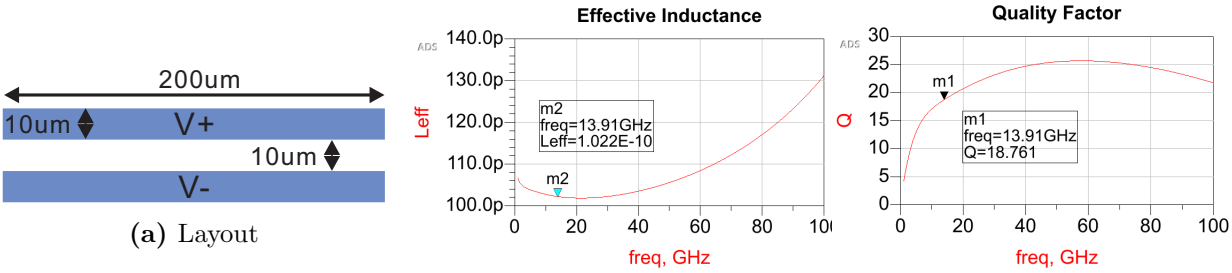


Figure 4.2: 3-D view of the Möbius loop



(a) Layout

(b) L_{eff}

(c) Q

Figure 4.3: Transmission segment

4.2.3 TL Segment Designs

Fig. 4.4 and 4.5 are the TL segment design of RTWO(a) and RTWO(b). Every segment in both designs consists of a latch and a tuning bank. The segment of RTWO(a) in Fig. 4.4 uses a tail current biased latch with tail current filter, and the segment of RTWO(b) in Fig. 4.5 uses a switched voltage drive latch. Signal I_b is used to control the biasing current go through the latch in RTWO(a), and signal V_s is used to control the ON/OFF of the latch in RTWO(b). The current of RTWO(a) can be tuned by changing I_b from a range of 1.5mA

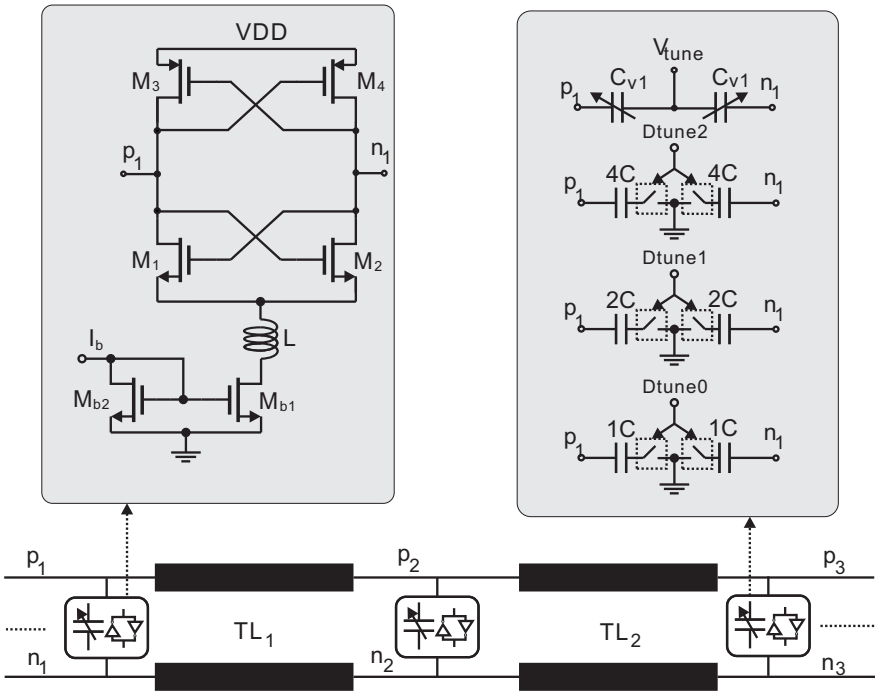


Figure 4.4: RTWO(a) with current drive latches. $M_{1,2} = 12fingers \cdot 1.2\mu m/130nm$, $M_{3,4} = 12fingers \cdot 2.4\mu m/130nm$, $L = 900pH$, $M_{b1,b2} = 32fingers \cdot 16\mu m/260nm$, $V_{tune} = 0$ to 1.2 V, $Cv1 = 13$fF to 41fF, C = 26fF, $I_b = 1.5$mA to 3.5mA

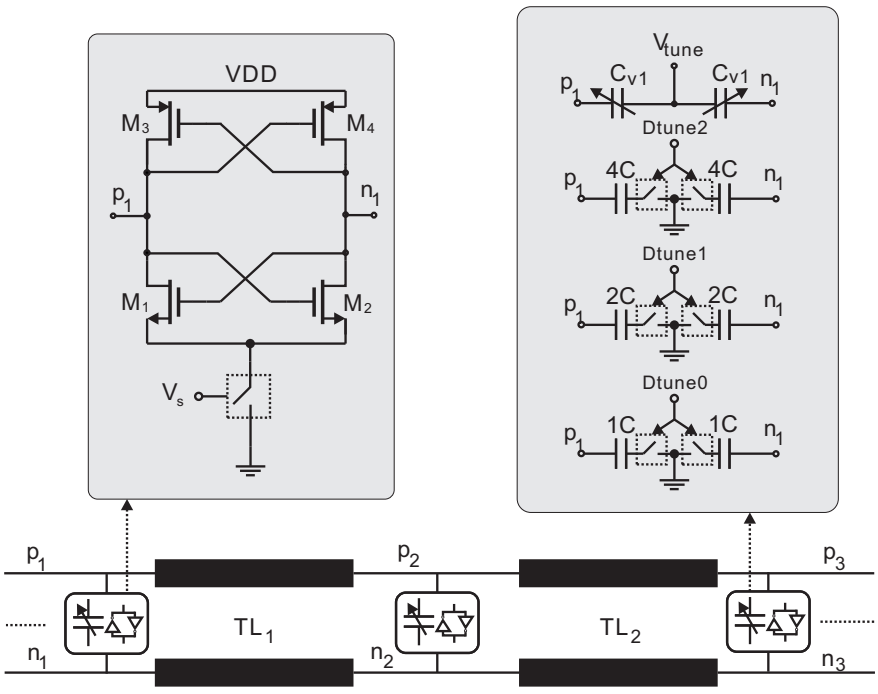


Figure 4.5: RTWO(b) with voltage drive latches. $M_{1,2} = 12fingers \cdot 1.2\mu m/130nm$, $M_{3,4} = 12fingers \cdot 2.4\mu m/130nm$, $M_{switch} = 16fingers \cdot 8\mu m/130nm$, $V_{tune} = 0$ to 1.2 V, $Cv1 = 13$fF to 41fF, C = 26fF, $V_s = 0$ or 1.2 V

to 3.5mA. Both designs have eight 3-bits discrete tuning banks with small size fine tuning varactors.

4.2.4 Tuning Bank

A wide tuning range of the oscillator is expected to accommodate different requirements, e.g., process variations that result in a broad spread in the center frequency from wafer to wafer must be compensated. The easiest way to accomplish this is with a robust varactor, that is, one that produces a broad capacitance swing relative to the fixed resonator capacitance as the tuning voltage is swept through its full range, which is limited by the power supply. The wider operation region of the varactor, regardless of whether it is realized using a MOS capacitor or a p-n junction, the more tuning capability is provided. However, the increased sensitivity of frequency tuning comes at the cost of increased phase noise. Varactor capacitance is a function of the control voltage. Clearly, additive noise on the control voltage can convert to phase noise sidebands via frequency modulation. However, the varactor, whose incremental capacitance is proportional to the instantaneous voltage around it, provides an average capacitance to the resonator that is affected by oscillating waveform's envelope and duty cycle. Even if the control voltage is noiseless, the varactor will detect envelope fluctuations caused by amplitude-modulated noise on the oscillation and transform them to phase noise by modulating the average capacitance. This process will result in an increase of several decibels in the phase-noise sidebands. It is possible to reduce FM sensitivity while maintaining a broad tuning range by combining discrete and continuous tuning. By applying discrete tuning bank, the frequency tuning will be less sensitive to the variation of power supply voltage.

For example, a 3-bits binary-weighted switched capacitor array shown in Fig. 4.4 and 4.5 can tune the oscillator center frequency to eight discrete frequencies. Then, using a small-size MOS varactor to interpolate continuously across these frequencies, we obtain a family of overlapping tuning curves that ensures consistent frequency coverage throughout the tuning range, as illustrated in Fig. 4.6. To make sure the frequency covers the tuning continuously, the size of tuning bank and the varactor must be chosen properly.

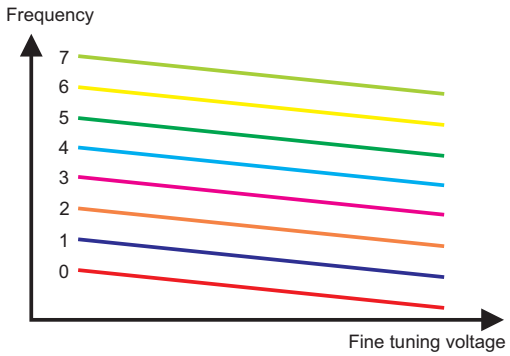


Figure 4.6: The curve of a 3-bits discrete tuning band with fine tuning

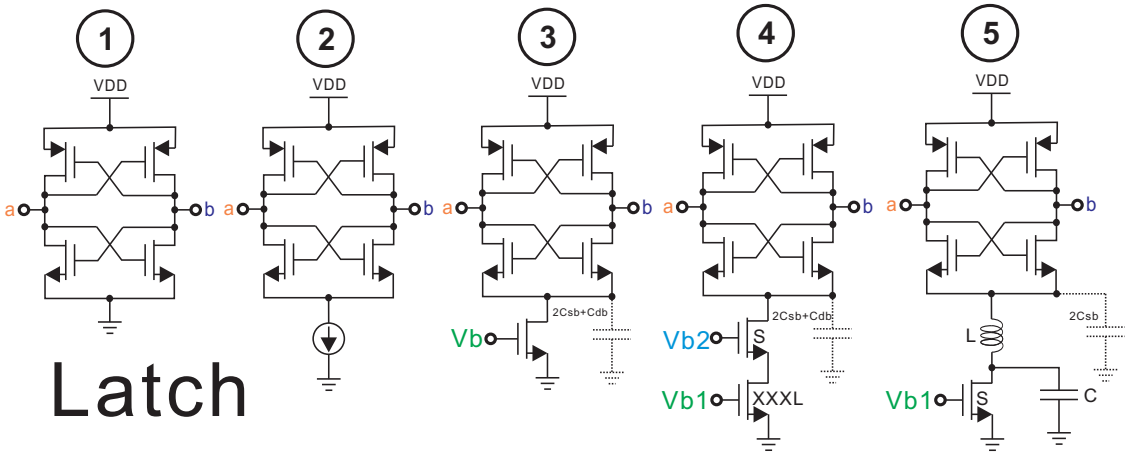


Figure 4.7: Different latch designs

Several amplifiers are plotted in Fig. 4.7: (1) is the original design. This structure has a critical issue—the latches directly connected to the power supply. A voltage drive-based latch is sensitive to the power supply voltage. $-Gm$ of the latches is easily changed by the variation of VDD. Also, the strong current variation might affect the power and ground of other latches. (2) is the current-mode latch with ideal current source. (3) is the simplest physical implementation of (2). Unfortunately, (3) degrades PN performance due to a number of reasons, e.g, flicker noise coupled from the bias network, the parasitic capacitance of the transistor, etc. The explanation of (3) will later talk in the next section. (4) introduces a cascades tail current transistor. A small size transistor on top generates a large flicker noise and an extra larger transistor with a big parasitic capacitance in the bottom. The larger channel width transistor partially rejects the flicker noise from the top

transistor, and the small channel width transistor partially isolates the influence of the larger parasitic capacitance from the larger transistor. This solution is not a great solution because the cascaded structure consumes a larger headroom voltage, which affects the voltage on the cross-connected inverters. (5) contributes less to the overall PN, which was used in this design.

4.2.5 Tail Filtering Technique

Hegazi(2001)[26] presents a technique that can limit phase noise and power consumption to differential oscillators. The technique is based on a new understanding of the physical processes underlying phase noise in differential oscillators. Leeson's proportionality is often used to describe phase noise in LC feedback oscillators,

$$\mathcal{L}(\omega_m) \propto \frac{1}{V_0^2} \cdot \frac{kT}{C} \cdot \frac{\omega_0}{Q} \cdot \frac{1}{\omega_m^2}. \tag{4.1}$$

In this equation, kT/C noise is expressed as the normalized to the power of LC tank amplitude. The constant of proportionality, which is phase noise, accounts for noise contributions from all the circuit components. The device excess noise number F must be defined as it pertains to device sizes, as well as to other circuit parameters. The bandpass resonator detects the fundamental frequency of the current waveform and excludes harmonics with an oscillation amplitude of differential voltage

$$V_0 = \frac{4IR}{\pi}, \tag{4.2}$$

where I is the bias current and R is the modeled resistance of the tank.

Rael(2000)[37] has found out the physical mechanisms of phase noise in the LC oscillator. And, from the theory proposed by Leeson, the oscillator's noise specified in Eq. (4.1), the oscillator's device excess noise number F is

$$F = 1 + \frac{4\gamma IR}{\pi V_0} + \gamma \frac{4}{9} g_{m,bias} R, \tag{4.3}$$

where I is the bias current, γ is the FET's channel noise coefficient (equal to 2/3 for long channels and greater for shorter channels), and $g_{m,bias}$ is the current-source FET's transconductance. Eq. (4.3) denotes three noise sources: the tank resistance, differential-pair FETs, and the current source. It is worth noting that thermal noise in differential-pair FETs results in oscillator phase noise that is independent of FET scale. In standard oscillators operating at high current levels and with moderate-to-high resonator quality factors, the contribution of the current source to phase noise outweighs that of other sources of phase noise. Assume that the third term, the input from existing sources, is eliminated from (4.3). Given that (4.2) indicates that the oscillation amplitude is proportional to the current, the device excess noise number simplifies to its smallest value

$$F_{min} = 1 + \gamma. \tag{4.4}$$

Consider the circuit in steady state. A cross-coupled differential pair biased at the equilibrium point by an ideal noiseless current has a negative resistance $-g_m$ and a noise voltage spectral density of $4kT\gamma/g_m$ due to the FET pair. However, there is no differential output noise if the differential pair is alternatively conducting current from one branch to the other. As a result, the oscillation samples the FET noise at each differential zero crossing point, or the twice frequency of the oscillation. Meanwhile, the fundamental part of the differential-pair current in relation to the oscillation voltage has a steady-state conductance that is exactly equal to the resonator loss conductance. Although the noise is cyclostationary, it has a white spectrum. The study demonstrated that the noise spectral density is identical to that of a linear resistor, with a magnitude equal to the effective steady-state negative resistance, but with a device excess noise number of γ:

$$\hat{i_n^2} = 4kT\gamma\frac{2I}{\pi V_0} = \frac{4kT\gamma}{R}. \tag{4.5}$$

Reference [37] demonstrated how current-source noise contributes to oscillator phase noise. Due to the switching activities, the differential pair eventually bring the low-frequency noise into two correlated AM sidebands around the fundamental. Low-frequency noise in

the current source does not generate phase noise directly. Noise frequencies close to the oscillation frequency are interpreted just beyond the tuned circuit's passband. However, since noise frequencies around the second harmonic downconvert to near the oscillation frequency and upconvert to around the third harmonic, they are rejected by the LC tank's bandpass characteristic. Around the oscillation frequency, a tone injected into the tuned circuit passband can be decomposed into half AM and half PM sidebands. Half of the noise in a current source that is near the second harmonic creates phase noise. While odd harmonics of the commutating waveform may downconvert higher noise frequencies close to the oscillation, these are ignored in a first-order calculation because their mean square contributions are small $(1/3^2, 1/5^2, 1/7^2, ...)$. The function of noise in the vicinity of even harmonics of the oscillation was first recognized by comparing the switching pair of an oscillator to that of a commutating mixer, and then by analyzing time-domain waveforms. The current source serves two functions in the differential LC oscillator: it establishes the bias current and also adds a high impedance in series with the differential pair's switching FETs. Odd harmonics flow in a differential path through the resonator capacitance and the switching FETs to ground in any balanced circuit, while even harmonics flow in a common-mode path through the resonator capacitance and the switching FETs to ground. Thus, strictly speaking, the current source need only provide high impedance to the even harmonics of the oscillation frequency, with the second harmonic usually being the dominant. By reducing the need for high impedance to a small band of frequencies, this definition can be realized in several specific ways.

To summarize, first, phase noise converted by current source only relates to the around second harmonic of oscillation frequency, and second, a high impedance at the tail current is needed only at the second harmonic to prevent the differential-pair FETs in the triode from loading the resonator. This indicates the use of a narrowband circuit to block the current source noise, making it appear noiseless to the oscillator, thereby providing a high impedance in the critical narrow band of frequencies. As shown in Fig. 4.8(a), connecting a large capacitor in parallel with the current source shorts noise frequencies about the second harmonic to ground is a solution. Then, as shown in Fig. 4.8(b), an inductor is placed between the current source and the tail to increase the impedance. The inductance is chosen

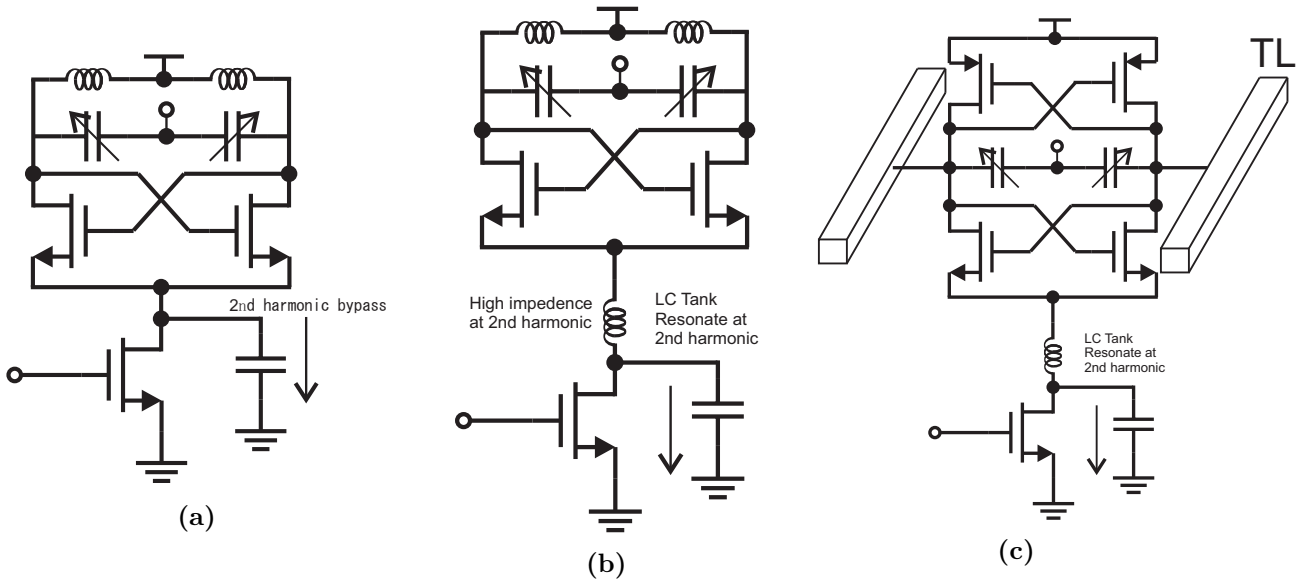


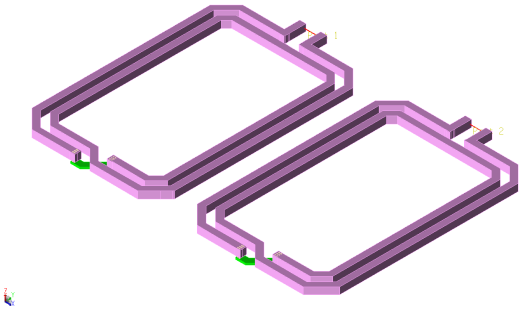
Figure 4.8: Tail-based VCO with noise filter

to resonate at the second harmonic in parallel with any capacitance present at the differential pair's common sources. The impedance at the tail is only constrained by the inductor's quality factor. What we refer to as a noise filter is comprised of the inserted inductor and the big capacitor. This technique can be applied on RTWO, as Fig. 4.8(c) shown. Because this RTWO is designed at a fundamental frequency around 14-GHz, the second harmonic is about 28-GHz. As a result, the resonant frequency of this LC resonator should be located at 28-GHz. The C is fully provided by the parasitic capacitance of the tail transistor, as the width of the tail transistor is $W_n = 8\mu m/finger \times 16 fingers = 128\mu m$.

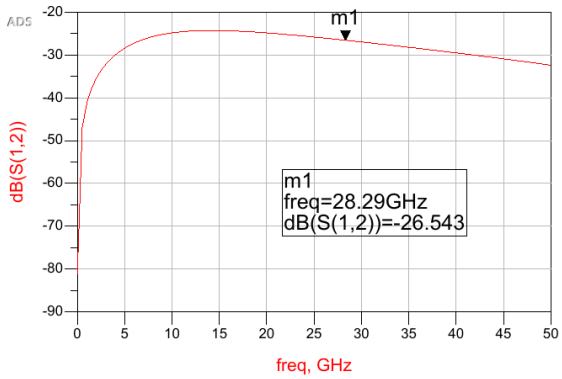
4.2.6 8-shaped Inductor

According to Zou(2019)[38], an effective way to reduce the coupling between inductors is to adopt an 8-shaped inductor. To verify the coupling reduction, three groups of inductor pairs will be compared. All three groups are set to 1-nH O-shaped/8-shaped inductor. Also, all three groups are set to the same centre-to-centre distance($d_{centre} = 80\mu m$).

Three comparison groups are shown in Fig. 4.9, 4.10 and 4.11. Every inductor in the three pictures has a port, and the two terminals are treated as a port of the network.

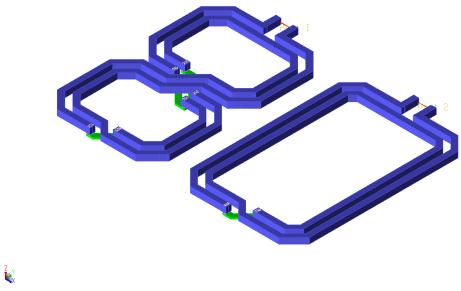


(a) 3D view

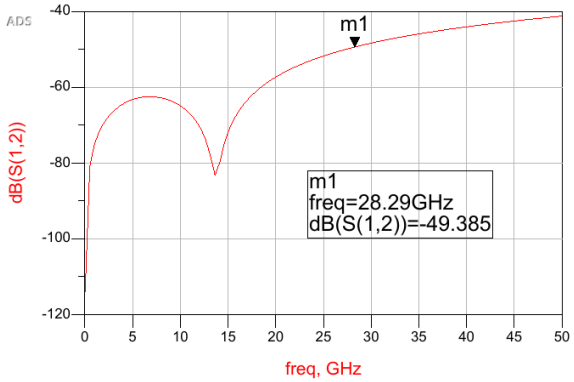


(b) S_{12} in dB

Figure 4.9: O-shaped/O-shaped($d_{centre} = 80\mu m$)

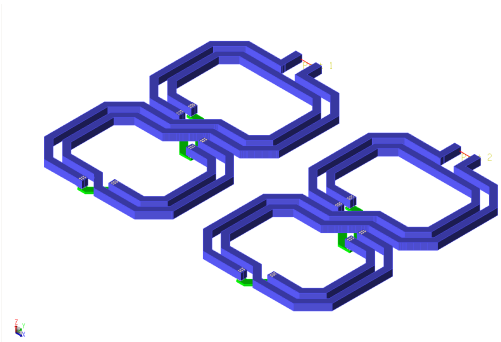


(a) 3D view

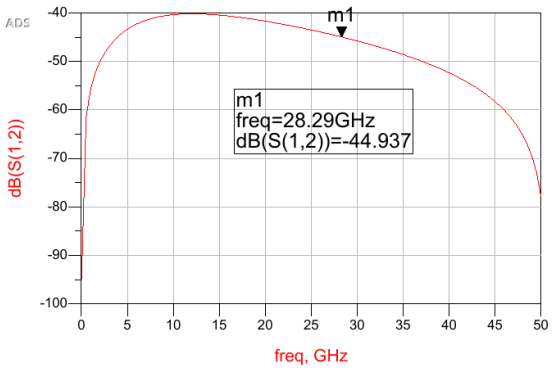


(b) S_{12} in dB

Figure 4.10: 8-shaped/O-shaped($d_{centre} = 80\mu m$)



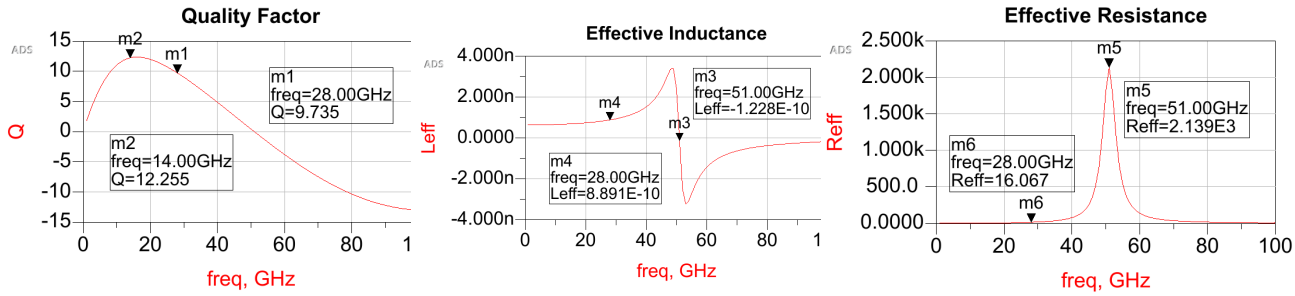
(a) 3D view



(b) S_{12} in dB

Figure 4.11: 8-shaped/8-shaped($d_{centre} = 80\mu m$)

The electric-magnetic field exists when energy feeds into the ports. Electric-magnetic field coupling will bring cross-talk issue between two inductors. This design targets to use the area inside the TL ring, which means tail inductors are close to each other. The first group in 4.9 shows that at the coupling coefficient $S_{12} = -26.54dB$ at 28-GHz. The second and third groups are used as compared with the first group. The coupling coefficient of 8-shaped/O-shaped and 8-shaped/8-shaped are $S_{12} = -49.39dB$ and $S_{12} = -44.94dB$.



(a) Q-factor **(b)** L_{eff} **(c)** R_{eff}

Figure 4.12: Properties of proposed 8-shaped inductor

As we can see, the coupling coefficient dropped down about $20dB$ when one of the inductors is an 8-shaped inductor. This phenomenon caused by the magnetic field cancelling of 8-shaped inductor. This is one of the important features of 8-shaped inductor because it significantly reduces interference. As Fig. 4.12(a), (b) and (c) show, the self-resonant frequency of the proposed 8-shaped inductor is at 51-GHz. Effective inductance and Q-factor are $L_{eff} = 889pH$ and $Q = 9.7$ at 28-GHz.

4.3 Layout

The size of the bond pad provided by the process is $82.8\mu m$ x $63\mu m$. By considering of the testing, the distance(center-to-center) of probes is set to $112\mu m$. This touching pad consists of a top thick metal layer and a connection on the METAL6 layer. The RTWO circuit is connected to METAL6 of the touching pads. A picture of the bond pads placing is shown as Fig. 4.13

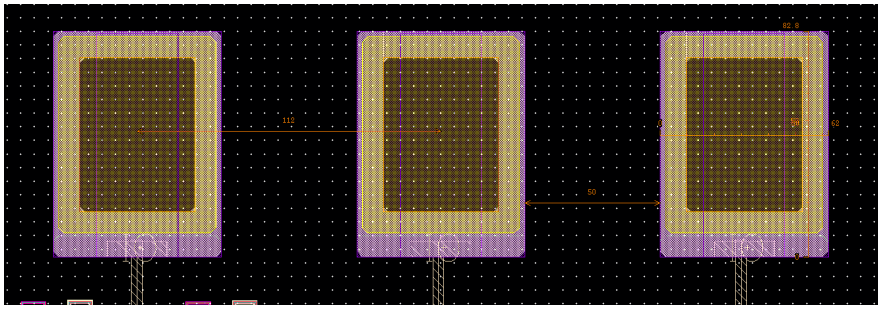


Figure 4.13: Three Bondpads

The TL ring takes an area of 420μm x 420μm. An area 390μm x 390μm inside the ring is used to place the tail current filter inductors. Eight tapping points located at 8 locations of the TL ring. Every two nodes have a distance of 200μm in between.

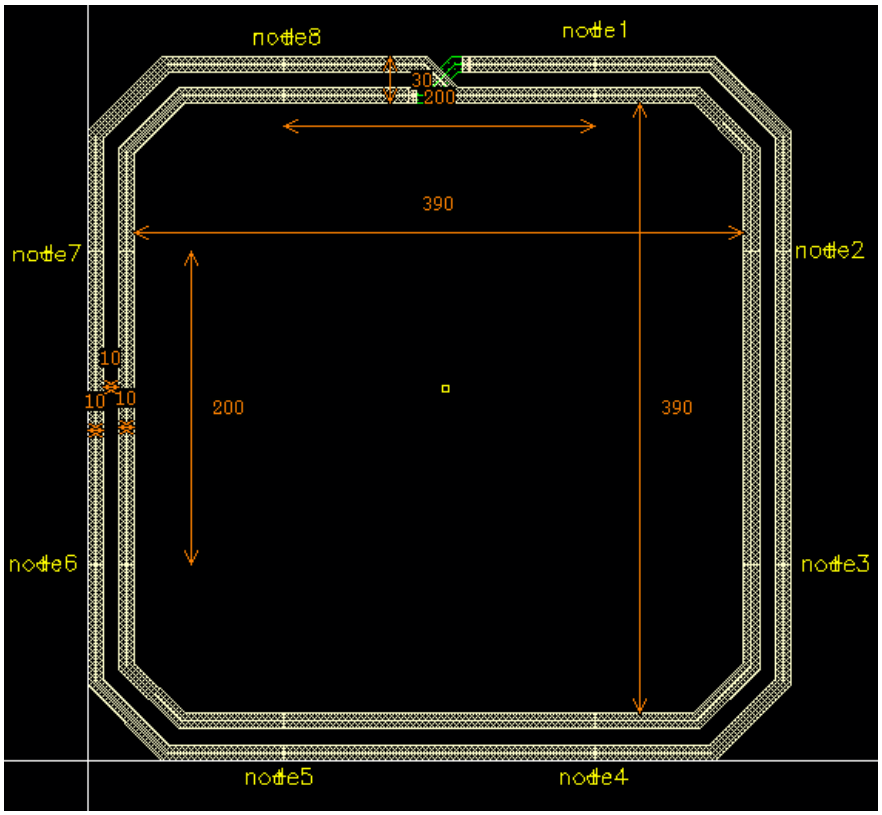


Figure 4.14: Full Möbius loop layout

The layout of the 8-shaped inductor is illustrated in Fig. 4.15(a). This inductor has 2 turns with an area of 110μm x 68μm. The white coloured area is the METAL8(3μm thick metal). The cross-sections(green lines) uses METAL7(0.3μm thin metal). The layout of the current-mode latch in RTWO is presented in Fig. 4.15(b). It can be seen that the design has a tail filter biasing with the latch but the same structure does not exist in the voltage-mode latch based RTWO, which is shown in Fig. 4.15(c). The voltage-mode latch only has an NMOS on the left side as the switch for the direction control. Both designs put the latches inside of the RTWO ring.

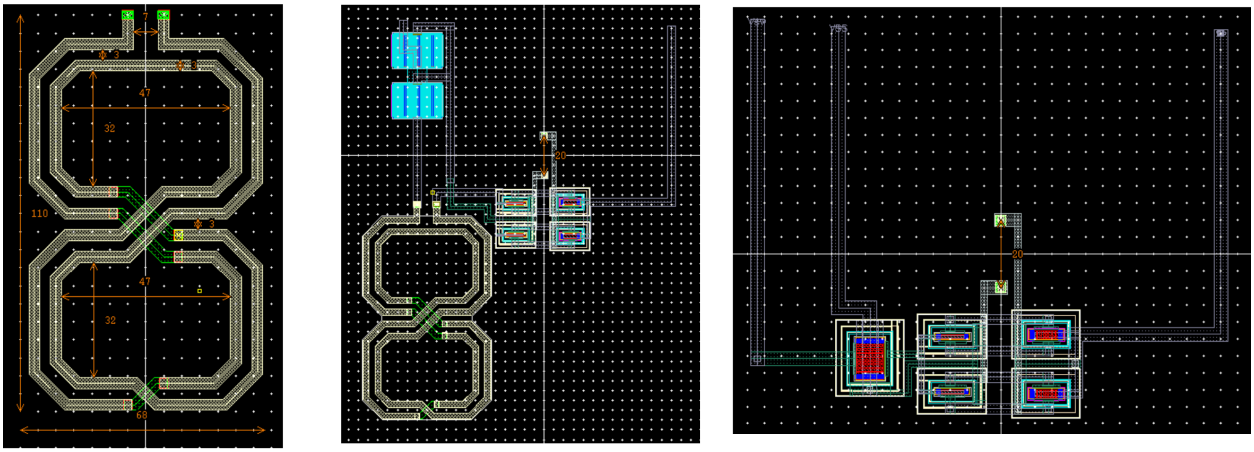


Figure 4.15: (a) Layout of the inudctor, (b) Layout of amplifier latch and tail current source with filter RTWO design, and (c) Layout of voltage-mode latch in RTWO design.

4.3.1 Full Chip Layout

The full chip layout with seal ring, shown as Fig. 4.16, takes a $2.5mm \times 1mm = 2.5mm^2$ silicon area. RTWO(a) is located on the left side, and RTWO(b) is located on the right side with their bond pads. A protective area of about 100μm wide ensures they are isolated from each other. Both designs are verified by Design Rules Checking(DRC) and Layout versus Schematic(LVS). The term "design rules" refers to a collection of parameters given by semiconductor manufacturers that allow the designer to validate the accuracy of

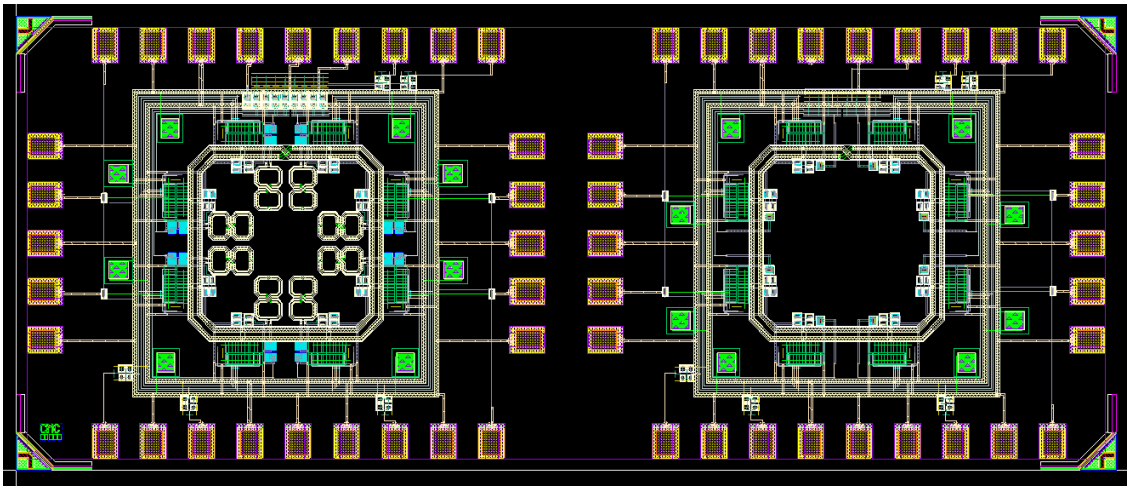


Figure 4.16: Full chip layout with sealring

a mask set. The design rules are process-dependent for each semiconductor manufacturing process. A design rule set defines some geometric and connectivity constraints in order to allow for variability in semiconductor manufacturing processes and ensure that the majority of parts function correctly. Layout versus Schematic (LVS) software is a form of electronic design automation (EDA) verification software that determines whether an integrated circuit layout matches the design's original schematic or circuit diagram. A good design rule review (DRC) verifies that the layout adheres to the rules intended/required for error-free fabrication. It does not, however, guarantee that it accurately reflects the circuit you wish to fabricate. This is the situation in which an LVS search is used. The software program reads a database file that contains all the layers that were created to display the circuit during layout. The database is then subjected to a series of area-based logic operations in order to evaluate the semiconductor components depicted in the drawing by their construction layers. Area-based logical operations accept polygon areas as inputs and produce polygon areas as outputs. These operations describe the device identification layers, the devices' terminals, the wiring conductors and via structures, as well as the pin positions (also known as hierarchical connection points). Numerous measurements can be made on the layers that comprise devices, and these measurements can be added to these devices. Typically, the layers that reflect "right" wiring (conductors) are made of and referred to as metals. Vias are sometimes used to refer to vertical relations between these layers. The extracted layout

netlist is then compared to the circuit schematic's netlist. If the circuit's two netlists match, it passes the LVS search. It is said to be "LVS clean" at this stage. The full layout with pads definitions and fillers can be found in Appendix.

4.4 Simulation Result

RTWO(a) achieved a $(15.67GHz - 11.89GHz)/13.78GHz \approx 27\%$ tuning range, and RTWO(b) achieved a $(15.55GHz - 11.87GHz)/13.71GHz \approx 26.8\%$. The different colors in Fig. 4.17 and 4.18 represent settings of the 3-bits discrete tuning bank from $Dtune = 0, 1, 2, 3, 4, 5, 6, 7$. Three temperature and corner settings are $TT@40°C$, $SS@120°C$ and $FF@-30°C$. The power consumption of RTWO(a) under TT corner is between 13mW

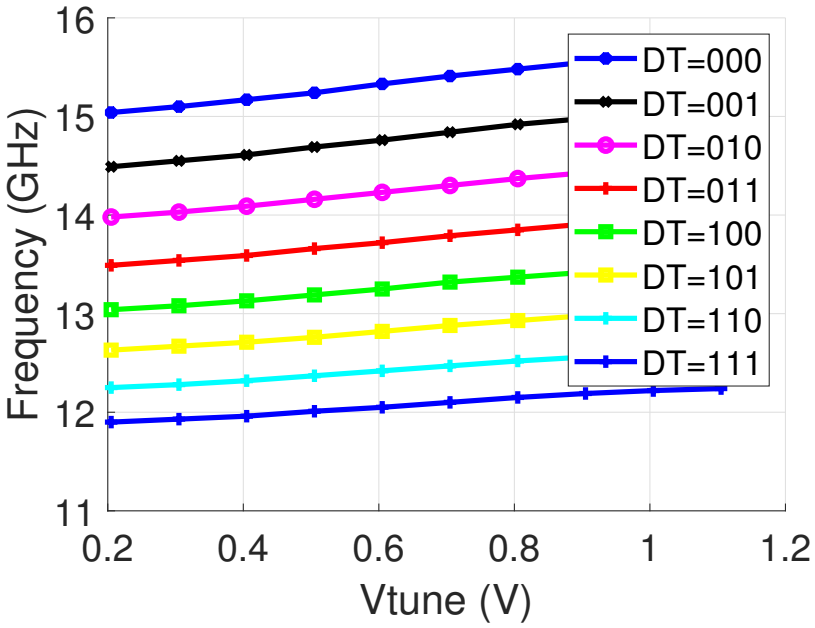


Figure 4.17: RTWO(a) frequency tuning(11.89-GHz to 15.67-GHz) under $TT@40°$

and 18.4mW(as shown in Fig. 4.19), and the power consumption of RTWO(b) under TT corner is between 14.6mW and 20.5mW(as shown in Fig. 4.20). They have similar power

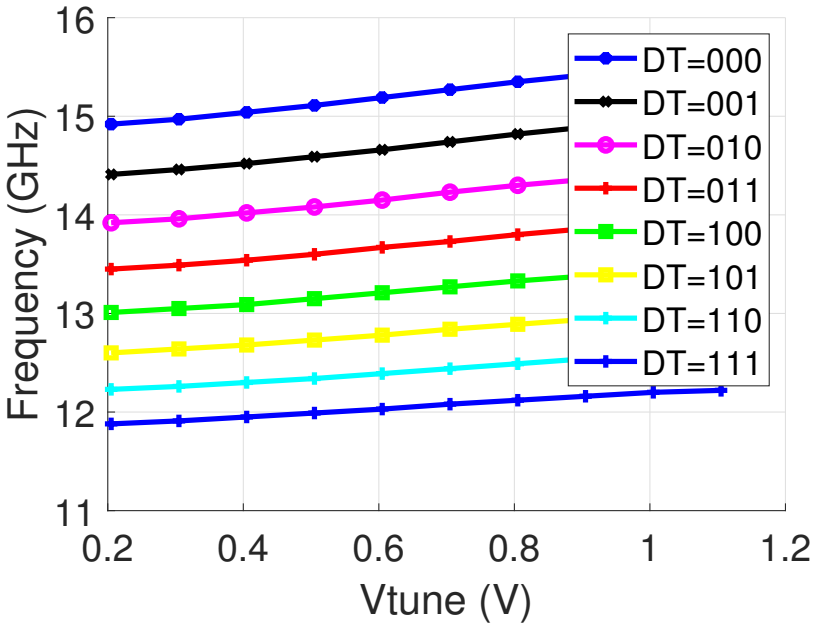


Figure 4.18: RTWO(b) frequency tuning(11.87-GHz to 15.55-GHz) under TT@40°

consumption range, and this will benefit the comparison work. Typical power consumption of RTWO(a) and (b) are 15.7mW and 17.55mW prospectively.

RTWO(a) phase noise across 3 corners at centre frequency(13.75-GHz) are shown in Fig. 4.21. RTWO(b) phase noise across 3 corners are shown in Fig. 4.22.

The FoM of RTWO(a) is 184.8dBc/Hz at 13.75-GHz, and the FoM of RTWO(b) is 180.8dB/Hz at 13.75-GHz. It is obvious that, on average, the FoM of RTWO(a) is 4dB better than RTWO(b). Fig. 4.23 and 4.24 show both results. The noncontinuous of the line is caused by the inaccuracy of harmonic balance, but the average FoM can be used as a reference.

4.5 Summary

Two RTWOs with the same operation frequency range were implemented in a TSMC 130-nm CMOS process for comparison purpose. The current source filtering technique was applied to the first RTWO whereas the second RTWO used a voltage-mode amplifier. The

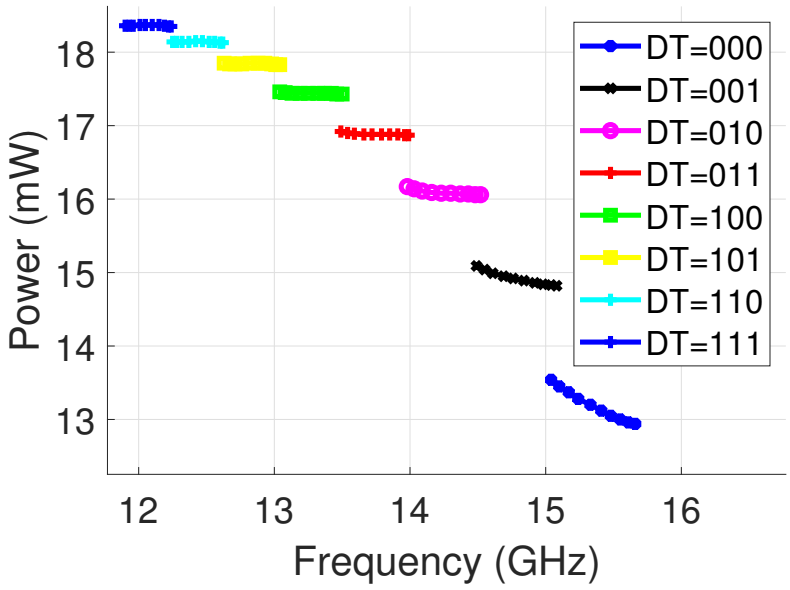


Figure 4.19: RTWO(a) power consumption within tuning range(13mW to 18.4mW) under TT@40°

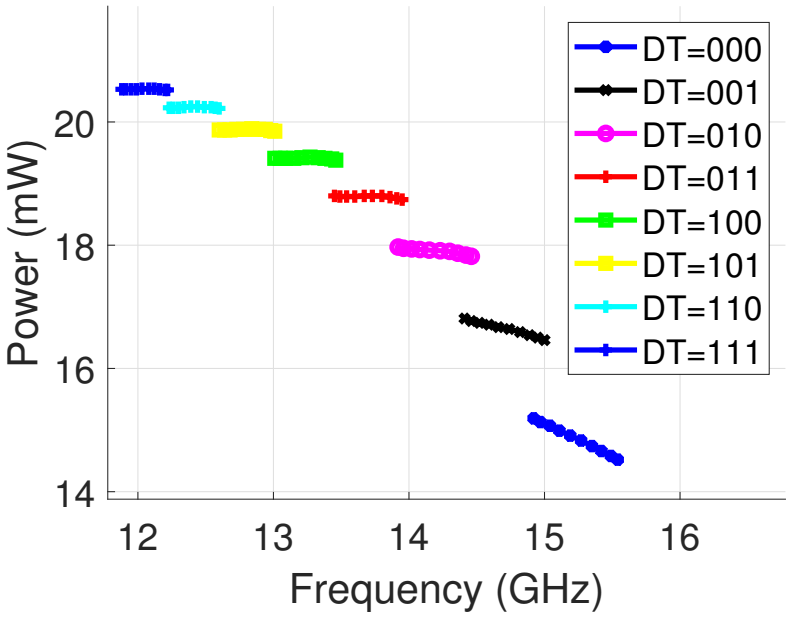


Figure 4.20: RTWO(b) power consumption within tuning range(14.6mW to 20.5mW) under TT@40°

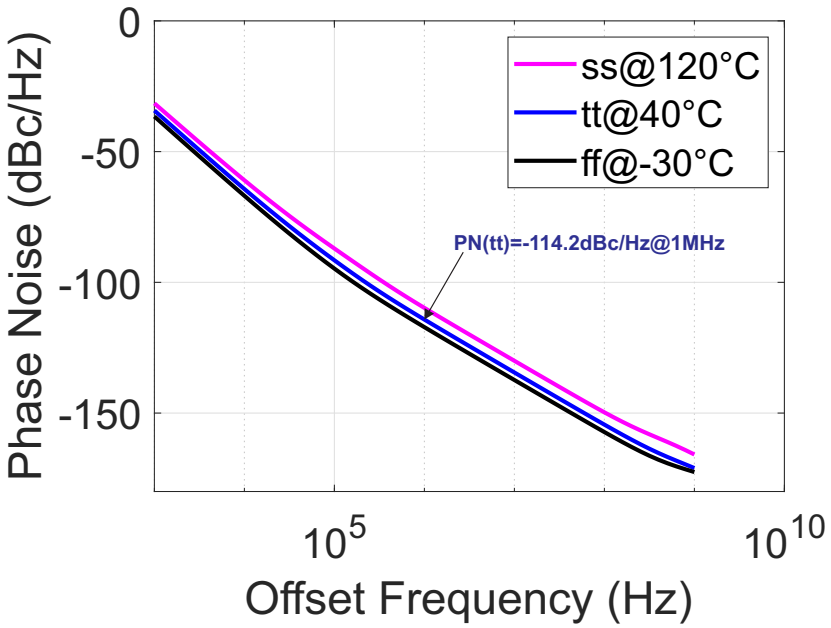


Figure 4.21: RTWO(a) PN across three corners at 13.75-GHz with 16-mW power

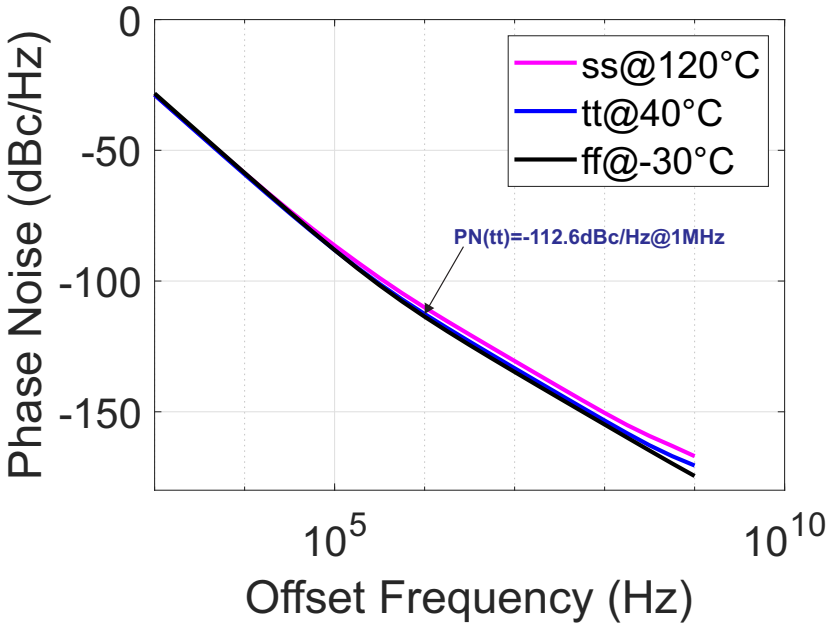


Figure 4.22: RTWO(b) PN across three corners at 13.75-GHz with 18-mW power

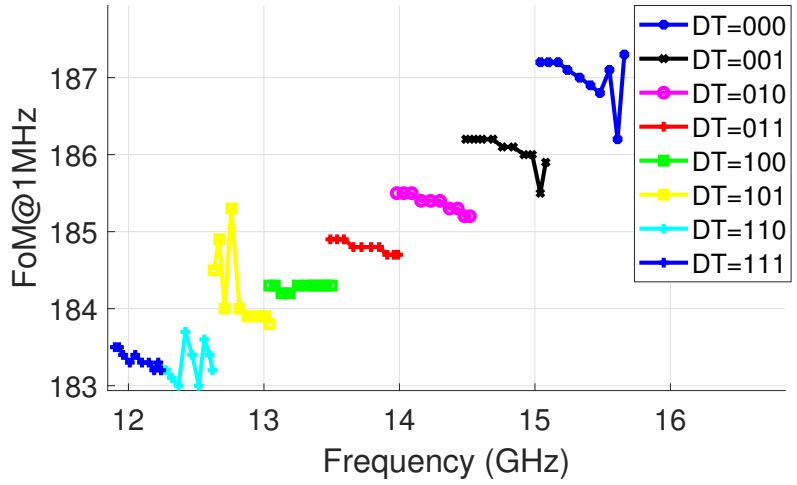


Figure 4.23: RTWO(a) FoM with PN@1MHz offset vs Frequency(TT@40°)

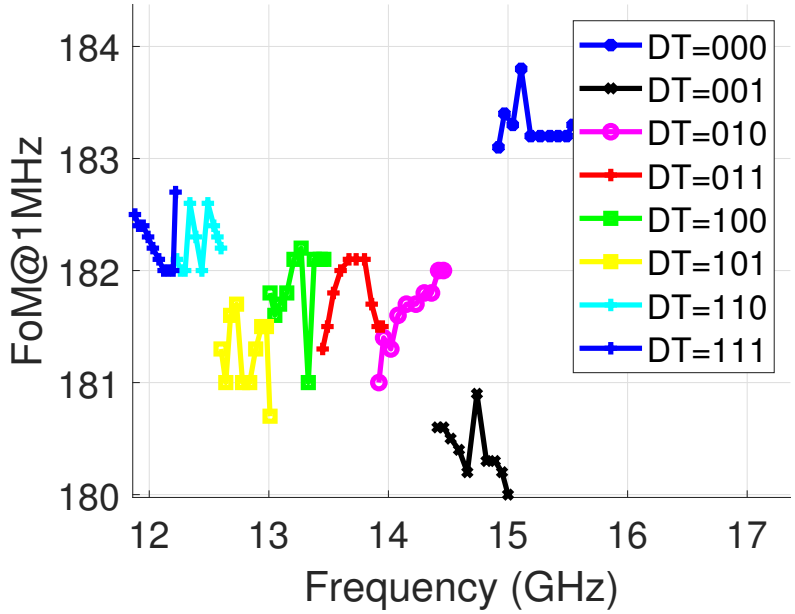


Figure 4.24: RTWO(b) FoM with PN@1MHz offset vs Frequency(TT@40°)

FoM shows that the one with filtering technique offers 4 dB better than that of voltage-mode amplifier based RTWO. Both designs have a centre frequency of 13.75-GHz with a 27% tuning range with similar power consumption, 15-18 mW in maximum. The designs have been submitted for fabrication.

Chapter 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

In conclusion, this thesis presents the design of three Ku band low-noise rotary travelling-wave voltage-controlled oscillators for RF microelectronics applications in 130-nm standard CMOS technology. The RTWO consists of a differential TL loop, eight groups of amplifiers and tuning banks, a direction control circuit targeting the 16-GHz and 14-GHz frequency bands. The ability of the RTWO to guide the signal to the wanted direction at a low cost is implemented through digital logic. By applying 200 samples of Monte-Carlo simulations, the reliability of the direction control technique is verified. A comparison is made with state-of-the-art RTWO designs, resulting in a remarkable performance RTWO, with a FoM = 190.3 dBc/Hz at 1MHz offset for the first RTWO design. The schematic simulation shows that: i) The reliability of the direction control. ii) The tunable power consumption. iii) The low phase-noise performance with 11.2% tuning. The simulated PN at 1 MHz offset is -113.7 dBc/Hz. The second design demonstrates that the tail current filtering technique provides a better phase noise performance as compared to the third design, which only has voltage-mode amplifier employed. The 8-shaped inductor, which has low magnetic field coupling, is introduced into the design. An examination of the 8-shaped inductor in magnetic field coupling is also performed, demonstrating that since the inductor has an asymmetric magnetic field pattern, the injected magnetic coupling noise around the inductor area not noticeably affects the inductor. In addition, the discovery of optimization rules is found.

It applies to magnetic-field related passive devices, such as transmission lines, inductors, transformers/baluns. An overall 4 dB FoM improvement is expected from the current source filtering under the same power consumption. The simulated PN results at 1 MHz for the two RTWOs are -114 dBc/Hz and -110 dBc/Hz, respectively. The tuning ranges for both RTWOs is the same at 27%. Unlike the first design, which only has schematic simulations based on the GF 130-nm CMOS process, the second and third designs implemented in a TSMC 130-nm 1P8M CMOS technology with 1.2 V supply voltage, are submitted to the foundry for fabrication.

5.2 Future Work

5.2.1 Design Improvements

One part that definitely can be improved is the layout of the design. A start-up circuit should be added to the oscillator design for reliable startup because it ensures the oscillation startup in industrial applications. The full layout with metal fillers can be found in the Appendix, where the floating metal are close to the inductors and the TLs due to the local/global density requirements from the foundry. This might affect the performance of the TLs and the inductors, which are supposed to be placed away from any of the conductors. Lower Q can be expected from this impact. More study and simulation are expected to be done. In the future design, a smaller inductor should be considered to narrow the empty space.

The second part that has not done yet is the post-layout simulation. Though it is challenge to perform post-layout simulation to have magnetic components included, it is necessary to match the schematic and extracted simulations. The possible solution is to extract the circuits excluding TLs and inductors. When it comes to simulations, S-parameter file should be used in the post-layout simulation.

The third part is the on-chip reference current generation. In stead of using external reference current, an on-chip band-gap can be designed with special considerations of the noise contribution.

5.2.2 Exploiting RTWO in Applications

RTWO can be used as the Digital-controlled oscillator(DCO) of a PLL. Similar to [5], the All digital phase-locked loop(ADPLL) originally has multi-phase output because an RTWO performs the role of VCO. This type of ADPLL can be applied in the key component of high-speed circuits, such as Software-defined radio(SDR) ADC/DAC clocking and LO. A fully digital tuning bank should be considered because it provides a wider tuning range. According to [5], the tuning range of RTWO based ADPLL can achieve 53%. As compare to wide tuning LC tank VCOs, this tuning range is excellent.

5.2.3 Testing Fabricated Chip

Chip testing will be involved in the future work. This design uses a multi-contact probe as the DC probe, illustrated in Fig.5.1(a). The supply voltage and the digital bits will

(a) A DC multi-contact probe[39] **(b)** A RF multi-contact probe[40]

Figure 5.1: Probes

be injected to the circuit through this multi-contact probe whereas for the output RF signals, low-loss RF probes will be mounted to the probe station, shown in Fig.5.1(b). RF wafer probes convert electro-magnetic energy traveling through coaxial cables to the on-wafer DUT

and its touch pads. A low-loss cable should be used in the test. In addition, an external constant current source is also needed to provide the bias current. To capture the signal, a bias-T should be connected to the output of RF cables. The conversion process must be carried out with the fewest possible distortions and energy losses.

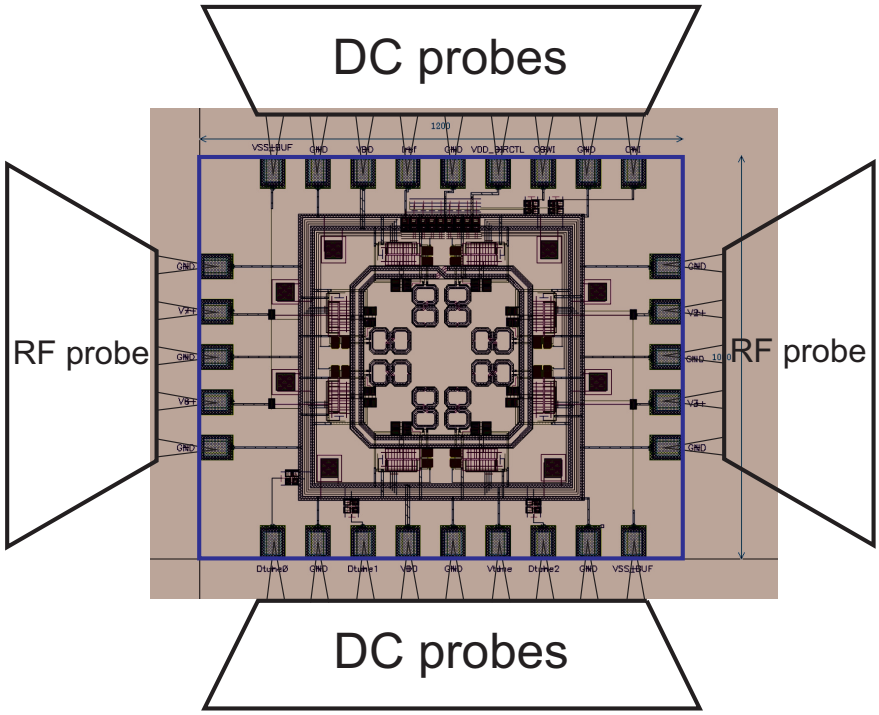


Figure 5.2: DUT and probes

A detailed probing position is shown in Fig. 5.2. The same applied to the second fabricated design. 5.3 shows the configuration of the output signal to the analyzer. The testing plan also includes borrowing equipment and getting laboratory support from CMC.

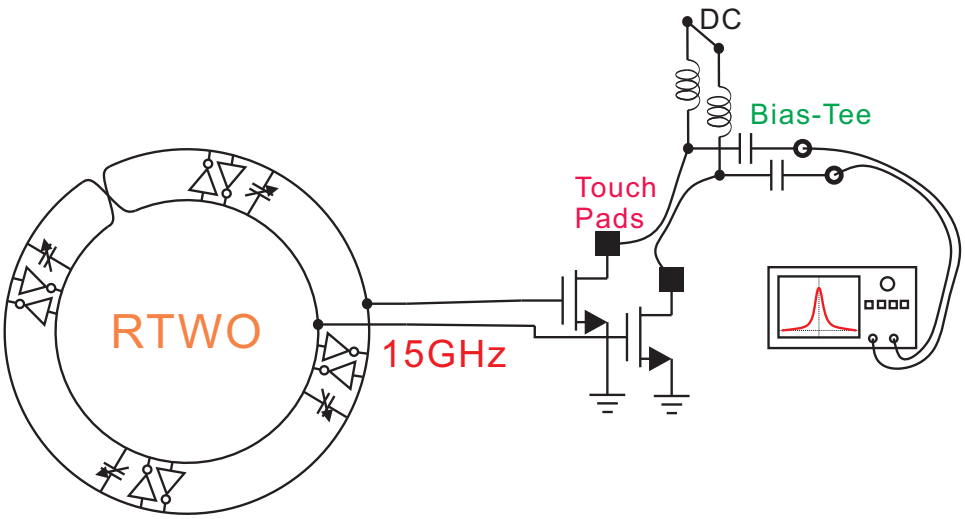


Figure 5.3: Testing scheme

Appendix A

16-GHz RTWO Segment RLGC model

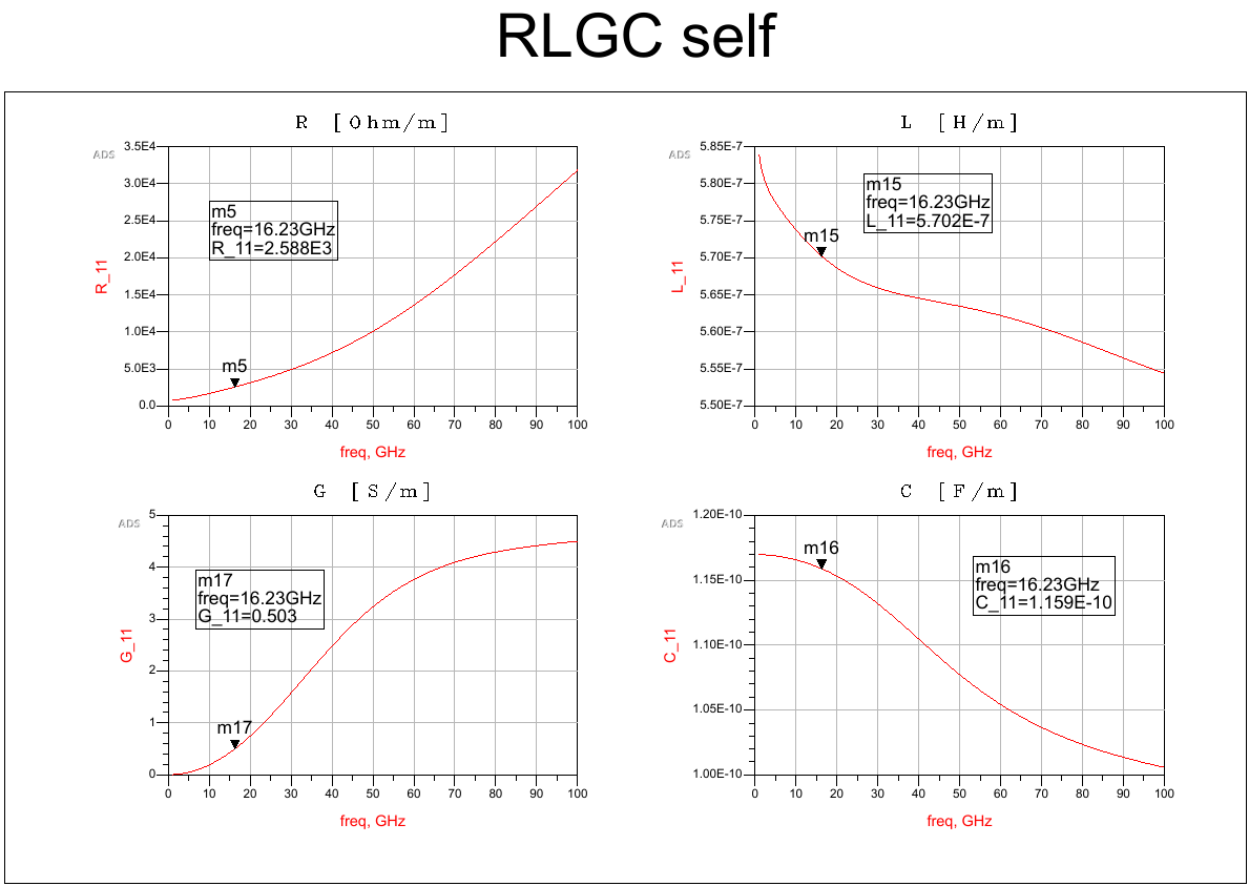


Figure A.1: Self RLGC

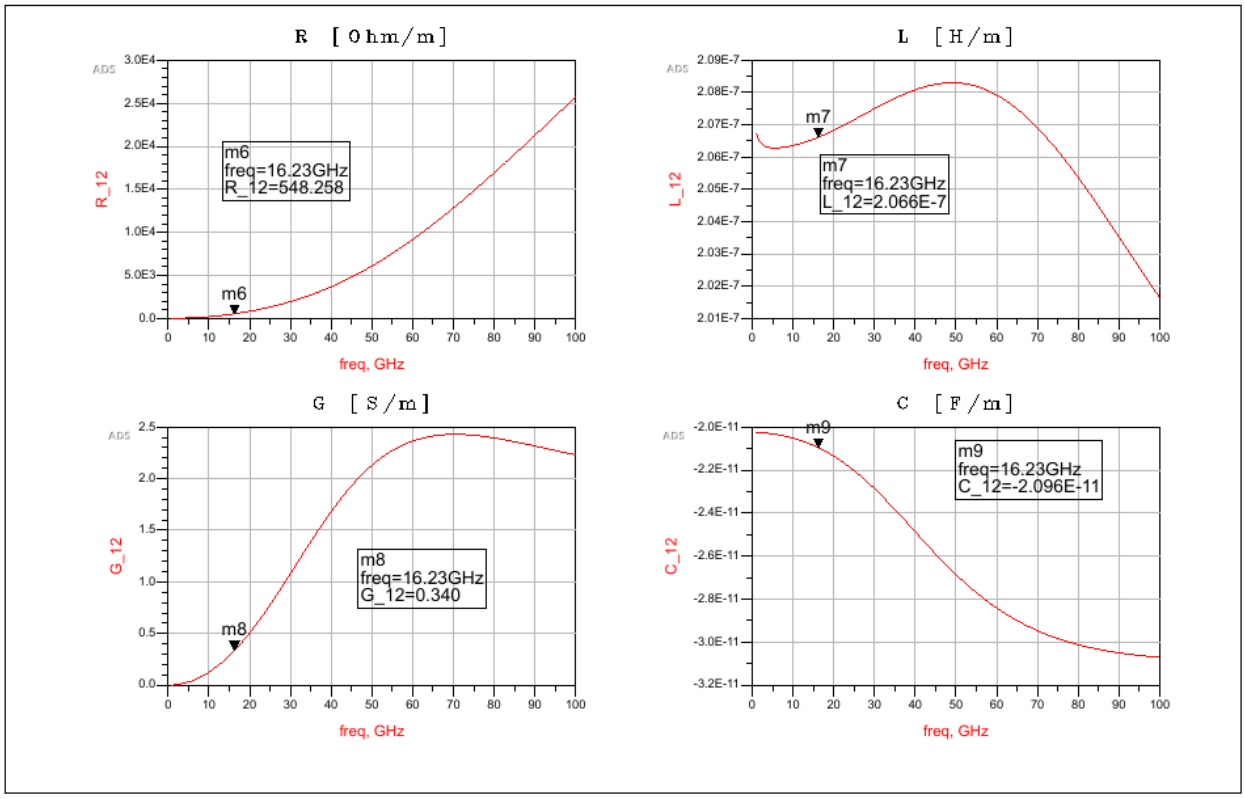


Figure A.2: Mutual RLGC

Appendix B

Full Chip Layout with Pad and Fillers

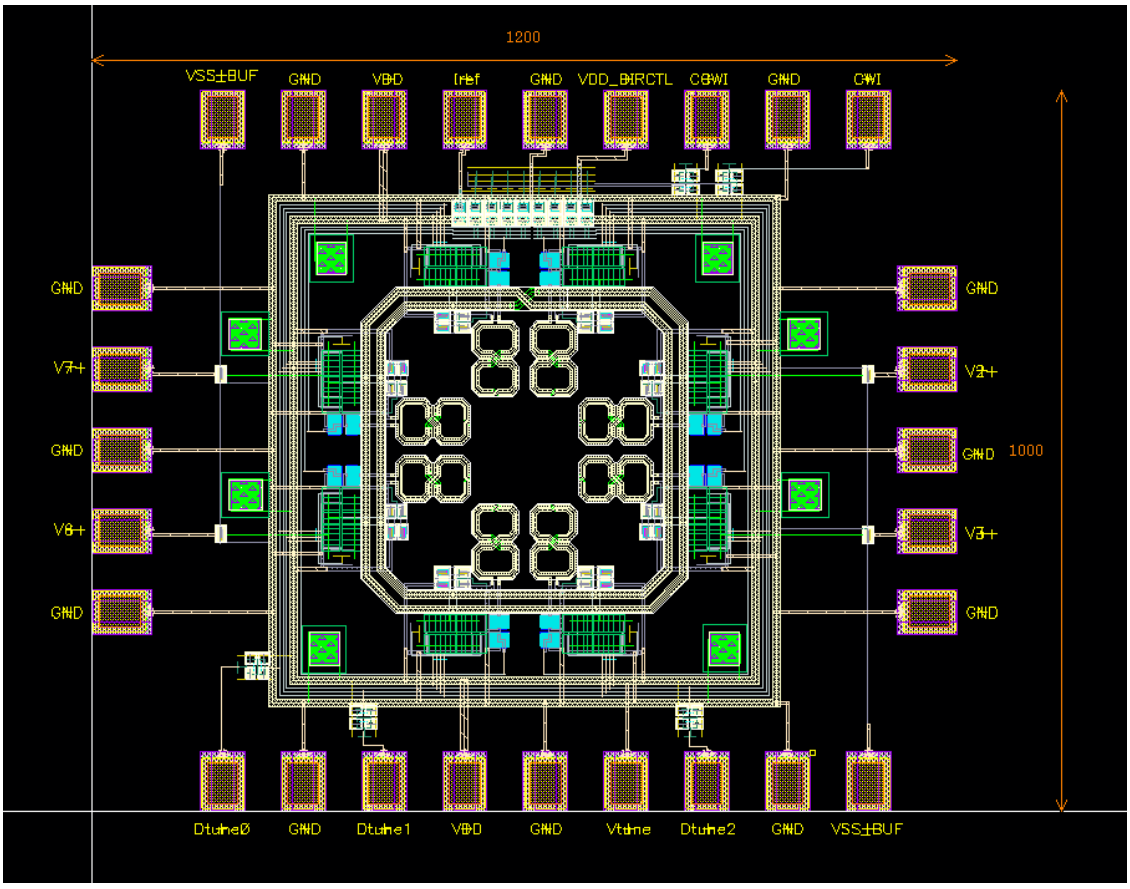


Figure B.1: RTWO(a) full layout

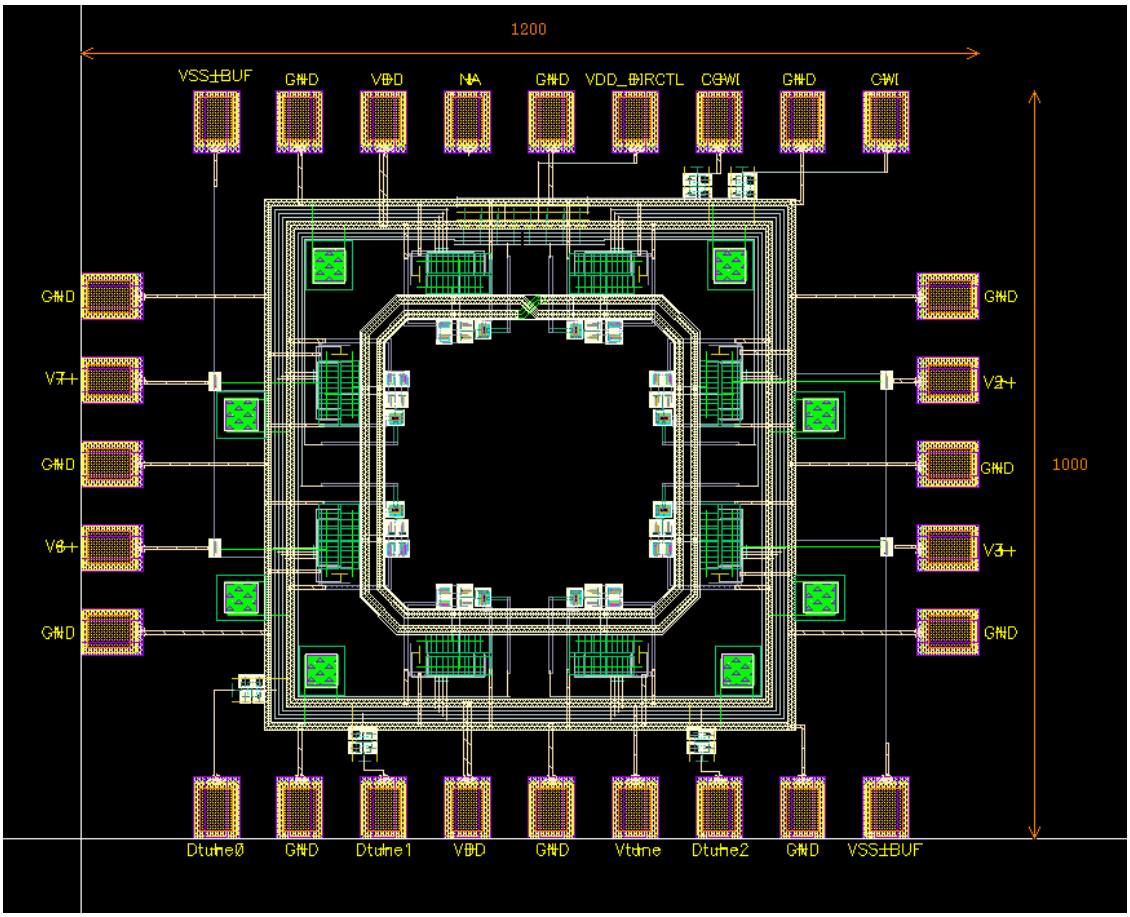


Figure B.2: RTWO(b) full layout

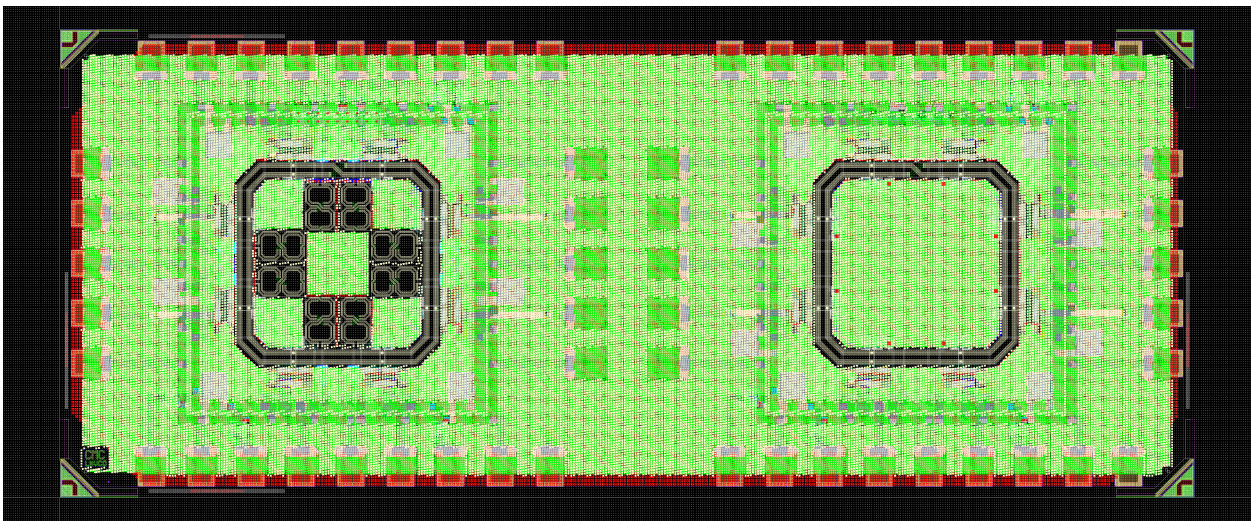


Figure B.3: Filled RTWO

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