Optimum Switch Sizing for Class DE Amplifier

by
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Abstract

Recently, integrated class DE amplifiers without matching networks have been proposed as a compact solution to drive a multi-element piezoelectric ultrasound transducer array for high-intensity focused ultrasound (HIFU) therapy. These transducers produce acoustic energy that translates into heat for tissue ablation. In order to steer the focal zone, each element in the transducer array is driven at a different phase. Hence, there's a need for the power amplifier with a digital control unit in this application.

Since each element in the transducer array has a different electrical characteristic and they have to be driven at the same frequency, it is a challenge to drive all transducers in the array at their optimum conditions. This work introduces strategies to determine efficient driving parameters for an entire transducer array. In addition. a method to improve the power efficiency of the class DE amplifier by choosing the optimum size for switching MOSFETs is also proposed. During the operation of a class DE amplifier, losses are caused by the ON resistance and the drivers of the MOSFET gate capacitances. These parameters are directly dependent on the size of the switching MOSFETs. A wider MOSFET will have a higher gate capacitance, but lower ON resistance. With the correct sizing, these losses can be greatly reduced to improve power efficiency and prevent excessive heating. The challenge with this method is the wide selection of transducers with varying impedance. As the load impedance changes, the MOSFET size also needs to be changed to maintain the maximum power efficiency. Also, the proposed design must deliver at least 1 W output power to the transducer in order to produce enough acoustic pressure. This output requirement will limit the available technology that can be used to design the amplifier. In addition, this work also proposes a new driving circuit that consumes less power to operate, and also allows a full 0-360 degree phase shift.

The design is simulated with Spectre simulator using 0.35 μm 50V CMOS process data available from Austria Micro Systems. The proposed design can deliver 1422mW of average power to 6-elements transducer array, and achieve up to 91% power efficiency.

Acknowledgments

I would like to thank you Lakehead University and CMC Microsystems for supporting this work. This thesis would not possibly be made without the guidance from my supervisor, Dr. Christoffersne, and my co-supervisor, Dr. Zhou. I also would like to thank my family, especially my mom for supporting me during my hard time to complete this thesis.

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List of Symbols

n	–	number of fingers
W	–	Width of a MOSFET transistor
L	–	Length of a MOSFET transistor
W_u	–	Unit width of a MOSFET finger
L_u	–	Unit length of a MOSFET finger
R_u	–	Unit resistance of one MOSFET finger
C_{gate}	–	Total capacitance at the gate of a MOSFET transistor
R_{Driver}	–	Output resistance from the driver circuit
C_{DS}	–	Total drain-to-source capacitance of a MOSFET transistor
C_{G_N}	–	Gate capacitance of one NMOS finger
C_{G_P}	–	Gate capacitance of one PMOS finger
Z	–	Impedance.
R_S	–	Series resistance
L_S	–	Series inductance
C_S	–	Series capacitance
X_S	–	Total reactance in series branch
C_P	–	Total parallel capacitance at the load
R_{SW}	–	Total on-resistance
C_{SW}	–	Total switching capacitance
C_{ext}	–	Total external capacitance added to the load
f	–	Frequency
f_s	–	Series resonance frequency
f_p	–	Parallel resonance frequency
f_{real}	–	Frequency obtained from real part of the impedance
f_{img}	–	Frequency obtained from imaginary part of the impedance
D	–	Duty cycle of the output pulse
t_{on}	–	On-time of the output pulse
T	–	Period of a signal
t	–	Time in seconds
i_D	–	Drain current
V_t	–	Threshold voltage
θ_1	–	First order of mobility degradation
θ_2	–	Second order of mobility degradation
K'	–	Gain factor

SR – Slew rate
ω – Angular frequency
ω_{real} – Angular frequency obtained from real part of the impedance
ω_{img} – Angular frequency obtained from imaginary part of the impedance
Z_o – Load impedance.
R_o – Real part of load impedance.
X_o – Imaginary part of load impedance.
υ_o – Output Votlage
i_o – Output current
i_s – Current flowing through series branch
V_o – The fundamental component of output Votlage
I_s – Phasor corresponding to i_s
I_P – Peak current
V – High voltage power supply
ϕ – Conduction angle in radians
P_L – Load power
P_{RSW} – Conduction power loss
$P_{gate_{Driver}}$ – Power consumed by the gate driver circuit
P_O – Power loss from digital circuit
P_G – Total power loss at the gate of the switch
P_S – Switching Loss
P_{Lost} – Total power loss
η – Driver efficiency
V_a – average load peak voltage
I_a – Effective current going through the load
I_{P_a} – Corrected peak current
k – Effective voltage factor
E – Total energy dissipated
V_G – Voltage applied to the gate of a MOSFET transistor
ΔV – Voltage drop across the switch
δ – $\frac{\Delta V}{V}$ ratio
δ_e – Observed $\frac{\Delta V}{V}$ ratio
CLK – Clock signal
EN – Enable signal
RN – Reset signal
V_{HV1} – High voltage supply to the 30V-50V level shifter
V_{HV2} – High voltage supply to the load and 30V-50V level shifter

List of Abbreviations

HIFU – High Intensity Focused Ultrasound
MRI – Magnetic Resonance Imaging
MOSFET – Metal-Oxide Semiconductor Field-Effect Transistor
NMOS – N-channel MOSFET
PMOS – N-channel MOSFET
ZDS – Zero Derivative Switching
ZVS – Zero Voltage Switching
BVD – Butterworth Van Dyke
DLU – Digital Logic Unit
LPF – Low Pass Filter
LIPUS – Low Intensity Pulsed Ultrasound
CMUT – Capacitive Micromachined Ultrasonic Transducers

Chapter 1

Introduction

1.1 Motivations and Objectives

High intensity focused ultrasound (HIFU) is a non-invasive surgical technique that uses heat to ablate tissue in human body. One common application for HIFU is cancer treatment. Tumor ablation can be done by focusing acoustic energy from the transducers. That energy is translated to heat delivered to the focal zone of the ultrasound transducer. Since it is a very precise operation, it needs to be monitored in real-time by Magnetic Resonance Imaging (MRI). Any body movement can cause a displacement in focal zone, and damage nearby healthy tissue. In order to steer the focal zone of the ultrasound to compensate the body movement, a multi-element HIFU transducer array is needed to produce a proper focal pattern. Each element in the transducer array is driven at different phase, so that the location where the energy is focused can be controlled. Such development entails a driving system that can pilot a large number of elements, with enough power, at the highest-possible efficiency, and must be compatible with MRI environment.

The challenge is that most high power drivers for piezoelectric ultrasound transducers require external matching networks to maximize the output power and minimize the reflections. However, these matching network circuits would interfere with the MRI-guidance system, so they cannot be used. Wong [3] has proposed a class DE amplifier without a matching network design that can output about 1W of power at 90% efficiency. The circuit topology of this amplifier is similar to that of class D topology, but its operation satisfies class E switching condition. The switches are driven by pre-programmed pulse signals applied at the gate of the switching MOSFET. A

shunt capacitor is connected at the load to make a dead time between the switch-on times [5]. Song [4] expanded the work further by making a full-bridge class DE amplifier with a built-in programmable digital circuit to control the frequency and duty cycle.

Even though class DE amplifier designs without matching network have been done, none of those designs focus on optimizing switching MOSFET sizes. The wider the MOSFET, the less on-resistance, which reduces the conduction loss. However, a wider MOSFET has a higher gate capacitance, so the power loss due to gate driving circuit would increase. Therefore, in order to achieve the best-possible power efficiency, the switching MOSFET sizes must be optimized for the particular transducer. Power loss is one of the most important factors in integrated circuit design, as it can cause heating problems, and affect the sustainability of the system. In addition, when driving a transducer array, the excitation frequency must be common for all transducers, but due to small differences in transducer impedances, the optimum driving frequency for each of them is not the same. This problem will cause the amplifier to not being able to operate in ideal class DE condition, and thus increase the switching loss. As a result, the individual duty cycle and external capacitor for each transducer must be adjusted to compensate for variations in the impedance of each array element.

The main objectives of this thesis are:

1. Propose strategies to drive transducer arrays.

2. Develop a design methodology to optimize a driver to a range of transducer impedances.

1.2 Thesis Overview

Chapter 2 reviews basic concepts used in the thesis, along with a brief summary of related published work. Chapter 3 presents an in-depth analysis of the class DE amplifier working under non-ideal operation and two methods to determine the driving parameters for ultrasound transducer arrays. The design of an improved transducer driver is covered in Chapter 4, along with a general design methodology to optimize the driver performance for a given ultrasound transducer impedance. Two case studies are presented to demonstrate the proposed methodology.

1.3 Contribution

Part of this research has been published in [1] and another paper is in preparation to be submitted to IEEE Transaction on Biomedical Circuits and Systems.

Chapter 2

Background Information and Literature Review

2.1 Introduction

Power amplifier is always one of the key components in the transducer driver. Linear amplifiers are often used because of its linear gain and low output impedance. However, the trade-off is a medium to low power efficiency. As a result, some designs use switched amplifiers to reduce the power loss. The most common types of switched amplifiers are class D and class E.

This chapter will first briefly explain the electrical model and characterization of ultrasound transducers. Then, an overview of ultrasound drivers published by other research groups is presented. This chapter also covers the principle of operation of class DE amplifiers and a review of the previously proposed transducer drivers based on this type of amplifier.

2.2 Transducer Characteristic

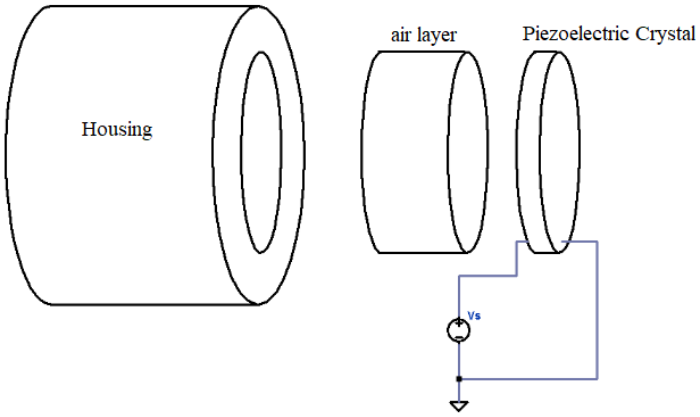

Figure 2.1: Exploded view of a transducer [3]

The transducers used in this work are composed of a piezoelectric crystal, an air backing layer, and a housing to protect the internal connection as shown in Figure 2.1. When there is a voltage applied to the crystal, it will vibrate and produce the ultrasound. The acoustic power will depend on the electrical power from the driver.

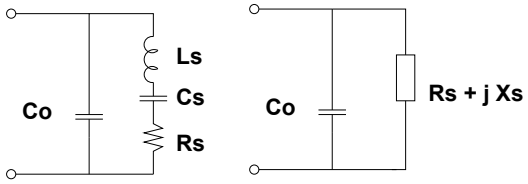

Figure 2.2: Piezoelectric transducer simplified equivalent circuit.

The piezoelectric resonator in the transducer can be represented by a Butterworth Van Dyke (BVD) equivalent circuit, as shown in Fig. 2.2. The series branch consist of L_S, C_S, and R_S components, which determine the mechanical oscillating characteristics of the resonator. The static capacitor, C_o, is determined by the physical characteristics of the resonator. The characteristics of the transducers are measured by using a vector network analyzer. The setup is as shown in Figure 2.3. The transducer is supported so that the one end with the electrical connector is above the water surface, while its crystal part is submerged in the water. The absorber is placed on the bottom of the water bucket. The transducer is then connected to the

vector analyzer to measure its S parameters. Figure 2.4 shows an example of a magnitude of the transducer impedance vs. frequency plot. There are 2 sets of transducer arrays used in this work. Their physical sizes and electrical characteristics will be discussed in Chapter 3.

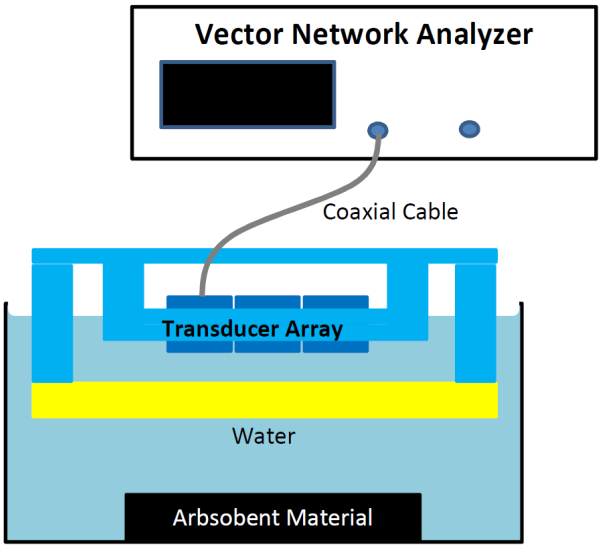

Figure 2.3: Measuring the impedance of the transducers

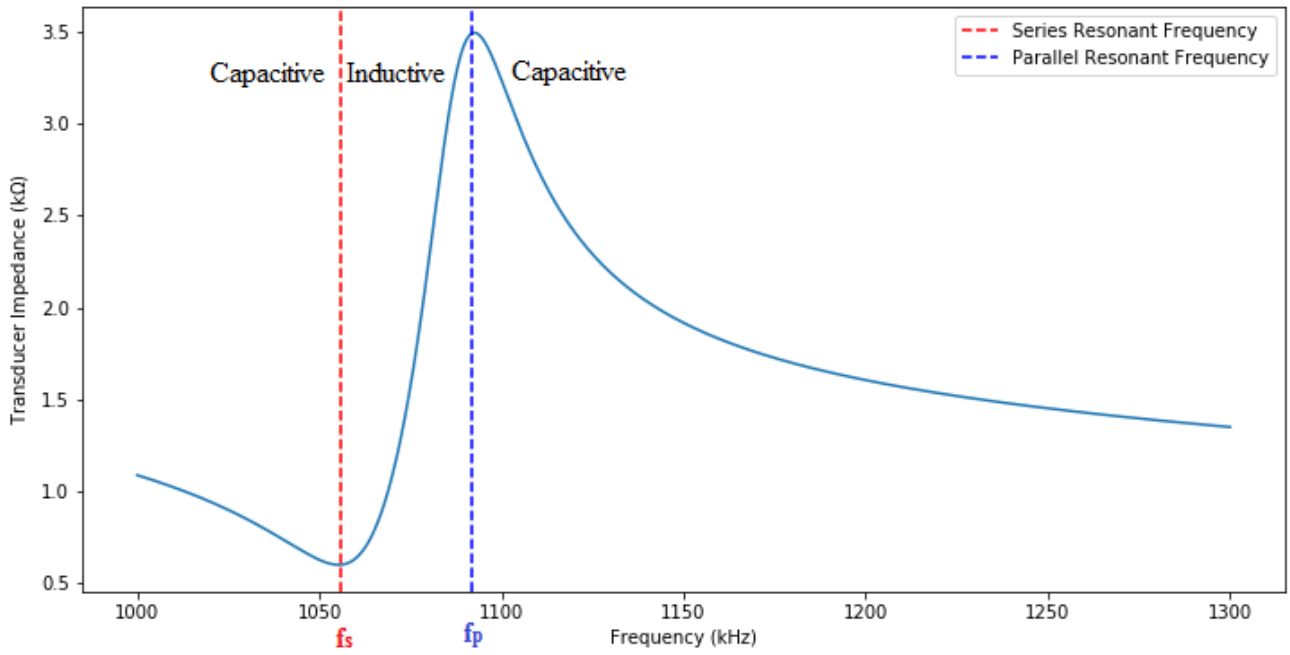

Figure 2.4: Magnitude of the Transducer Impeadance vs Operating Frequency. f_s is the series resonant frequency, where as f_p is the parallel resonant frequency [15]

2.3 Previous Work on RF Amplifiers

2.3.1 Class A, B and AB amplifiers

In these topologies, the output voltage follows the voltage from the input. The differences between these 3 classes are their biasing conditions, and angle of conduction [13]. A tuned matching network is often used for impedance matching and harmonic filter, and thus improve the power efficiency of the circuit. However, the main objective of this research is to design a driver without a matching network to eliminate all inductive components. Therefore, this type of circuit will not be considered in the design.

Capineri [12] has used a class AB amplifier to obtain a low-output-impedance and linear-gain amplifier to drive ultrasound transducer arrays. This design is composed of discrete components, and is used to drive the transducer array for diagnosis, and it offers a low power efficiency as shown in Table 2.1. As a result, the proposed system from Capinery does not meet the objectives of this thesis.

A more recent work done by D. Ghisu [11] has used class AB topology to design a high bandwidth linear amplifier for medical ultrasonic transmitter applications. Even though, the

author never mentions the overall efficiency of the design, class AB amplifier can only achieves 50% - 78.5% power efficiency theoretically [13]

Table 2.1: Results from Capineri's class AB design

$R_L(\Omega)$	5.6		18		120	
f (MHz)	1	10	1	10	1	10
P_{out} (W)	59.89	43.21	23.44	19.36	3.65	3.09
η (%)	56.39	64.88	41.73	32.49	9.84	5.66

2.3.2 Class D amplifier

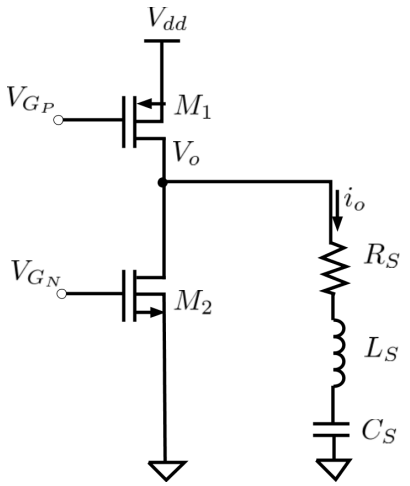

Figure 2.5: Schematic of class D amplifier[14]

The schematic for class D amplifier is shown in Figure 2.5. This type of amplifier can also be used as an inverter, which uses the same pulse signal for both M1 and M2, so that only the NMOS M1 or the PMOS M2 is turned ON at a time [35]. However, the switching transistors in this topology are often driven by 2 separate pulses to prevent the current spike during the transition when M1 and M2 are turned ON/OFF at the same time. When the PMOS M1 conducts, there is a current path from Vdd to the load. On the other hand, when M1 is off, M2 will conduct and let the load discharge. The waveform for this type of amplifier is shown in Figure 2.6, where V_{in} is used to drive both the NMOS M1 and PMOS M2. In general, class D amplifier must operate above the series resonant frequency of the load because current spikes created by leading current of a capacitive load can cause a breakdown of a parasitic bipolar transistor inside a MOSFET during an on-off transition [14]. However, this efficiency for this type of amplifier is reduced by the parasitic capacitance across the switching MOSFET under high-frequency operation.

Using this class D topology, Hall and Cain [35] have proposed a driver that can output 20 W of output power, at 90% power efficiency, for a 512-channel transducer array. The transistors M1 and M2 are driven by the pulse signal TTL_in. The inductor L1 and capacitor C1 are used to tune the amplifier to cancel out the higher harmonics.

Agbossou has proposed a class D amplifier in a full bridge configuration to drive the piezoelectric transducers for a chemical reactor plant [15]. The design is shown in Figure 2.8. According

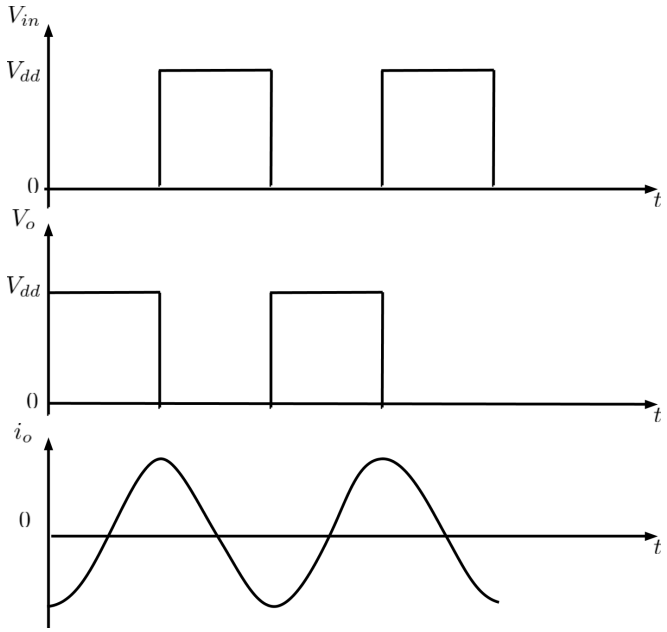

Figure 2.6: Waveforms of class D amplifier [14]

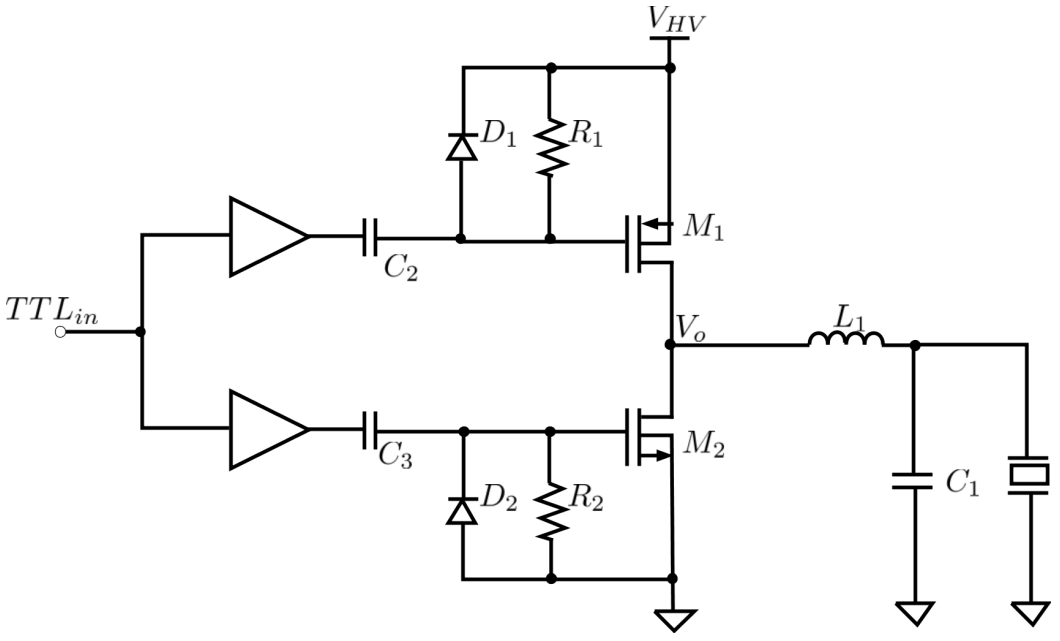

Figure 2.7: Schematic of the transducer driver proposed by Hall and Cain

to the author, the driver can output 2 kW of power, at > 90% power efficiency. Due to the characteristics of the transducers changing with the temperature, as the operating frequency is slightly different from the transducer series resonant frequency, the load will most likely become capacitive . By connecting a Low Pass Filter (LPF) in front of the load, it will have an inductive characteristic when the operating frequency is higher than the transducer's resonant frequency.

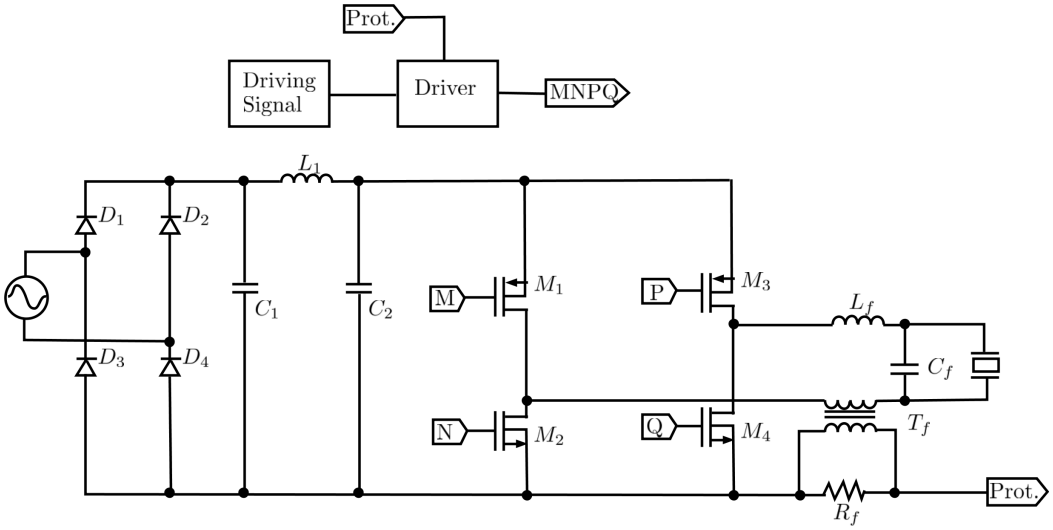

Figure 2.8: Schematic of class D Amplifier proposed by Agbossou [15]

Another class D Amplifier is designed by Yang and Xu [16] for Audio Beam system as shown in Figure 2.9. The application has the switching frequency of 600 kHz. The 2 resistors in this design are used along with the OPAMP and the gate driving circuit to provide over-current protection to the switching MOSFET. The 2 inductors L1 and L2 are needed to reduce instantaneous current through the transducer.

Lewis and Olbricht [21] have developed a 48 W, 1.54 MHz high intensity ultrasound driver that do not require matching network for military and medical applications, as shown in Figure 2.10. In order to deliver all power from the voltage supply to the load, the output impedance of the amplifier is designed to be lower than 0.05 Ω. Multiple transistors are stacked in parallel to achieve the target output impedance. The design is implemented using discrete components to reduce the cost.

Ang *et al.* [22] have designed a 0.8 W, 1.5 MHz integrated amplifier for Low Intensity Pulsed Ultrasound (LIPUS) applications as shown in Figure 2.11. LIPUS is an emerging technique that

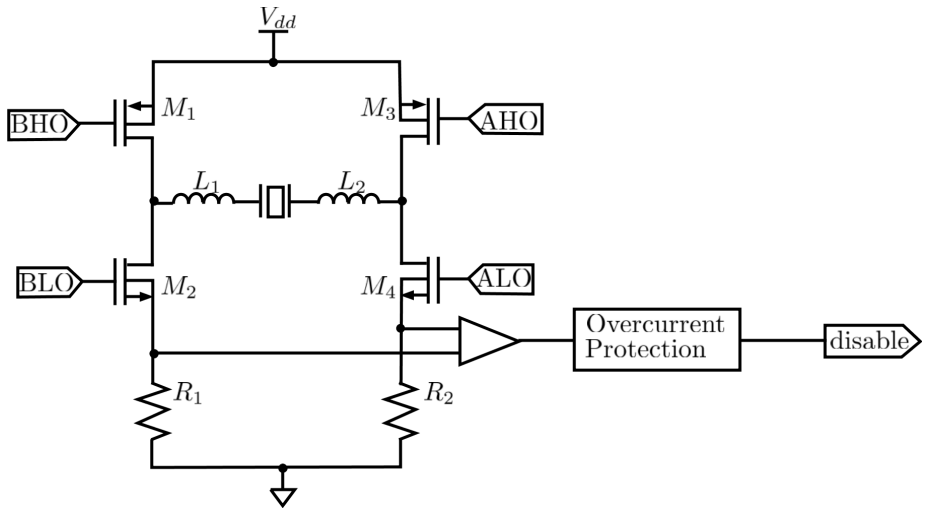

Figure 2.9: Schematic of a class D amplifier proposed by Yang and Xu [16]

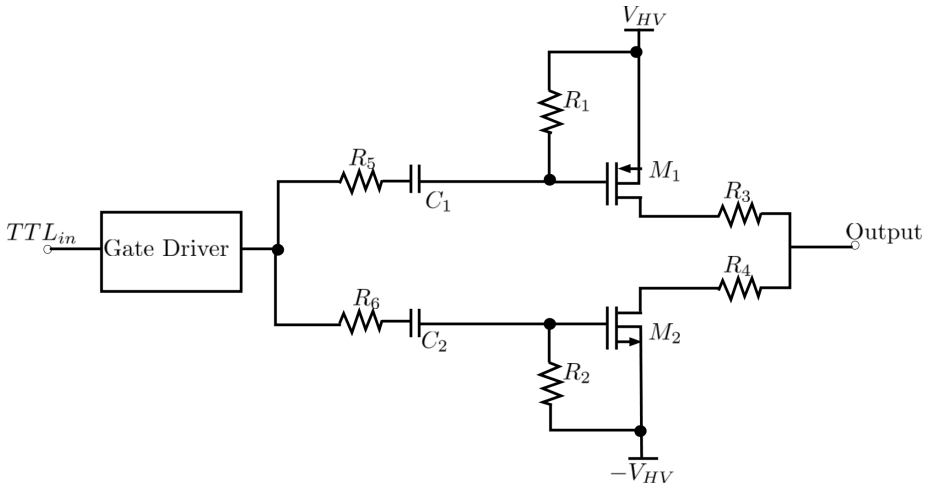

Figure 2.10: Schematic of the switched-mode amplifier proposed by Lewis and Olbricht [21]

uses ultrasound for bone, tooth-root healing, and dental tissue formation. The overall efficiency of the system is approximately 70%. However, this design requires an external matching LC network for impedance matching, and eliminate higher harmonic contents from the output signals.

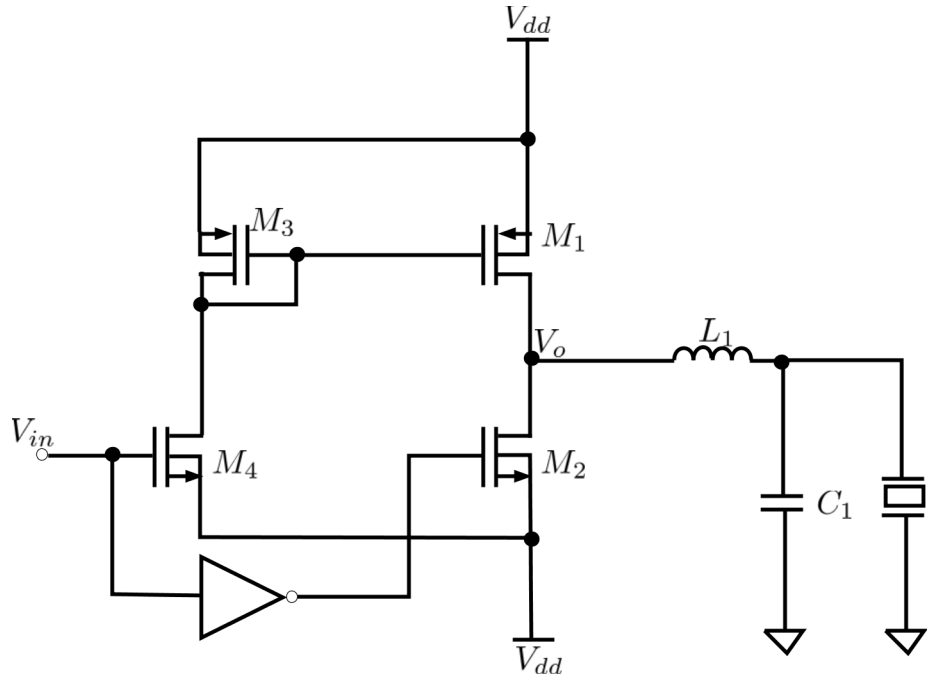

Figure 2.11: Schematic of LIPUS amplifier proposed in [22]

One of the most recent design is done by O. Farhanieh and A. Bozkurt [20]. This group has designed a drive system for Capacitive Micromachined Ultrasonic Transducers (CMUT) array. Their goal is to design a system that is as compact as possible, so that the transducer probe can be used at a difficult-to-reach location inside the human body. The reason why they use CMUTs in this design are because CMUTs don't need backing layer, and suffer less from self heating. The proposed system consists of a built-in clock signal, pulse generator, and a high-voltage class D amplifier. According to the authors, while driving 20 V_{pp} pulse into the transducer at 10 MHz, the system consumes 560 mW power, and 130 mW of which is delivered to the load. The overall efficiency is 23%.

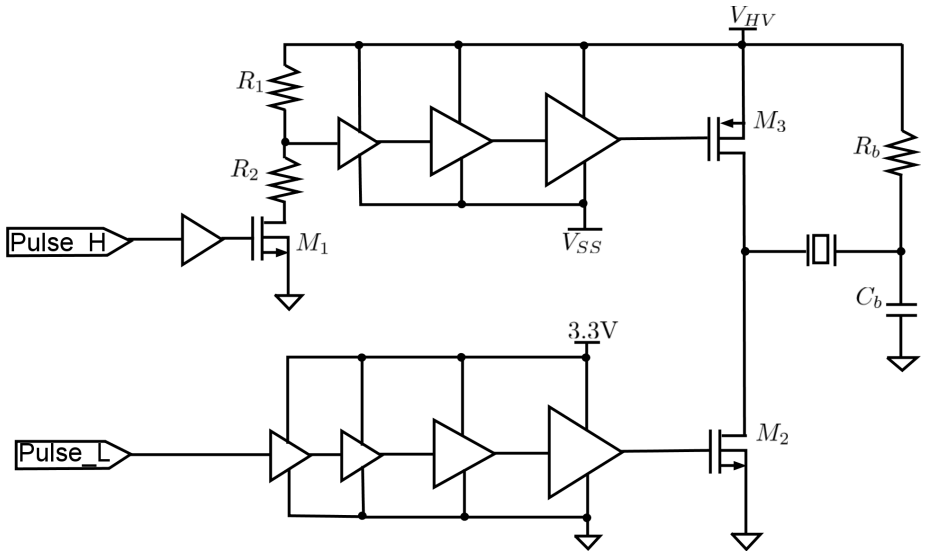

Figure 2.12: Proposed Amplifier from O. Farhanieh [20]

2.3.3 Class E Amplifier

A typical class E amplifier design is as shown in Figure 2.13, which theoretically offers 100% power efficiency. The choke inductor L_f allows v_{DS} to slowly get to 0V at the same time that M1 conducts. This feature allows zero voltage switching (ZVS) and zero derivative switching (ZDS) conditions to eliminate the switching loss. The output waveform of class E amplifier is shown in Figure 2.14.

Tao Yuan has proposed a class E amplifier [10] to drive an inductive load transducer. In his work, he mentions that operating the transducer at its series resonant frequency does not take advantage of the loss reduction mechanism, which occurs between the resonant and anti-resonant frequencies. Therefore, for maximum transducer conversion efficiency, the operation frequency has to be selected in this range, leaving the transducer load to have an inductive characteristic. In order to make the load resistive, an external capacitor is connected to the load as shown in Figure 2.15.

Another class E amplifier circuit is designed by Chen et. al [19]. Output power from this design is said to be 42 W at 42 kHz, and up to 90% efficiency. The circuit consists of an AC power regulator, fly-back circuit, and a class E amplifier.

Even though class E offers high power efficiency, this type of amplifier cannot be used in the HIFU application due to the choke inductor L_f in the design. In order for this amplifier to

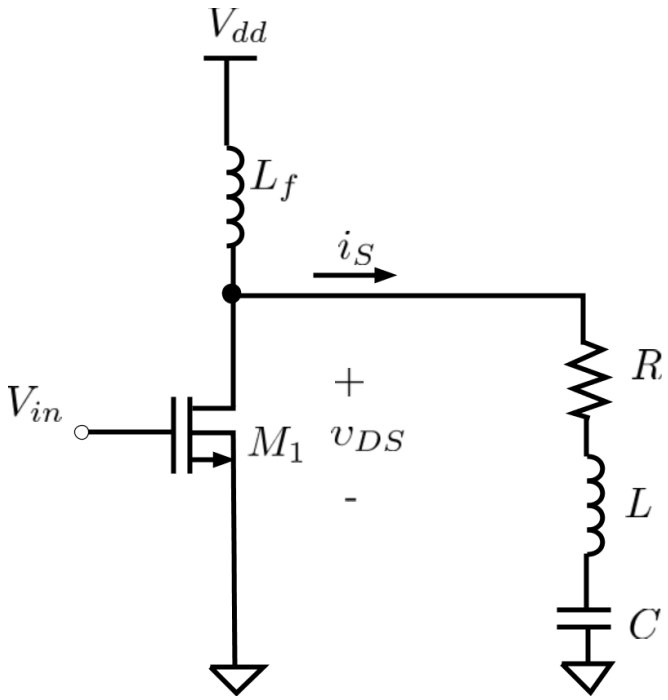

Figure 2.13: Schematic of class E amplifier [14]

work, a big inductor is required, which would consume a lot of die area inside the chip. A 10 nH integrated spiral inductor can consume 226x226 μm^2 in die area [29]. Whereas, the choke inductor used in [10] is about 4 mH, which is not feasible to integrate inside a chip. Also, if the design is intended to work in MRI environment, it is limited to use air-core inductor only.

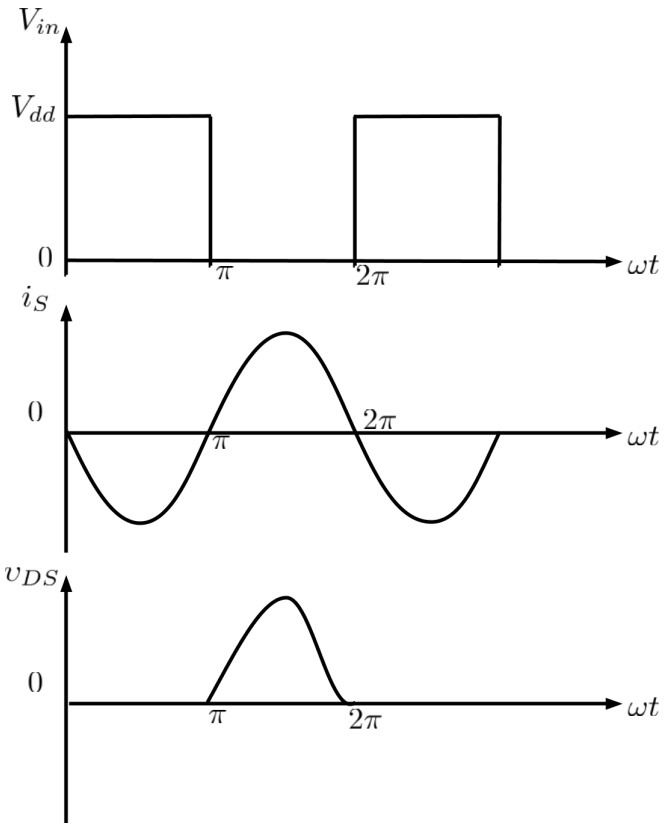

Figure 2.14: Waveforms of class E amplifier [14]

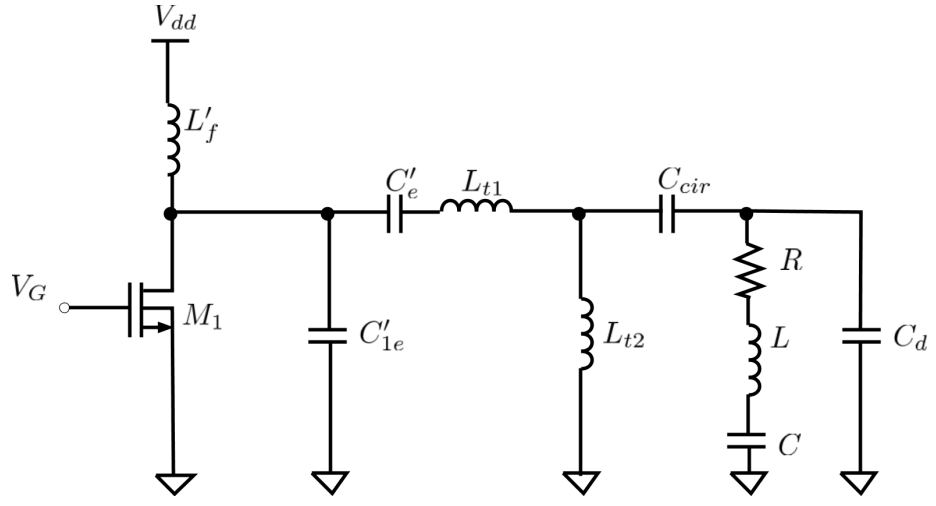

Figure 2.15: Yuan's class E Amplifier Design [10]

2.3.4 Class DE amplifier

Another type of switched amplifier is class DE, which uses a similar circuit as class D while maintaining ZVS and ZDS conditions as class E. The simplified circuit is shown in Figure 2.16, and the output waveform is displayed in Figure 2.17. The circuit in this topology is similar to class D amplifier. The differences are at the shunt capacitor (C_P), a tuned circuit composed of L_s and C_s, and the gate driving signals. The shunt capacitor is a part of the tuned circuit, which includes the parasitic capacitance from switching MOSFETs. The tuned circuit is needed to maintain class E switching conditions. The duty cycle of the gate driving signal is typically around 25%, which is different than the 50% duty cycle in class D amplifier to allow more dead time between the switch-on time.

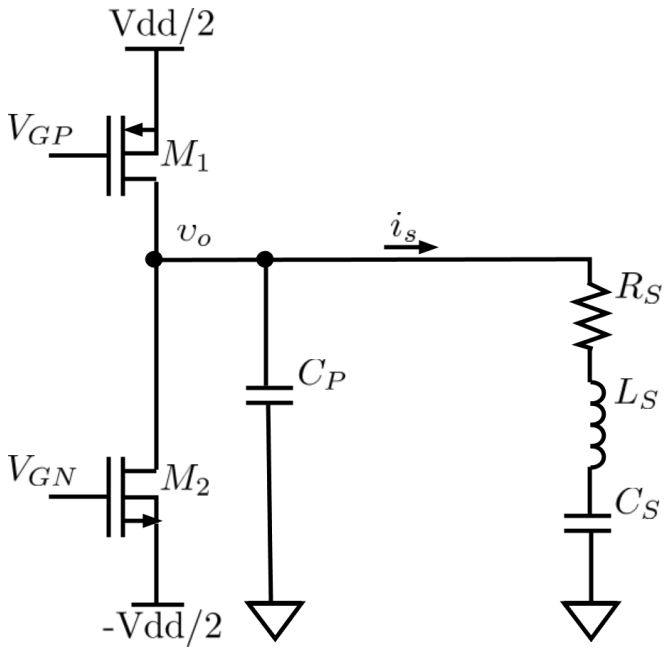

Figure 2.16: Class DE simplified circuit

During the ϕ to π interval, M1 is turned ON, while M2 is OFF. The current flowing through the series branch, i_s, raises from 0 to its maximum value. The output voltage, v_o, is equal to the voltage from the supply (V). The potential across C_P is 0V during this interval, so no current flows through the parallel branch. The drain-to-source voltage of M1 is 0 V throughout this interval.

From π to $\pi + \phi$, all transistors are switched OFF. Hence, there is no current flowing through

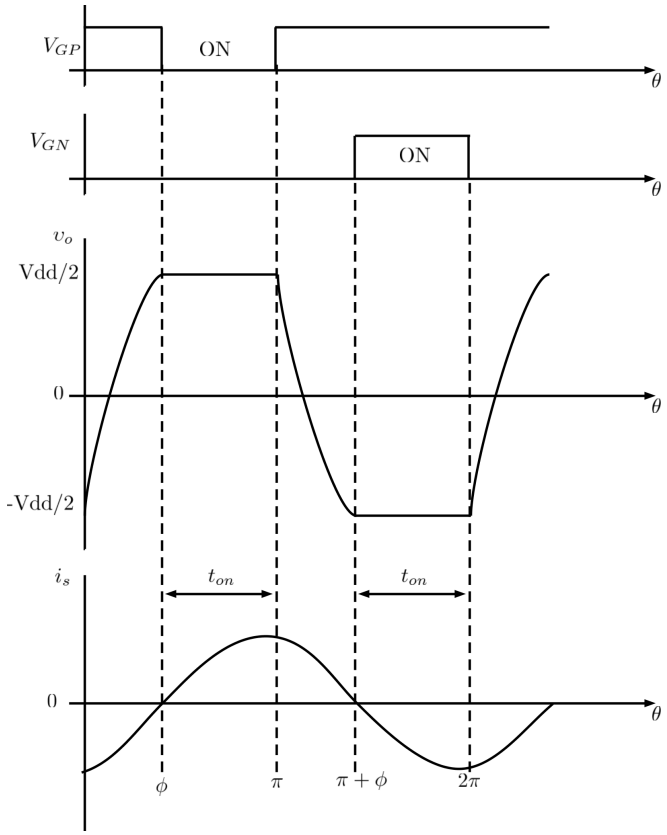

Figure 2.17: Class DE waveform

the transistors during this interval. The parallel capacitor, C_P, will provide the current to the series branch. The current will start to decrease from its maximum value to 0 at the end of the interval. At the same time, υ_o also decreases from its highest potential (V) to its lowest potential (-V), so the voltage across M2 is 0V. The derivative of υ_o also becomes zero at the end of this interval. As a result, both ZVS and ZDS conditions are satisfied at the instant when M2 is turned ON.

Between $\pi + \phi$ to 2π, M1 stays OFF, whereas M2 is turned ON. The current i_s is now flowing through the drain to source of M2, in the opposite direction. The output voltage, υ_o is held at -V, so the drain-to-source voltage of M2 is 0 V throughout this interval.

From 0 or 2π to ϕ, all transistors are switched OFF. C_S and L_S keep the continuity of the current by discharge through C_P. As a result, by the time i_s reaches 0 A at the end of the interval, υ_o approaches +V, and its derivative becomes zero, which satisfies both ZVS and ZDS conditions.

Since the transducer's equivalent circuit is a series-parallel RLC circuit, it can be used as part of the tuned network for class DE amplifier. Class E switching conditions can still be enforced by connecting an external capacitor across the transducer load. Wong [3] has proposed a transducer driver using this topology to drive a transducer load. This design consists of a logic block, gate drivers, and a push-pull amplifier at the output stage as shown in Figure 2.18. The logic block in this design is used to ensure that the 2 switches M1 and M2 do not close at once. Since part of the tuned network is fixed by the equivalent circuit of the transducer, the amplifier may not be able to operate in ideal class DE condition [7]. The value of C_{ext} has to be calculated, and readjusted to account for this condition.

Using the same topology, Song [4] has changed the design to a full-bridge configuration to increase the output power. The proposed design is shown in Figure 2.19, which consists of a programmable digital logic unit (DLU), 4 gate drivers, and the H-bridge amplifier. The logic unit is programmable, so the design can drive different transducers at the optimum duty cycle to achieve better efficiency. Similar to the half-bridge configuration, this design also has 4 intervals that satisfy ZVS and ZDS conditions when the switches are turned ON. However, with this design, the output peak-to-peak voltage is doubled, so the output power is thus increased by 4 times when using the same DC supply voltage.

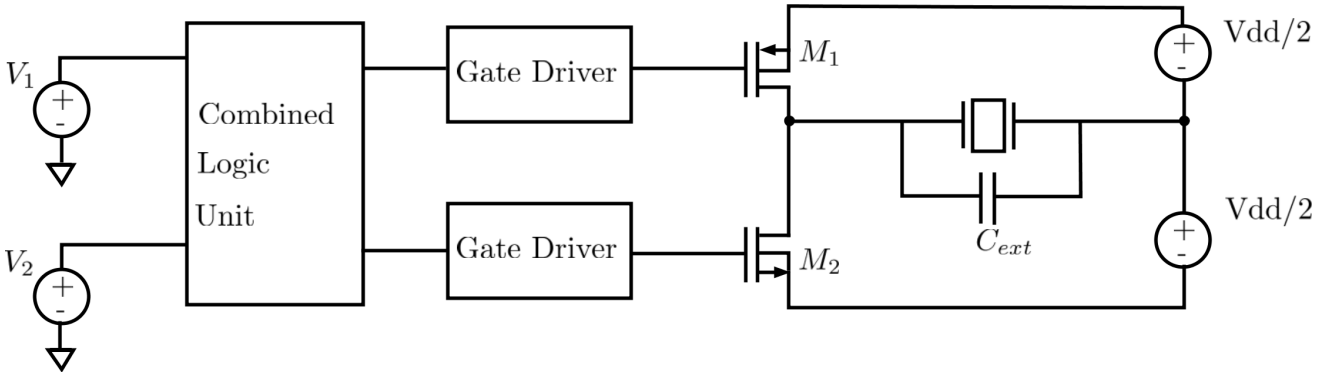

Figure 2.18: Overall system of Wai's design [3]

Wong's and Song's designs are compared with other designs discussed in previous sections as shown in Table 2.2. Wong's design achieves a higher power efficiency. By utilizing full-bridge configuration, Song's design can achieve higher output power at the expense of lower efficiency. However, both of these works are designed to drive a single transducer. When a transducer array is considered, the excitation frequency must be common for all transducers, but the individual duty cycle and external capacitor for each transducer must be adjusted to compensate for variations in the impedance of each array element.

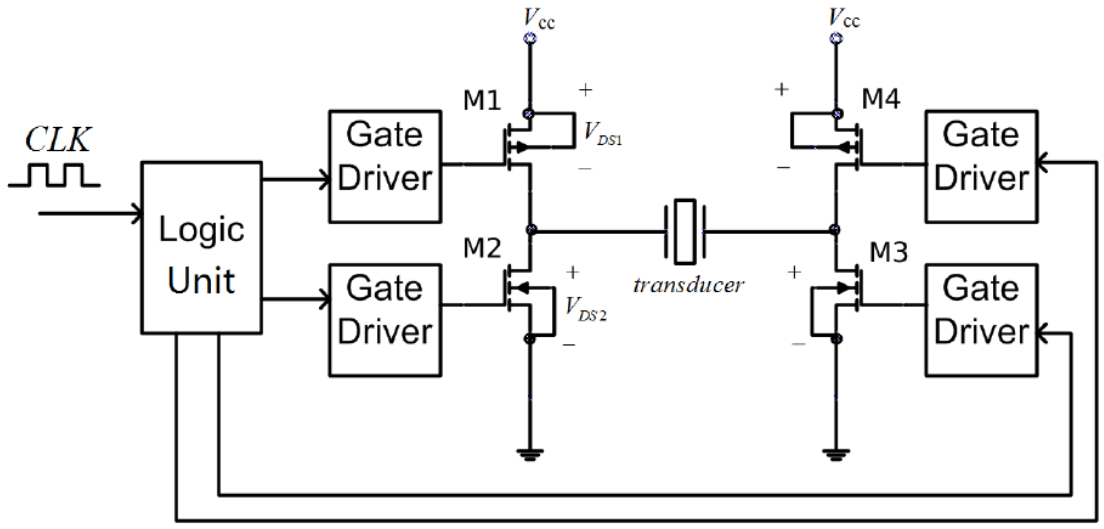

Figure 2.19: Proposed design by Ruiqi [4]

2.3.5 Summary

Table 2.2 summarizes all reviewed works in this chapter. Overall, class DE topology is more suitable for HIFU application because it offers high power efficiency without using matching network.

Table 2.2: PreviousRF amplifier designs comparison

Reference	Topology	Output Power (W)	Efficiency (%)	Features	Comments
[12]	Class AB	60	56	Using only discrete components, no matching network required	Lower power efficiency
[35]	Class D	20	90	Handle 512 channel array	Requires: LC tuning network, protection resistors, and unchanged drive signal
[15]	Class D	2000	90	High output power, auto adjust the load characteristic	Require matching network
[21]	Class D	50	90	Cost-effective, high efficiency	Using discrete components, high output capacitance
[22]	Class D	0.8	70	built-in pulse generator, compact	Requires external LC matching network
[20]	Class D	0.13	23	Built-in CLK signal, pulse generator, power amplifier	Low Output Power
[19]	Class E	42	90	AC power regulator	Requires LC matching network
[3]	Class DE	1	91.5	No matching network required	non-programmable DLU
[4]	Class DE	3.6	89	Programmable digital logic unit	Driver's circuit consumes too much power and does not allow 0^o to 360^o phase shift.

Chapter 3

Strategies to Drive Ultrasound Transducer Arrays

3.1 Introduction

Practically, amplifiers cannot all operate in ideal class DE condition while driving an array. This is because all transducers in the array must be driven at the same frequency, but due to small differences in transducer impedances, the optimum driving frequency for each one is not the same. Moreover, some transducers do not even allow ideal class DE condition at any frequency [3]. Therefore, the transducers may be driven outside of ideal conditions. The operation of the class DE amplifier in this mode will be analyzed first considering switching and other losses. Using the results of this analysis, two methods to drive transducer arrays are developed and validated.

3.2 Amplifier Analysis

The simplified circuit is shown in Figure 3.1. The parallel capacitor,

$$C_P = C_O + C_{SW} + C_{ext}, \tag{3.1}$$

includes the transducer parallel capacitor (C_O), the parasitic capacitance of the switches (C_{SW}), and any additional external capacitance (C_{ext}). If optimum class DE switching conditions are not possible,zero voltage switching (ZVS) is relaxed while zero derivative switching (ZDS) is still enforced as shown in Figure 3.2. ZDS is needed to reduce the sensitivity to parameter variations. The circuit analysis is done with the following assumptions:

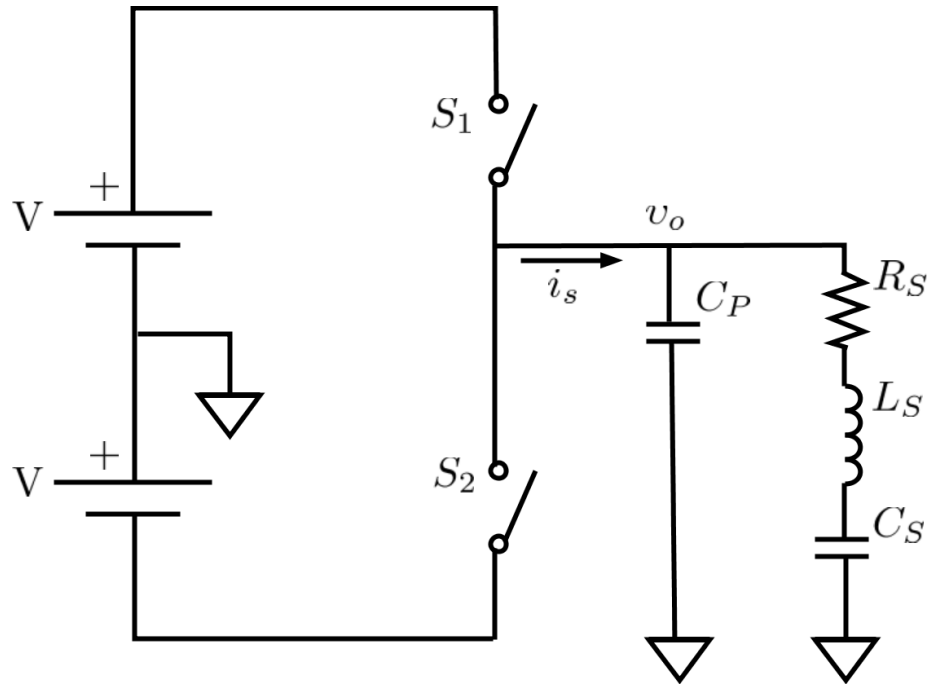

Figure 3.1: Simplified class DE circuit

- Capacitors are ideal.
- Transistors are replaced by ideal switches . There are no parasitic capacitance, no channel resistance, no turn-on and turn-off delays and an infinite amount of resistance while turned off.

At the instance when the switch is ON, the voltage difference at the switch is defined as ΔV. The energy loss due to the suboptimal switching (E_S) is:

$$E_S = \frac{1}{2} C_P \Delta V^2. \tag{3.2}$$

The average power loss due to switch is thus can be estimated:

$$P_S = \frac{1}{T} C_P \Delta V^2. \tag{3.3}$$

The duty cycle indicate the amount of on-time (t_{on}) over a period (T):

$$D = \frac{t_{on}}{T}. \tag{3.4}$$

The conduction angle (ϕ) is thus:

$$\phi = \pi(1 - 2D). \tag{3.5}$$

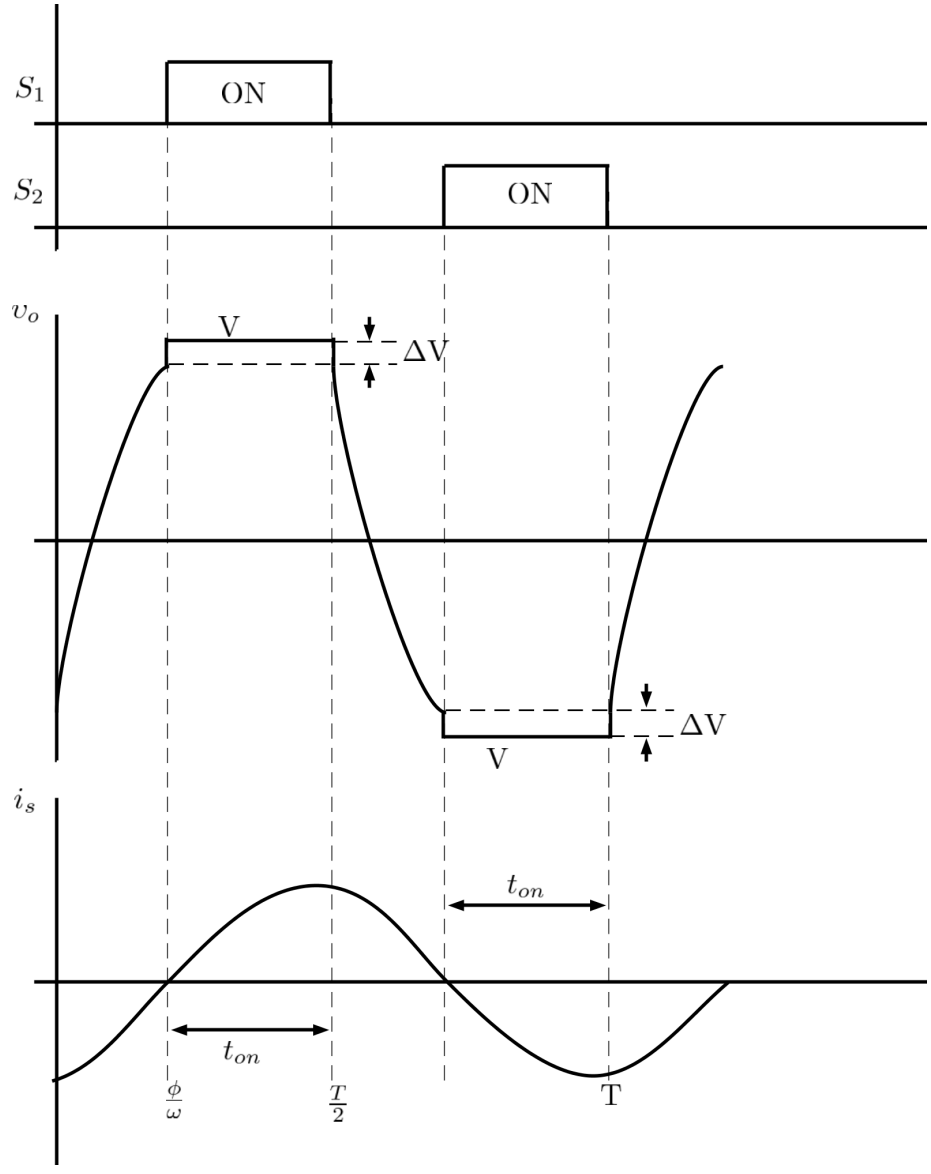

Figure 3.2: Class DE output waveform outside optimum condition

The current in the series branch can be approximated by:

$$i_s = I_P sin(\omega t - \phi), \tag{3.6}$$

where I_P is the peak value, $\omega = 2\pi/T$, and t is time. During the interval $[0,\frac{\phi}{\omega}]$, when all of the MOSFET switches are OFF, the current through the series branch is supplied by the capacitor C_P:

$$i_s = -C_P \frac{dv_o}{dt}. \tag{3.7}$$

Substituting Equation (3.7) into (3.6), and integrate the equation in the $[0, \frac{\phi}{\omega}]$ interval:

$$v_o = \frac{I_P}{\omega C_P} cos(\omega t - \phi) + C. \tag{3.8}$$

Applying the following boundary conditions to Equation (3.8):

$$v_o(t = 0) = -V,$$
$$v_o(t = \phi/\omega) = V - \Delta V,$$

the output voltage for $0 \leq t \leq \frac{\phi}{\omega}$ is found to be:

$$v_o = \frac{I_p}{\omega C_p} \left[cos(\omega t - \phi) - cos\phi - \frac{1 - cos\phi}{2 - \delta} \right], \tag{3.9}$$

where $\delta = \Delta V/V$, and the peak current is given by:

$$I_P = \frac{(2 - \delta)\omega C_P V}{1 - cos\phi}. \tag{3.10}$$

Then, the average load power (P_{L1}) can be estimated by

$$P_{L1} = \frac{1}{2} R_S I_P^2. \tag{3.11}$$

The operation of class DE outside its ideal condition has been studied in [7]. To obtain the optimum frequency and duty cycle for the transducer operating outside class DE condition, the fundamental component of the output voltage (Vo) is defined using Fourier Analysis:

$$V_o = \frac{2}{T} \int_0^T v_o(t) exp(-j\omega t) dt.$$

The required series branch impedance (Z_S) is obtained as the ratio of V_o and the phasor corresponding i_s (I_s)

$$Z_S = R_S + jX_S = \frac{V_o}{I_s}. \tag{3.12}$$

By equating the real and imaginary components of the series impedance, the condition for class DE can be found as:

$$\omega C_P R_s = \frac{1 - cos(2\phi) + \delta(\frac{3}{2} + \frac{cos(2\phi)}{2} - 2cos\phi)}{(2-\delta)\pi}, \tag{3.13}$$

$$\omega C_P X_s = \frac{2\phi - sin(2\phi)}{2\pi}. \tag{3.14}$$

In the case when the switch resistance (R_{SW}) plays a big factor in the power losses (R_{SW} is not too small compared to R_S). The voltage reduction at the load is approximated here as follows:

$$V_a = V - R_{SW} I_a = V - \frac{R_u I_a}{n}, \tag{3.15}$$

where V_a is the average load peak voltage, and I_a is the average current going through the switch during the ON-period of the MOSFET $[\phi, \pi]$. The corrected peak current (I_{P_a}) can be obtained from Equation (3.10) as follows:

$$I_{P_a} = \frac{(2-\delta)\omega C_P V_a}{1 - cos\phi}. \tag{3.16}$$

The average current I_a can be obtained by averaging the current during the conduction interval [ϕ, π]:

$$I_a = \frac{(2-\delta)\omega C_P V_a}{1-cos\phi} \left(\frac{1}{\pi - \phi} \int_\phi^\pi sin(\theta - \phi) d\theta \right),$$

$$I_a = \frac{(2-\delta)\omega C_P V_a}{(1-cos\phi)(\pi-\phi)} \left(1 - cos(\pi - \phi)\right). \tag{3.17}$$

Substituting Equation (3.17) into (3.15) to obtain the average voltage as follows:

$$V_a = \frac{1}{1+k} V, \tag{3.18}$$

where k is given by:

$$k = \frac{(2-\delta) R_{SW} \omega C_P (1 - cos(\pi - \phi))}{(1 - cos\phi)(\pi - \phi)}. \tag{3.19}$$

Using the Equation (3.10) for the peak current and (3.18) for the effective voltage, the load power considering the effect of switch resistance is approximated as follows:

$$P_L \approx \frac{1}{2} R_S \left(\frac{(2-\delta)\omega C_P V}{(1+k)(1 - cos(\phi))} \right)^2. \tag{3.20}$$

During the ON state of the switches (from ϕ to π), the conduction loss (P_{RSW}) caused by the NMOS and PMOS can be estimated by:

$$P_{RSW} = 2\left[\frac{1}{\pi}\int_{\phi}^{\pi} R_{SW}[I_{Pa}sin(\theta-\phi)]^2 d\theta\right]. \tag{3.21}$$

Solving the integral in Equation (3.21), and combining with (3.20) to set

$$P_{RSW} = 2\frac{R_{SW}}{R_S}P_L[1-\frac{\phi}{\pi}+\frac{sin(2\phi)}{2\pi}]. \tag{3.22}$$

The observed voltage difference at the switch during the on-time can be estimated by:

$$\Delta V = \delta V_a + (V - V_a) = \frac{\delta + k}{1+k}V = \delta_e V, \tag{3.23}$$

where $\delta_e = \frac{\delta+k}{1+k}$. The energy lost due to the non-optimal switching condition is derived from 3.3

$$P_S = fC_P\delta_e^2 V^2. \tag{3.24}$$

Then, the total power loss (P_{Loss}) is:

$$P_{Loss} = P_S + P_G + P_{RSW}, \tag{3.25}$$

where P_G is the power loss caused by the driving circuit. A small portion of this power loss is from the digital logic unit, whereas the majority is from the gate driver's circuit connected at the gate of the switching MOSFET. This power loss depends on the gate capacitance, thus it increases with frequency. The driver efficiency (η) is defined as:

$$\eta = \frac{P_L}{P_L + P_{Loss}}. \tag{3.26}$$

3.3 Method I - Driving Parameters for Efficiency

3.3.1 Introduction

As mentioned in section 3.2, when driving a transducer array, due to variations in the impedance of each array element, it is usually not possible to simultaneously drive all transducers in the ideal conditions. Furthermore, some transducers don't even admit ideal class DE operation. The following method can be used to determine the drive parameters to achieve the best-possible power efficiency in sub-optimal class DE operation, and predict load power and losses in each amplifier.

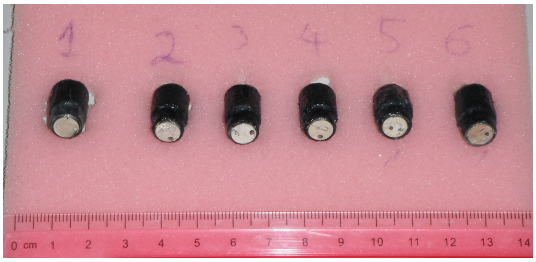

Figure 3.3: Transducer array used in this work

3.3.2 Transducer Characterization

The piezoelectric transducers used in this work are shown in Figure 3.3. The crystal is shaped as a disc with a diameter of 7 mm and a thickness of 2.8 mm. The proposed drive method would work with any set of transducer array. However, this particular transducer array is chosen because it's available in the lab, and it does not support ideal class DE operation. The intention of this research is to predict the load power and switching losses in the extreme case when the driver is not originally designed for the particular transducer array. To consider the variations in acoustic environment, two characterization setups were performed for each transducer. The first one is with absorber material in parallel with the transducer (Table 3.1) and another with the absorber material at an angle of 45^o respect to the transducer (Table 3.2).

Table 3.1: Characteristics of the transducer array with parallel absorber

Transducer	1	2	3	4	5	6
f_S (kHz)	1054	1055	1055	1056	1056	1054
f_P (kHz)	1077	1080	1084	1081	1087	1077
C_O (pF)	95	96	86	66	117	99
R_S (pF)	615	443	718	743	562	417

3.3.3 Determination of Driving Parameters

Since the driver is originally designed for a transducer with a much lower series resistance than the one used in this work [4], its switching resistance is much lower than the transducer's resistance ($R_{SW} << R_S$). As a result, the conduction loss is negligible according to Equation (3.22). The power consumption from the driver's circuit is assumed to be known. Also, the

Table 3.2: Characteristics of the wet transducer array with 45^o absorber

Transducer	1	2	3	4	5	6
f_S (kHz)	1054	1055	1060	1052	1056	1055
f_P (kHz)	1077	1081	1084	1081	1087	1079
C_O (pF)	95	96	86	66	117	99
R_S (pF)	615	443	718	743	562	417

switch and external capacitance are assumed to be known and are the same for all transducers. However, C_O is different for each transducer, thus:

1. The impedance in the series branch can be found using:

$$Z_S = \frac{1}{\frac{1}{Z_T} - j\omega C_O}, \tag{3.27}$$

   where Z_T is the measured transducer impedance.

2. The operating frequency will have to be in between the series resonant and anti-resonant frequencies. Therefore, for each frequency in this range, the duty cycle is numerically calculated using Equation (3.14). Then, δ can be solved using Equation (3.13). Thus, for the case when $\delta > 0$,

$$\delta = \frac{2\pi\omega C_p R_S - 1 + \cos(2\phi)}{\pi\omega C_p R_S + \frac{3}{2} + \frac{\cos(2\phi)}{2} - 2\cos\phi}. \tag{3.28}$$

   If δ is a negative number, it can be brought up to 0 by adding more C_{ext}. The value of C_{ext} can be found by solving for C_P using Equations (3.13) and (3.14) with $\delta = 0$. The optimum duty cycle vs frequency for the transducer array is shown in Figure 3.4.

3. Since the effect from switch resistance R_{SW} is neglected, the load power from Equation (3.20) is thus:

$$P_L = \frac{1}{2} R_S \left(\frac{(2-\delta)\omega C_P V}{1 - cos(\phi)} \right)^2. \tag{3.29}$$

   The switching loss is approximated from Equation (3.3), and the overall array power efficiency can be approximated by:

$$\eta = \frac{\sum_i P_{Li}}{\sum_i (P_{Li} + P_{Si} + P_{Oi})}, \tag{3.30}$$

where, P_{Oi} represents gate driver losses and the i subscript represents the transducer index. Figure 3.5 shows the average efficiency of the entire array at different driving power losses. If these losses are at 0 W, there actually is a peak efficiency at $f = 1069$ kHz. As P_O increases, the switching loss becomes insignificant, as it is only a small portion of the total power losses. With the driving losses from this driver at approximately 180 mW, along with the driving frequency at 1069 kHz, the expected performance for each driver is tabulated in Table 3.3. The efficiency for the entire array is really low due to high power losses from the driving circuit.

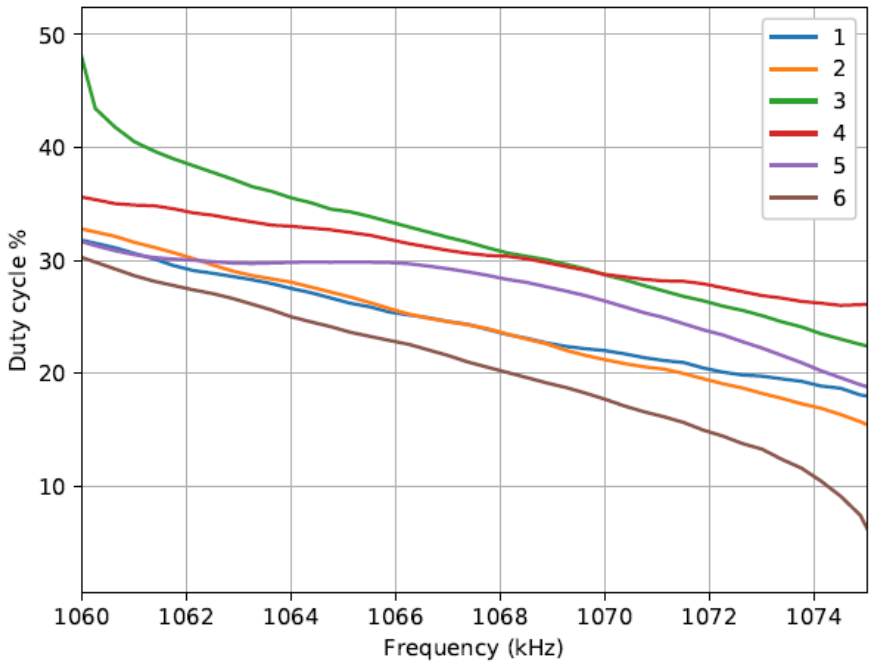

Figure 3.4: Optimum duty cycle vs frequency for the transducer array

3.3.4 Simulation and Experimental Results

The array performance is evaluated by a steady-state simulation using an in-house circuit simulator which is available at https://github.com/cechrist/cardoon. For simulations, the circuit topology is the same as shown in Figure 3.1. Transducers are modelled using the measured scattering parameters in two different modes:

1. Mode 1: the scattering parameters are only used for the fundamental frequency, for all other harmonics only the parallel capacitor of the lumped-element equivalent circuit is considered.

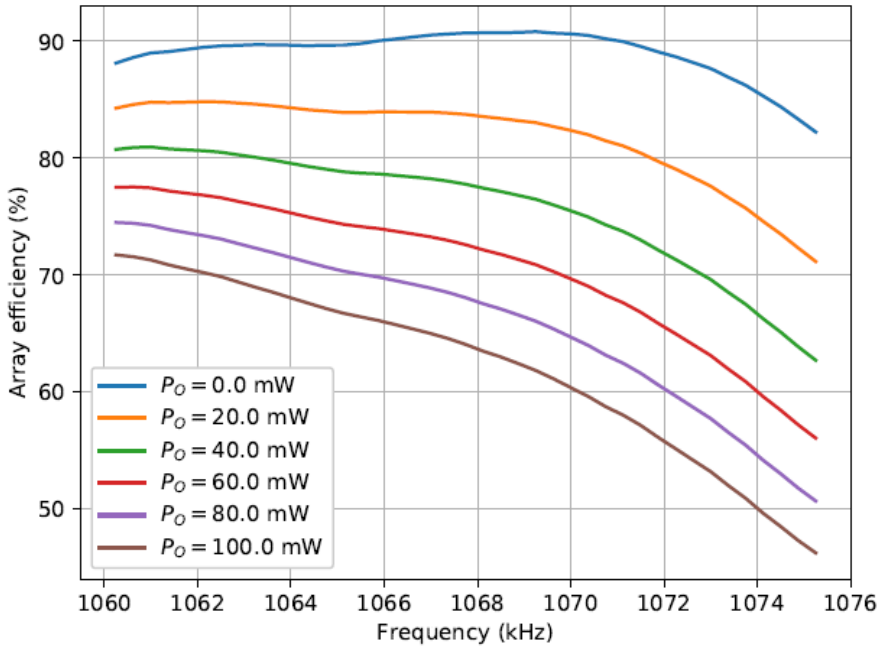

Figure 3.5: Power efficiency vs frequency for the transducer array with different driving power losses

Table 3.3: Expected result for each transducer at $f = 1069$ kHz and $P_O = 180$ mW

Transducer	1	2	3	4	5	6
$D(\%)$	22	22	30	29	27	19
δ	0.72	0.30	0.77	0.86	0.57	0.37
P_L (mW)	146	151	265	200	290	112
P_S (mW)	27	5	29	29	20	7
$\eta(\%)$	42.7	43.8	55.3	49.2	58.2	37.1

This mode removes the odd-harmonic secondary resonances from the transducer response.

2. Mode 2: measured S parameters are used up to the ninth harmonic.

There are 4 simulations performed for each transducer:

- Sim1: Perpendicular absorber, Mode 1
- Sim2: 45^o absorber, Mode 1

- Sim3: Perpendicular absorber, Mode 2
- Sim4: 45^o absorber, Mode 2

Figure 3.6 shows the output voltage and current of transducer 3 using all 4 modes. The harmonic components do have some effect on the current waveform by looking at the simulation results in Mode 3 and 4. However, this effect is small because the charge contributions of high frequency oscillations tend to compensate each other. Figure 3.7 shows the output waveforms with the harmonic components considered (Simulation mode 3) for all transducers in the array.

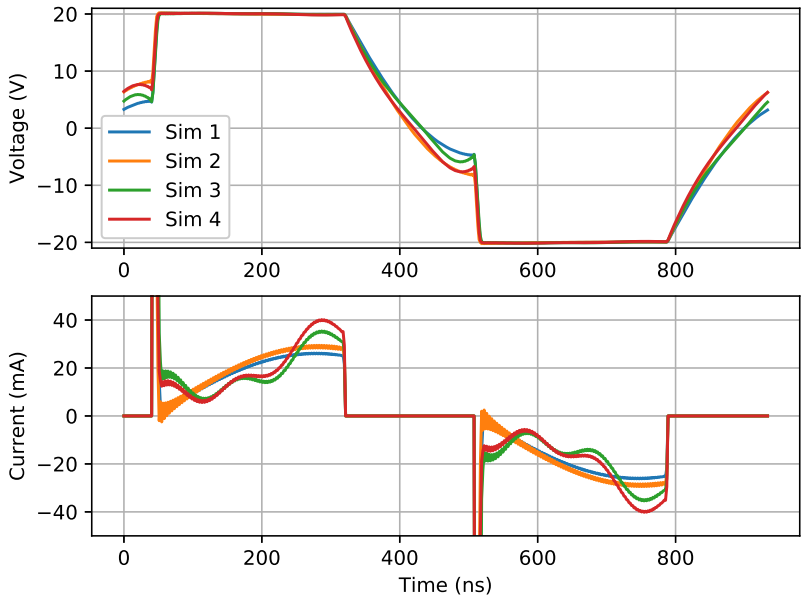

Figure 3.6: Trans 3 output voltage and current

To obtain the experimental results, the setup is as shown in Figure 3.8. The transducer is submerged into the water, while coaxial connector is held above the water surface. A short coaxial cable is used to connect the transducer and the driver. The supply voltage is initially set at 20V as seen from the power supply. However, it is measured to be 20.2V. The measured output capacitance of the driver is 26 pF. This includes the switch capacitance (C_{SW}, and also the external capacitance (C_{ext}) from the oscilloscope probe and stray capacitance from the circuit. The experimental output waveforms for the transducer array are shown in Figure 3.9. Table 3.4 and 3.5 show the calculation along with the simulation and experimental results. For

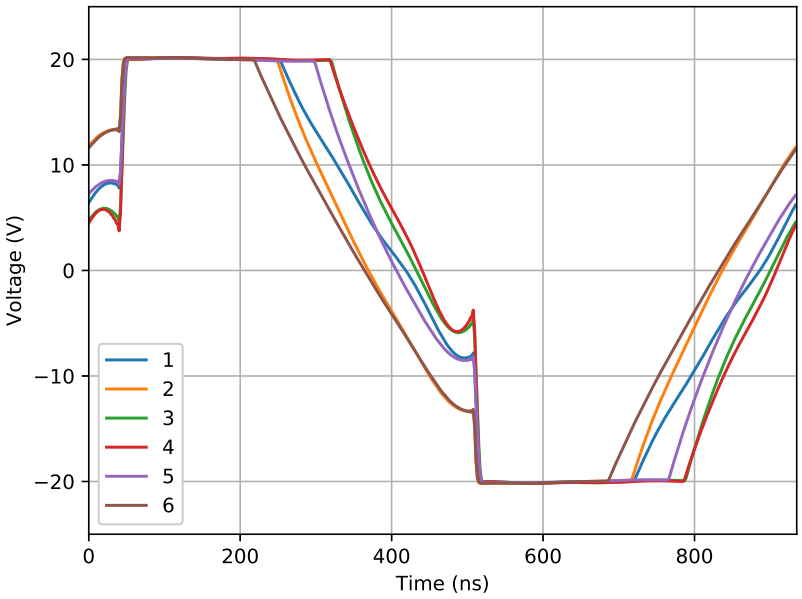

Figure 3.7: Sim 3 Output voltages

experimental results, P_L is calculated based on the measured load voltage and the measured reflection coefficient of the transducer (Γ) as follows:

$$P_L = \frac{V_o^2}{2Z_o}\frac{1-|\Gamma|^2}{|1+\Gamma|^2}, \tag{3.31}$$

where, V_o is determined using Fourier analysis of the sampled output voltage and Z_o is 50 Ω. The differences between the simulation and experimental results can be because the experiment is performed on a different day than the transducer characterization, with slightly different environmental conditions that can affect the transducer's electrical characteristics. In addition, the driver's output capacitance is non-linear, and the duty cycle cannot be programmed at its exact optimum value from Table 3.3. These 2 factors can greatly affect the measured δ as shown in Equation (3.28). However, there are some agreement between simulation 3 and the experiment to indicate that the predicted values based on the fundamental frequency response under one acoustic condition are a good approximation.

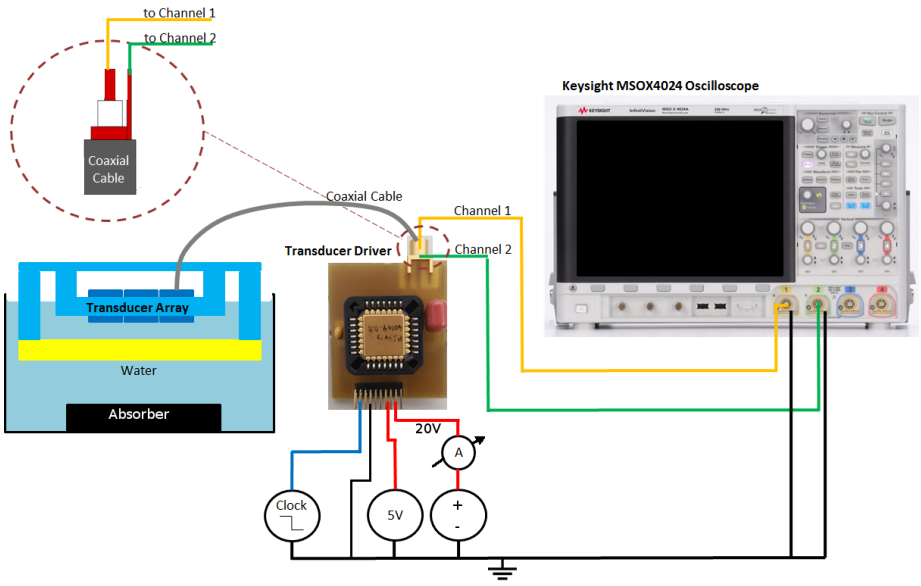

Figure 3.8: Experimental Setup

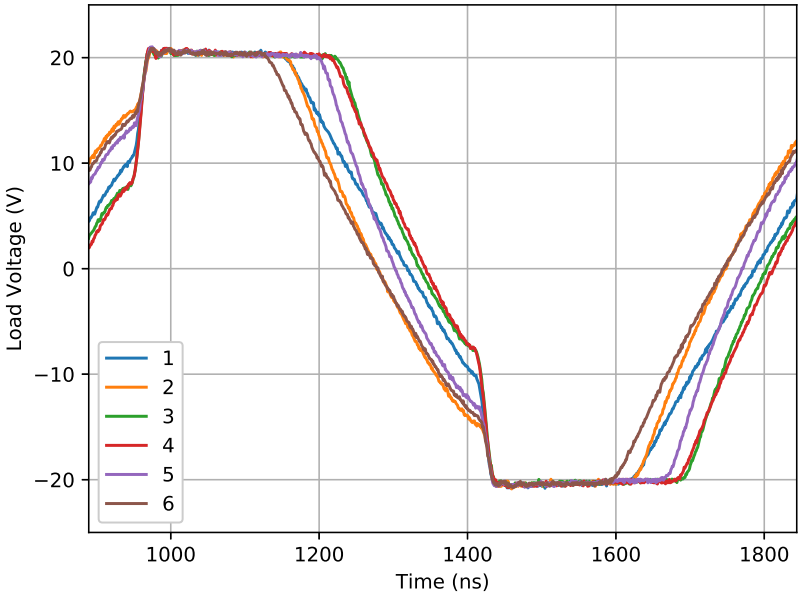

Figure 3.9: Experimental output voltage for all transducers.

Table 3.4: Simulated and experimental δ at 1069 kHz

Transducer	1	2	3	4	5	6
Theory	0.72	0.30	0.77	0.86	0.57	0.37
Simulation 1	0.72	0.31	0.77	0.86	0.57	0.37
Simulation 2	0.68	0.30	0.60	0.82	0.57	0.32
Simulation 3	0.60	0.34	0.77	0.80	0.59	0.34
Simulation 4	0.58	0.33	0.66	0.78	0.59	0.30
Experimental	0.50	0.27	0.63	0.63	0.36	0.31

Table 3.5: Simulated and experimental P_L (mW)

Transducer	1	2	3	4	5	6
Theory	146	151	265	200	290	112
Simulation 1	143	149	258	197	282	110
Simulation 2	150	158	272	200	294	114
Simulation 3	148	145	258	199	280	110
Simulation 4	155	153	269	203	292	111
Experimental	167	160	267	201	296	118

3.4 Method II - Driving Parameters for Equal Power

3.4.1 Introduction

Even though the driving method from section 3.3 provides a good approximation to determine efficient driving parameters for an entire array, it does not equalize the power delivered to each transducer. In order to electronically steer the focal zone of the transducer array, all transducers must be excited at the same power level [30]. The maximum differences between the load power must be less than 10%. Then the steering can be done by adjusting the phase of each element. This method improves the analysis of the amplifier efficiency and further develops the previously proposed method to equalize the power delivered to each transducer under the

following conditions:

- Same supply voltage for all drivers,
- Zero voltage derivative switching (ZDS) to reduce sensitivity to parameter variations, and
- Highest possible driver efficiency under the equal power constraint. This is achieved by selecting the array excitation frequency, individual duty cycles and capacitive matching networks for each transducer.

3.4.2 Transducer Characterization

The picture of the transducer array is shown in Figure 3.10. The crystal is shaped as a disc with a diameter of 20 mm and a thickness of 2.8 mm [25] Similar to the last method, the

Figure 3.10: Real-life image of the transducer array used in this work

transducers are characterized with 2 different setups. In the first setup, the absorber is placed in parallel with the transducer. Then, it is placed at a 45^o angle for the second setup. The characteristics for this set of transducers are shown in Table 3.6 and 3.7.

The transducer conversion efficiency, defined as the ratio between the acoustic power over the electrical power delivered to the transducer was also measured. The acoustic power of the transducers was measured using the radiation force method [26] with an absorber placed at the bottom of a container filled with deionized-degassed water, and the transducer suspended 2 cm away from the absorber. The container was placed on an analytical scale [27] with the transducer surface parallel to the absorber. Fig. 3.11 shows the variation of the conversion

Table 3.6: Transducer parameters with parallel absorber

Transducer	A	B	C	D	E	F
f_S (kHz)	998	1000	1002	999	1005	1003
f_P (kHz)	1106	1106	1109	1105	1114	1111
C_0 (pF)	557	545	665	619	622	521
C_S (pF)	130	125	156	145	148	121
L_S (μH)	195	203	162	175	170	208
R_S (Ω)	40	41	43	47	41	39

Table 3.7: Transducer parameters with 45° absorber

Transducer	A	B	C	D	E	F
f_S (kHz)	998	1000	1002	997	1005	1003
f_P (kHz)	1106	1106	1110	1106	1113	1111
C_0 (pF)	561	493	739	696	527	638
C_S (pF)	132	112	178	150	122	151
L_S (μH)	192	226	142	170	205	167
R_S (Ω)	40	42	43	49	42	39

efficiency with frequency for each transducer and also for the entire array under the assumption that all transducers receive the same electrical power. The efficiency peak happens between f_S and f_P at a frequency near 1040 kHz.

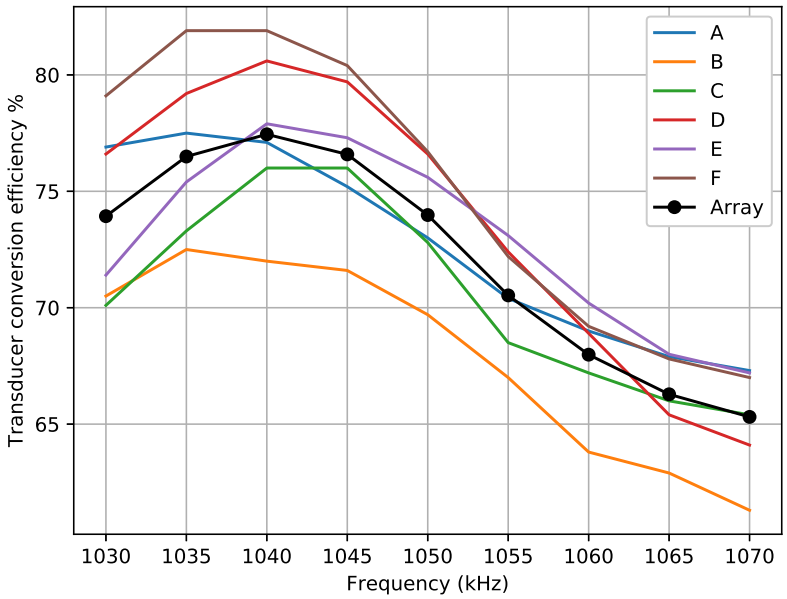

Figure 3.11: Transducer conversion efficiency as a function of frequency.

3.4.3 Determination of Driving Parameters

The objective of the method is to deliver the same power at the fundamental frequency to all transducers in the array while maximizing the combined power efficiency in the array. The proposed method thus equalizes the power delivered to each transducer while minimizing heating in driving circuits. For the following steps we assume that the switch capacitance (C_{SW}) is the same for all transducers, but C_0 may differ for each transducer.

1. Measure the transducer impedance (Z_T) of each element in the array in the frequency interval of interest.

2. Determine the parallel capacitance C_0 for each transducer. The impedance of the series resonance branch is calculated as follows:

$$Z_S = \frac{1}{\frac{1}{Z_T} - j\omega C_0}.$$

3. For (non-optimum) class DE operation, the operating frequency must be between the highest f_S and the lowest f_P for all transducers and it must be in the region where the series branch impedance is inductive. Based on these considerations, select a range for f.

4. Set $C_{ext} = 0$ for all transducers. For each frequency in the considered range, numerically obtain ϕ for each transducer using Equation (3.14) and use that value to solve for δ in Equation (3.28). If $\delta > 0$, the transducer can not be driven in ideal class DE mode and the obtained value of ϕ corresponds to the best possible efficiency in sub-optimal mode. The c Else, if $\delta < 0$, C_{ext} must be increased to make $\delta = 0$. A negative value of δ can cause the parasitic diode inside the MOSFET to conduct during its OFF state. The value of C_{ext} is obtained by setting $\delta = 0$ and numerically solving for C_p and ϕ using Equations (3.14) and (3.13). Calculate P_{L1} for each transducer using Equation (3.11).

5. Take the minimum from the set calculated load powers (P_{min}). Now increase C_{ext} in all other transducers to make all load powers equal to P_{min}. This is achieved by simultaneously solving for C_p, ϕ and δ in the system of equations formed by combining Equations (3.11), (3.14) and (3.13).

6. Estimate final array power and efficiency using Equation (3.26) and select the operating frequency.

Figure 3.12 shows the load power and total power losses vs. frequency using the two sets of transducer characterization parameters, V = 20 V, $R_{SW} = 4.6\ \Omega$, $CSW = 26$ pF and $P_G =$ 180 mW. The overall efficiency is calculated using Equation (3.26), and shown in Figure 3.13. It seems that the efficiency does not change too much with respect to frequency. However, there is a peak efficiency when $f = 1042$ kHz. Figure 3.13 also shows the combined electrical-acoustic array efficiency obtained by multiplying the load power with the corresponding transducer conversion efficiency. Since the conversion efficiencies are not always available for a particular transducer array, this method focuses on optimizing the electrical power efficiency.

The minimum Power (P_{min}) found in step 4 is bolded in Table 3.8. In this step, there is still a big variation in load power. Hence, Step 5 is necessary to bring all of the load power to be the same. Lastly, Step 6 computes the power efficiency for the entire array. The final estimated maximum difference between load powers is approximately 1%.

3.4.4 Simulations and Experimental Results

The simulations are performed in 3 different modes:

- Mode 1: the transducer scattering parameters with perpendicular absorber are used for the

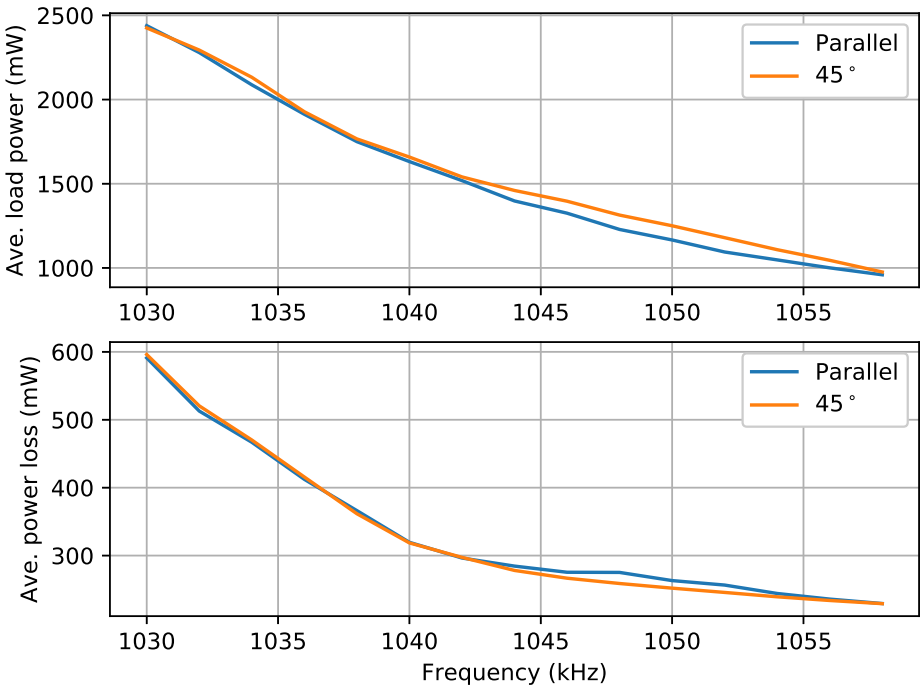

Figure 3.12: Electrical load power and losses *vs.* frequency

fundamental frequency. Secondary resonances are removed.

- Mode 2: up to ninth harmonics in the transducer frequency response are considered, and the transducer scattering parameters with perpendicular absorber are used.
- Mode 3: up to ninth harmonics in the transducer frequency response are considered, and the transducer scattering parameters with 45^o absorber are used.

Fig. 3.14 shows all transducer voltages using Mode 2. The upper graph in Figure 3.15 shows the output voltage waves for all 3 simulations with transducer D. The voltage drop (ΔV) due to R_{SW} can be observed. The lower graph shows the switch current waves along with the analytically calculated wave for the series branch current (i_s). The harmonic components clearly have some effect on the current waveform, but the harmonic oscillations tend to compensate each other out.

Tables 3.9 and 3.10 show the simulation results for P_L and δ_E respectively. Even though P_L from the simulations are smaller than expected, the most important thing is that the maximum difference for P_L is only 4% for simulation 1, 5% and 7% for simulation 2 and 3 respectively.

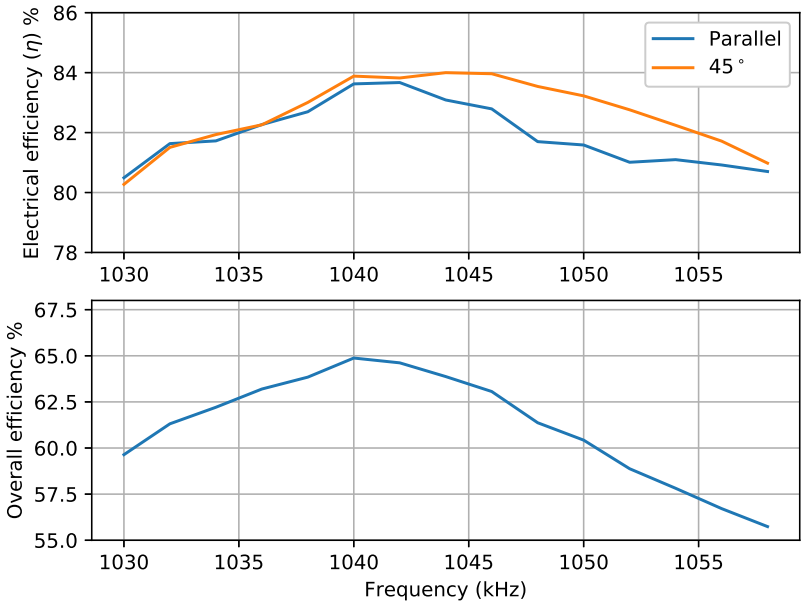

Figure 3.13: Array electrical efficiency (η) and overall combined electrical-acoustic efficiency *vs.* frequency.

Those differences are within the acceptable range. There are also some discrepancies in δ_E due to the presence of the harmonics.

The experimental setup is the same as from last method (Figure 3.8). The results are shown in Table 3.11. Again, even though measured P_L are smaller than the simulations and expected results, the maximum difference is 7%, which is in the acceptable range.

Table 3.8: Calculated parameters for each transducer at 1042 kHz section 3.4

Step	Transducer	A	B	C	D	E	F
4	P_{L1} (mW)	1910	1636	2067	**1626**	2171	1886
5	D (%)	24	26	21	25	20	23
	C_{ext} (pF)	561	305	803	284	1021	694
	δ	0.29	0.01	0.37	0.00	0.42	0.24
	P_{L1} (mW)	1626	1626	1626	1626	1626	1626
6	δ_E	0.31	0.05	0.39	0.04	0.45	0.27
	P_L (mW)	1522	1515	1521	1513	1523	1518
	L (mW)	286	253	332	255	371	281
	η_D (%)	84	86	82	86	80	84

3.5 Discussion

This chapter has covered 2 different strategies to drive ultrasound transducer arrays. Both methods are capable to determine capacitive matching networks and driving parameters for an ultrasound transducer array operating the drivers in sub-optimal class DE condition. However, Method II expands the work further by equalizing the output power across the entire transducer array. The results from both methods show that the array should be excited not at the transducer series resonance frequency but rather at an intermediate frequency between the series and parallel

Table 3.9: Simulated output power for each transducer

Transducer	A	B	C	D	E	F
Predicted (mW)	1522	1515	1521	1513	1523	1518
Simulation 1 (mW)	1480	1469	1435	1493	1437	1475
Simulation 2 (mW)	1470	1398	1452	1410	1462	1459
Simulation 3 (mW)	1468	1400	1466	1509	1463	1464

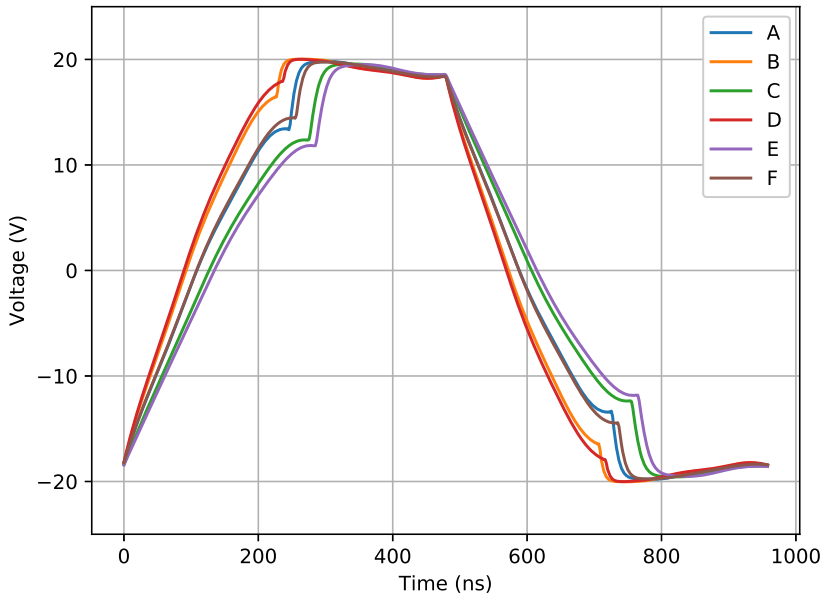

Figure 3.14: Output voltage for all transducers using the accurate transducer model (Sim 2).

Table 3.10: Simulated δ_E for each transducer

Transducer	A	B	C	D	E	F
Predicted	0.31	0.05	0.39	0.04	0.45	0.27
Simulation 1	0.33	0.09	0.41	0.04	0.45	0.28
Simulation 2	0.34	0.18	0.38	0.11	0.41	0.28
Simulation 3	0.34	0.18	0.39	0.17	0.41	0.28

resonances. This frequency is also close to the peak conversion efficiency of the transducer. In a production system the transducers in the array should be made as similar as possible to minimize the mismatches in electrical characteristics and conversion efficiency. Method II would then be used to compensate these mismatches.

In addition, by analyzing and observing the simulation results from the 2 driving methods, the following conclusion can be made:

- The driver design [4] does not supply enough power to the smaller transducers used in

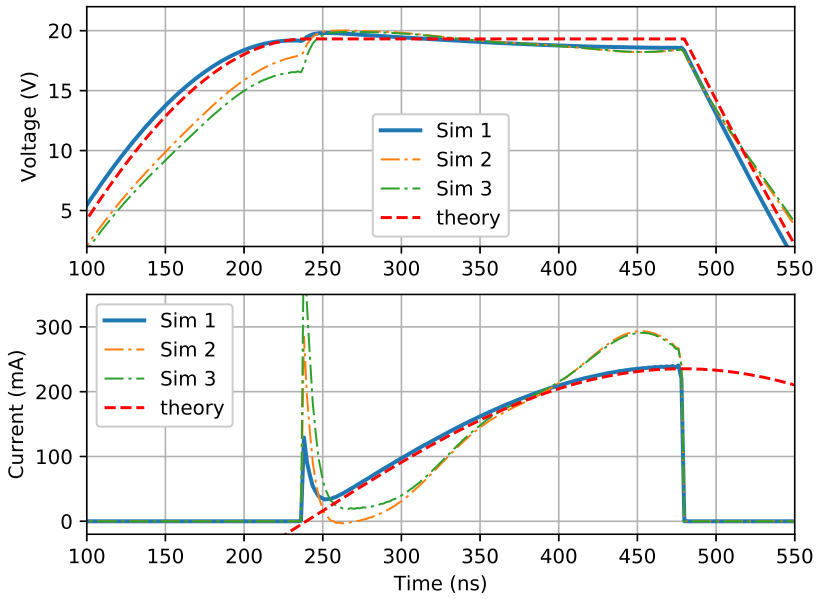

Figure 3.15: Output voltage and current waveforms for Transducer D.

Table 3.11: Summary of experimental results

Transducer	A	B	C	D	E	F
D (%)	23.8	26.0	20.8	24.8	19.6	23.0
C_{ext} (pF)	527	328	838	273	953	704
δ_E	0.35	0.26	0.41	0.21	0.42	0.32
P_L (mW)	1412	1336	1380	1322	1398	1346
P_{DC} (mW)	1710	1660	1742	1758	1830	1740
L (mW)	298	324	362	436	432	394
η_D (%)	83	80	79	75	76	77
P_L/P_3 (dB)	32	26	32	25	31	32

Method I. The average output power is only 194 mW. As a result, the first objective for this research is to increase the average load power.

- The results from method I show that the switching loss due to sub-optimal class DE condition is only a small fraction of the total power losses. The reason for this is because the gate driver loss from Song's design [4] is too high compared to the power delivered to the load. As a result, the proposed driving methods to minimize the switching losses are not effective. Therefore, one important objective for the new design is to propose a low power-consumption driving circuit.

- The power efficiency while driving the smaller transducer array is very low. This problem can also be fixed by choosing the appropriate MOSFET sizes to find a balance between power loss from switch resistance, and gate-driving circuit losses.

Chapter 4

Proposed Driver Design

4.1 Introduction

The case studies presented in Chapter 3 demonstrate that the driver must be designed considering the transducer impedance if high efficiency is desired. The main objectives of the new transducer driver are:

- Design a digital logic unit that allows 360^o phase delay, and features 1% duty cycle resolution.
- Achieve the best-possible power efficiency by maximizing the output power while keeping the power consumption at minimum.
- Propose a high efficiency driving circuit, that consumes much less power than [4].
- Determine the optimum switching MOSFET sizes to achieve the best-possible power efficiency.
- The design must operate below the breakdown voltage of the device used (NMOS50H).

In this chapter, section 4.2 provides an overview of the proposed driver. Sections 4.3 and 4.4 go further into the function and design analysis of each component in the driver. Then, section 4.6 discusses a methodology for optimum MOSFET switch sizing. At the end of this chapter, the performance the proposed design will be compared with the design from [4] to see the improvement.

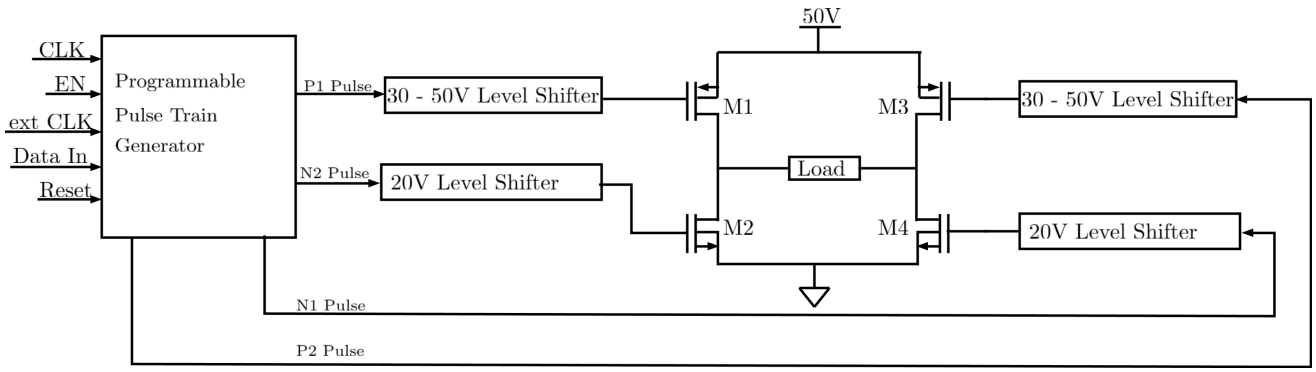

Figure 4.1: Proposed transducer driver

4.2 System Overview

The proposed system consists of a full-bridge configured class DE amplifier. To increase the output power at the load, the voltage supply is increased to the drain-to-source nominal voltage that the technology can handle. The driver will be implemented using AMS AG H35 CMOS process. The maximum drain-to-source and gate-to-source break down voltage is 50 V and 20 V respectively. As a result, the gate voltage at M1 and M3 must be a 30-50 V pulse; and 0-20 V pulse signal is required at the gate of M2 and M4.

The programmable pulse train generator is responsible to generate the pulse signals to drive the amplifier at a desired frequency and duty cycle. The design of this part will be discussed in Section 4.3. The output is a 0-5 V pulse going through the level shifters to drive the switching MOSFETs (M1-4). Since the driver is designed for the transducer array used in sections 3.3 and 3.4, the target operating frequency is around 1 MHz. Also, to implement those 2 drive methods, the target phase and duty cycle resolution is 1%.

4.3 Programmable Pulse Train Generator

The proposed digital logic unit is as shown in Figure 4.2, which consists of 2 counters, a 20-bits register, 3 comparators, and a pulse train generator block. In the 20-bits register, the first 7 bits are used for frequency divider; the next 7 bits are for phase delay, and the last 6 bits are reserved for duty cycle. In order to obtain the 1% duty cycle resolution, the clock frequency must be 100 times more than the frequency of the output pulse signal. Hence, 7 bits are needed to ensure the frequency divider can be programmed up to 100. Next, the same amount of memory (7 bits) is needed to achieve 360^o phase shift. Since the duty cycle must not exceed 50%, only

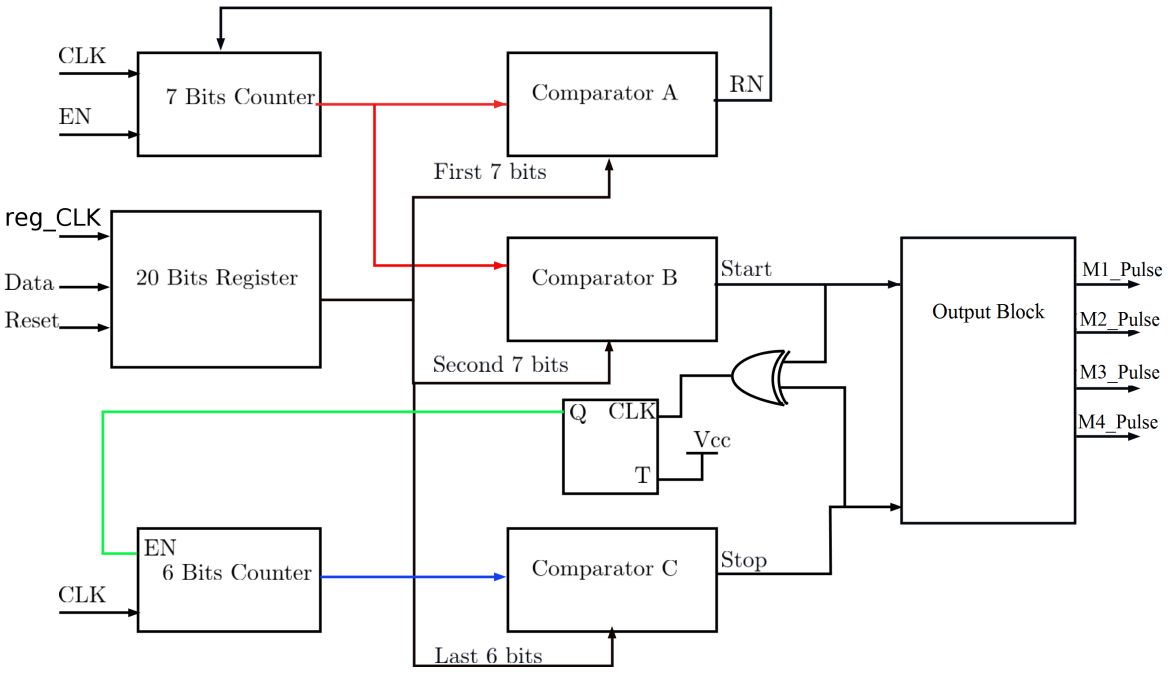

Figure 4.2: Block Diagram of the proposed Pulse Train Generator

6 bits are required for this feature. The register requires an external clock signal (reg_CLK), register Data (reg_Data), and an initial reset pulse signal to setup the frequency divider, phase shift, and the duty cycle for the pulse train generator. During the normal operation, the required inputs are an external clock signal (CLK) and an enable signal (EN). This design can output 4 pulse signals to the PMOS and NMOS of the full-bridge class DE amplifier.

4.3.1 Counters

There are 2 counters used in this design; one is 7-bits, and the other is 6-bits. The structure of the counter is shown in Figure 4.3. The 7-bit counter consists of 7 positive-edge trigger T flip-flops and AND gates. This synchronous design allows the counter to work at a higher frequency [8]. The 7-bits counter has two main functions, frequency divider and phase shift control. The 6-bits counter is used to control the duty cycle of the pulse. The EN pin is connected to T input of the flip-flop, so that the output Q will toggle at every clock cycle. The RN pin is the output of the Comparator A, which will reset outputs of this counter when it is set to logic '0'. All outputs of the 7-bits counter are connected to the inputs of the Comparator A and B; whereas all outputs of the 6-bits counter are connected to the inputs of the Comparator C.

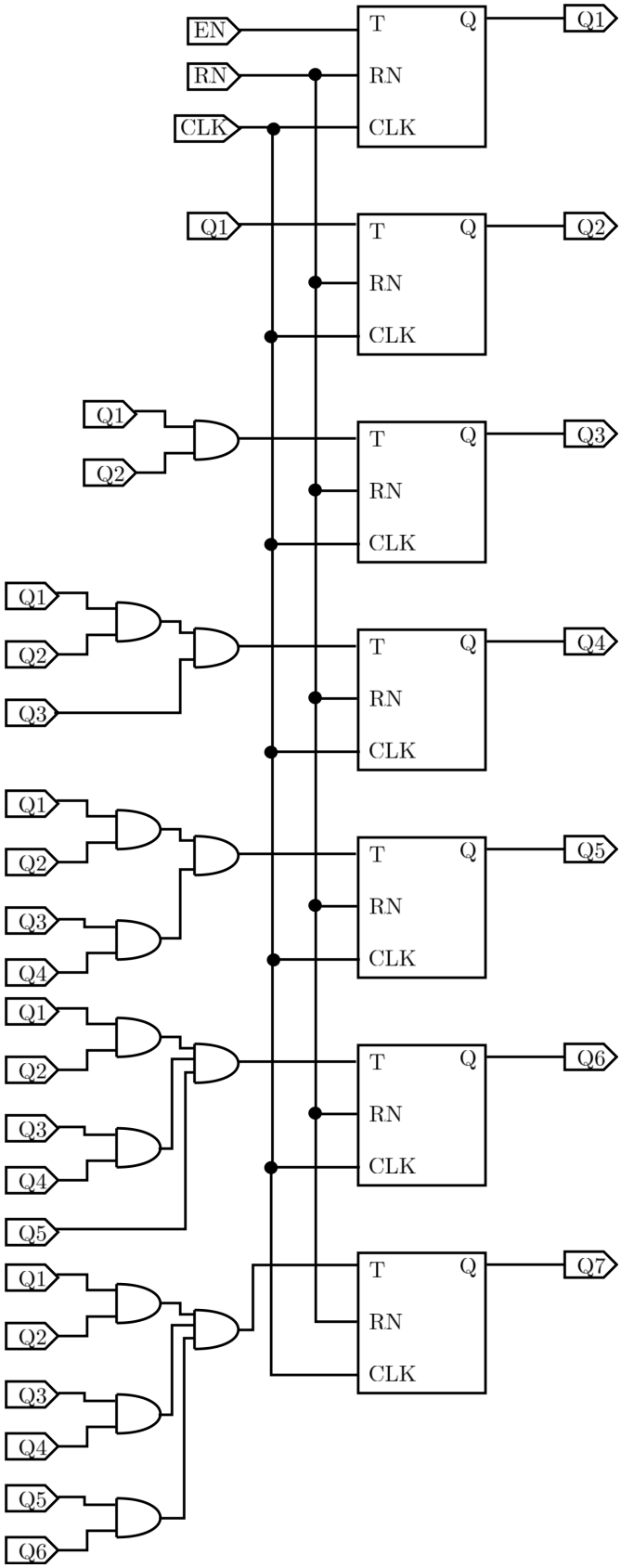

Figure 4.3: Schematic of the 7-bits counter

4.3.2 20-bits Register

The structure of the 20-bits register is shown in Figure 4.4. D flip-flops are used to consume less die area. This design uses the conventional Serial-In to Parallel-Out shift register to move data from Reg_Data input to each output of the flip-flops [4]. At the beginning of the data-transfer, there will be a pulse sent to Reset pin to reset all outputs of the flip-flops. Then, data will be shifted into the register after every positive-edge Reg_CLK signal. The register only has the capability to hold 20 bits, because that is all it needs to achieve the target phase and duty cycle resolution. The first 7 bits of the register (Q1 to Q7) are needed for the frequency divider. The next 7 bits (Q8 to Q14) contain the phase shift information. The last 6 bits (Q15 to Q20) are used to set the duty cycle of the output pulse.

4.3.3 Comparators

The structure of the 7-bits comparator is shown in Figure 4.5. It consists of 7 XOR-logic gate in the first stage, and several OR-logic gates. The inputs of the comparator are the outputs from the counter and the register. When the outputs of the counter (Q1 to Q7) match with the data from the register (R1 and R7), there will be a negative pulse at the output of the Comparator A. The output of the Comparator A is used to reset the first counter. The output of the first counter is also compared with the phase shift information stored in the register (R8 to R14) at Comparator B. The output of this Comparator B is sent to the pulse train generator to start turning on the selected MOSFET switches. Comparator C compares the outputs from the second counter with the duty cycle information to turn OFF the MOSFET switches.

4.3.4 Output Block

The schematic of the Pulse Train Generator is shown in Figure 4.6. It consists of two T flip-flops and a few different logic gates. Initially, both flip-flops are reset by applying a negative pulse to the RN inputs, so their output Qs are at logic '0', and $\overline{Q}$s are at logic '1'. This initial state will ensure that all switches are turned OFF. When the system is enabled, and a negative START pulse is applied at the input of the NAND gate, the clock state of the bottom flip-flop is changed, so the output will toggle. Hence, the outputs P1_Pulse changes to logic '0', and N2_Pulse switches to logic '1', which will turn ON the MOSFET M1 and M4 in Figure 4.1. When a negative STOP pulse is applied, the outputs in both flip-flops will toggle, so P1_Pulse and N2_Pulse will change back to their initial state (logic '1' and '0' respectively). In addition,

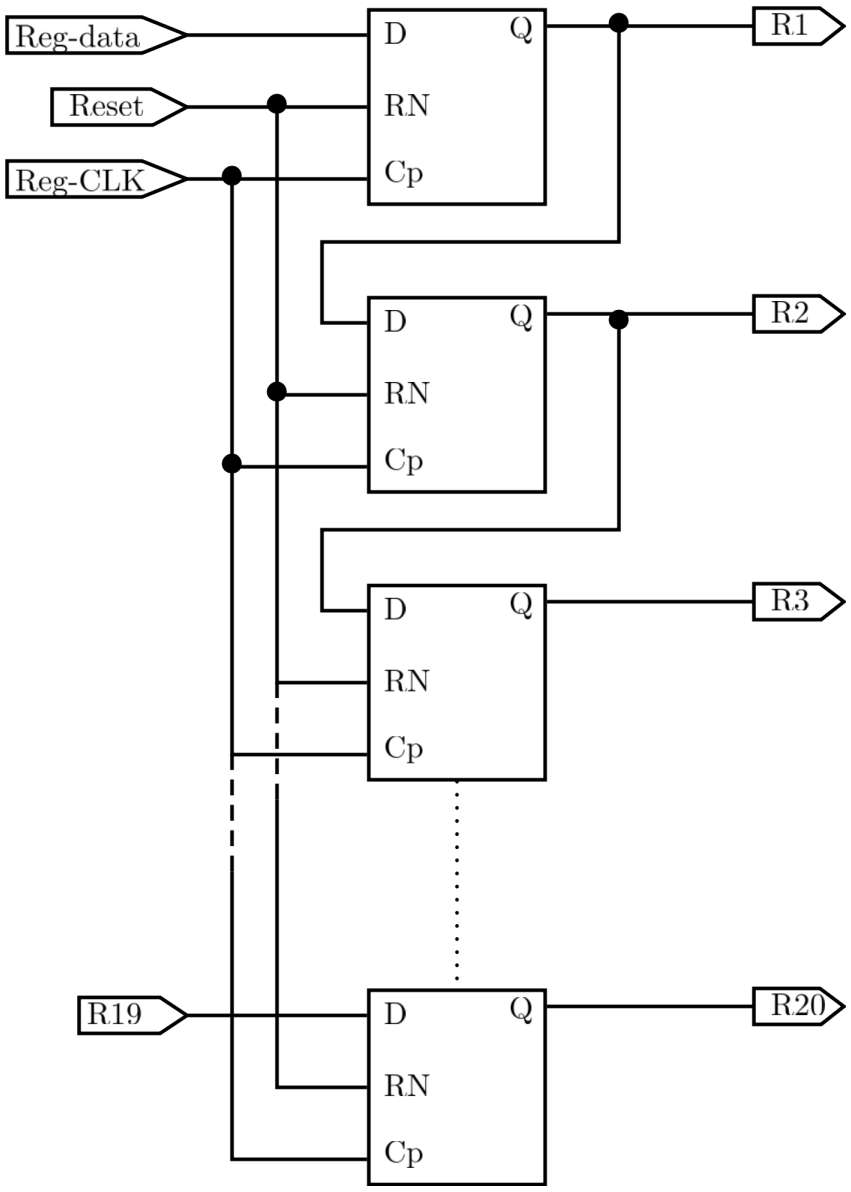

Figure 4.4: Schematic of the 20-bits Register

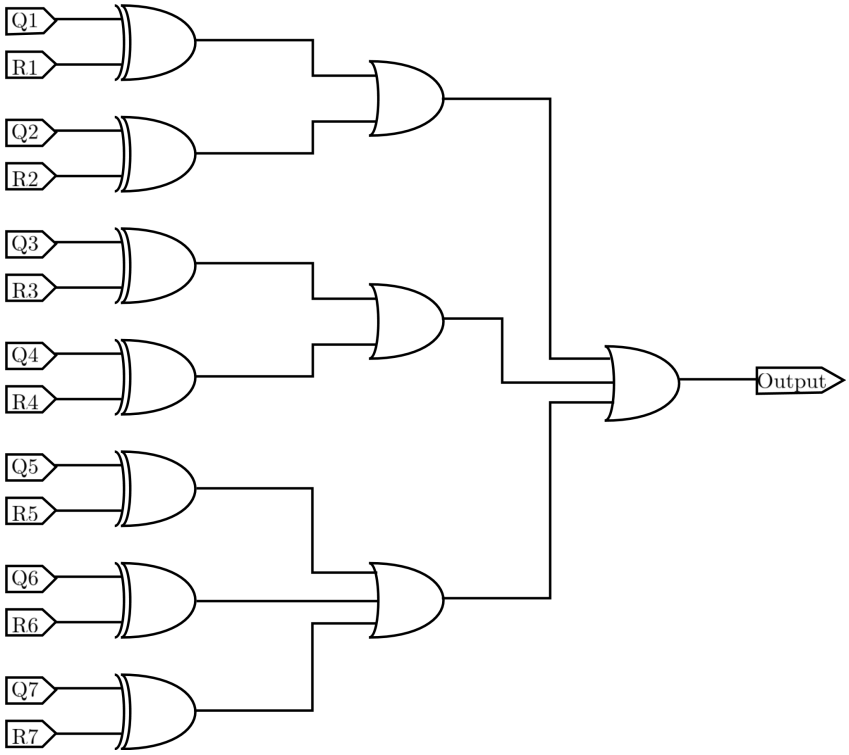

Figure 4.5: Schematic of the 7-bits Comparator

a negative STOP pulse will toggle the output of the top flip-flop, which means that the next START pulse signal will change the output state of P2_Pulse and N1_Pulse instead. By using this method, the MOSFET pairs M1-M4 and M2-M3 from Figure 4.1 will not be turned ON at the same time.

4.3.5 Outputs of the DLU

Frequency Divider

The first function of the DLU is to divide the incoming frequency from external clock signal. To achieve a resolution of 1% duty cycle per bit, the frequency divider is set to 100. In order to do such task, the number stored in the register must be set as half of the divider in decimal. The reason for this is because the system must send pulse signals to the amplifier at every half-period. As a result, with 7 bits reserved for this function, the system is capable of dividing the incoming frequency by a factor of 255. When the system is enabled, the output of the first counter will be compared with the first 7 bits of the register. When these 2 outputs match, there will be a pulse RN sent to reset the counter. Looking at Figure 4.7, the incoming clock signal is at 100 MHz,

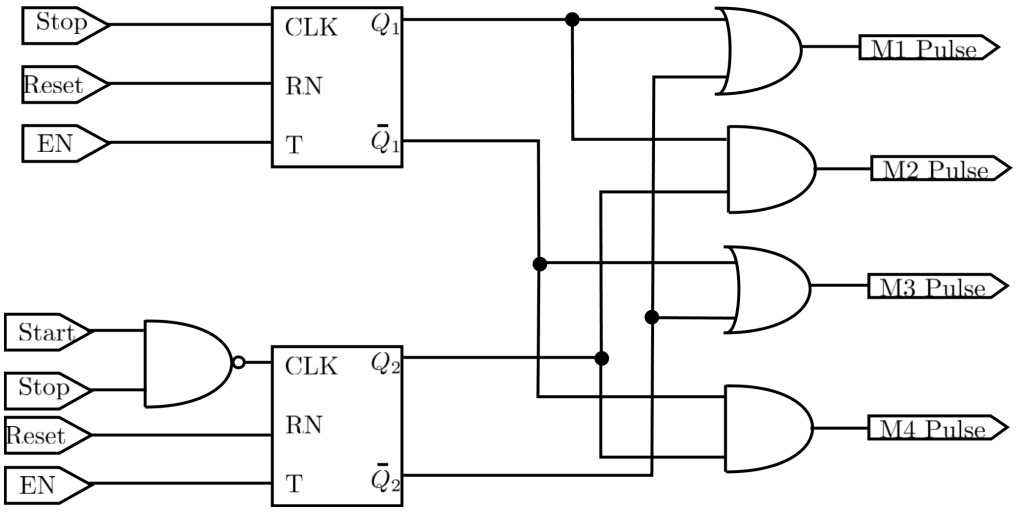

Figure 4.6: Schematic of the Output Block

as the frequency divider is set at 100 by storing 50 decimal in the first 7 bits in the register. As a result, RN pulse occurs at every 0.5 μs. The delay at the beginning is the set-up time to program the 20-bits register. Figure 4.8 shows the zoomed view of the RN pulse, which happens in less than 10 ns.

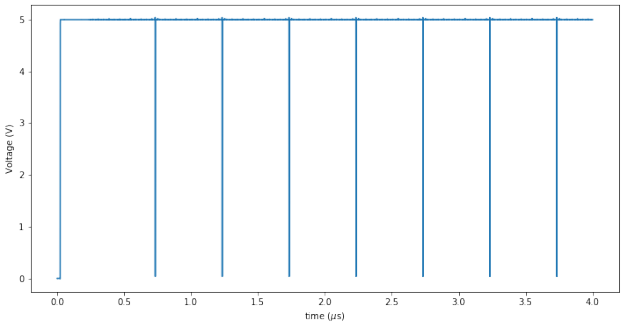

Figure 4.7: RN pulse for frequency divider

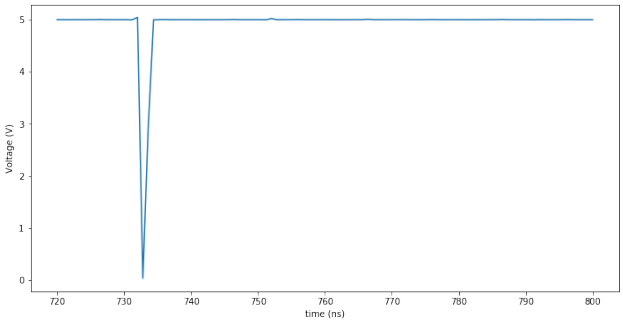

Figure 4.8: Zoomed view of RN pulse

Pulse Signal control

Initially, the 6-bits counter is disabled. As mentioned in section 4.3.3, when the outputs of the first counters match with the phase shift information stored in the register (R8 to R14), the Comparator B will send a negative START pulse signal to the Output Block. This signal triggers a positive-edged clock event to toggle either M1_Pulse and M4_Pulse or M3_Pulse and

M2_Pulse (As explained in section 4.3.4. Also, the START pulse signal will enable the 6-bits counter by introducing a positive-edged clock event at the T-flipflop in Figure 4.2. As this 6-bits counter counts up to the value of the duty cycle information stored in the register (R15 to R20), Comparator C will send a negative STOP pulse signal to the Output Block to turn OFF all of the MOSFETs. This STOP signal is also fed back to the T-flipflop in Figure 4.2 to disable the 6-bits counter.

Since the system must be able to adjust the phase shift to any time during the period, there must be 7 bits reserved for this information (same as frequency divider). However, the duty cycle information must never exceed 50% of the the period, so it only requires 6 bits to store the information.

Simulation Results

The simulation setup is just as shown in the block diagram 4.2. In order to drive the amplifier at 1MHz, the frequency divider must be set to 50. The next 7 bits are the phase shift, which is set at 42 (0.42T = 420 ns delay). The last 6 bits are used for duty cycle control, which is set at 25 for 25% as shown in Figure 4.9. Figure 4.10 shows the simulation results when programming the DLU to generate a pulse at 1MHz, 420 ns phase shift, and 25% duty cycle. Figure 4.11 shows the START and STOP pulses to generate the appropriate signals to drive the amplifier. The total power consumption for this DLU system is found to be 3 mW.

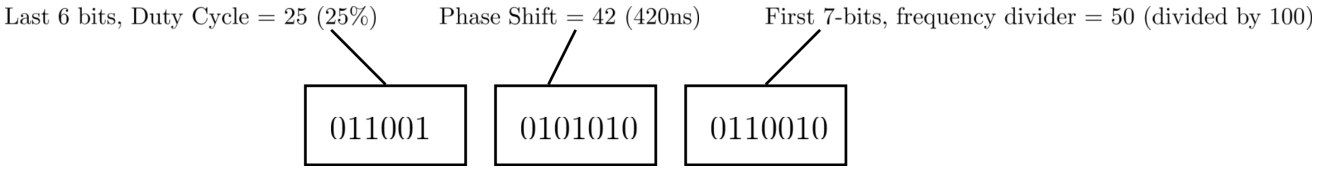

Figure 4.9: Data In Configuration

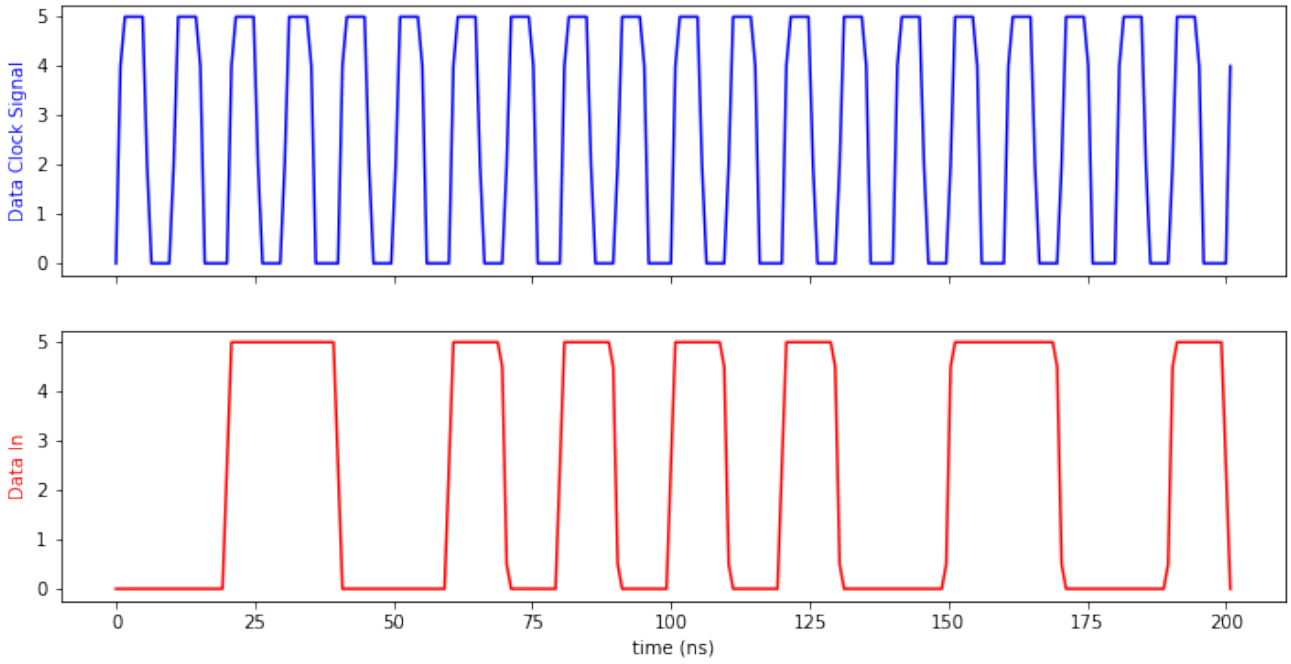

Figure 4.10: Simulation results for programming the DLU system

4.4 30-50V Level Shifter

This section will discuss 2 level shifters designs. The first one will try the same level shifter design used in [3] and [4], which consumes 33 mW to shift the voltage level from 5 V_{pp} to 20 V_{pp}. However, when the design used to convert the signal to 50 V_{pp}, it suffers a much higher losses due to the static current from the current source. As a result, a different design without the current source must be used. The end of this section will discuss the new level shifter design that only consumes 9.4 mW to convert the driving signal from 0-5 V pulse to 30-50 V pulse.

Conventional Level Shifter

The conventional level shifter is designed as shown in Figure 4.12. In order to drive the PMOS M1 and M3, the voltage swing at point A must be from 30-50 V. When the input voltage (In) is 5 V, M5, M7 and M9 are turned ON while M6 is OFF, so the voltage at point A is 50V. When the input voltage is 0 V, M6 and M10 are turned ON and act as a voltage divider circuit. The voltage at point A is now 30V. Since the NMOS M6, and PMOS M10 act like a voltage divider circuit, no external 30 V voltage supply is required. However, if this design is used to drive the

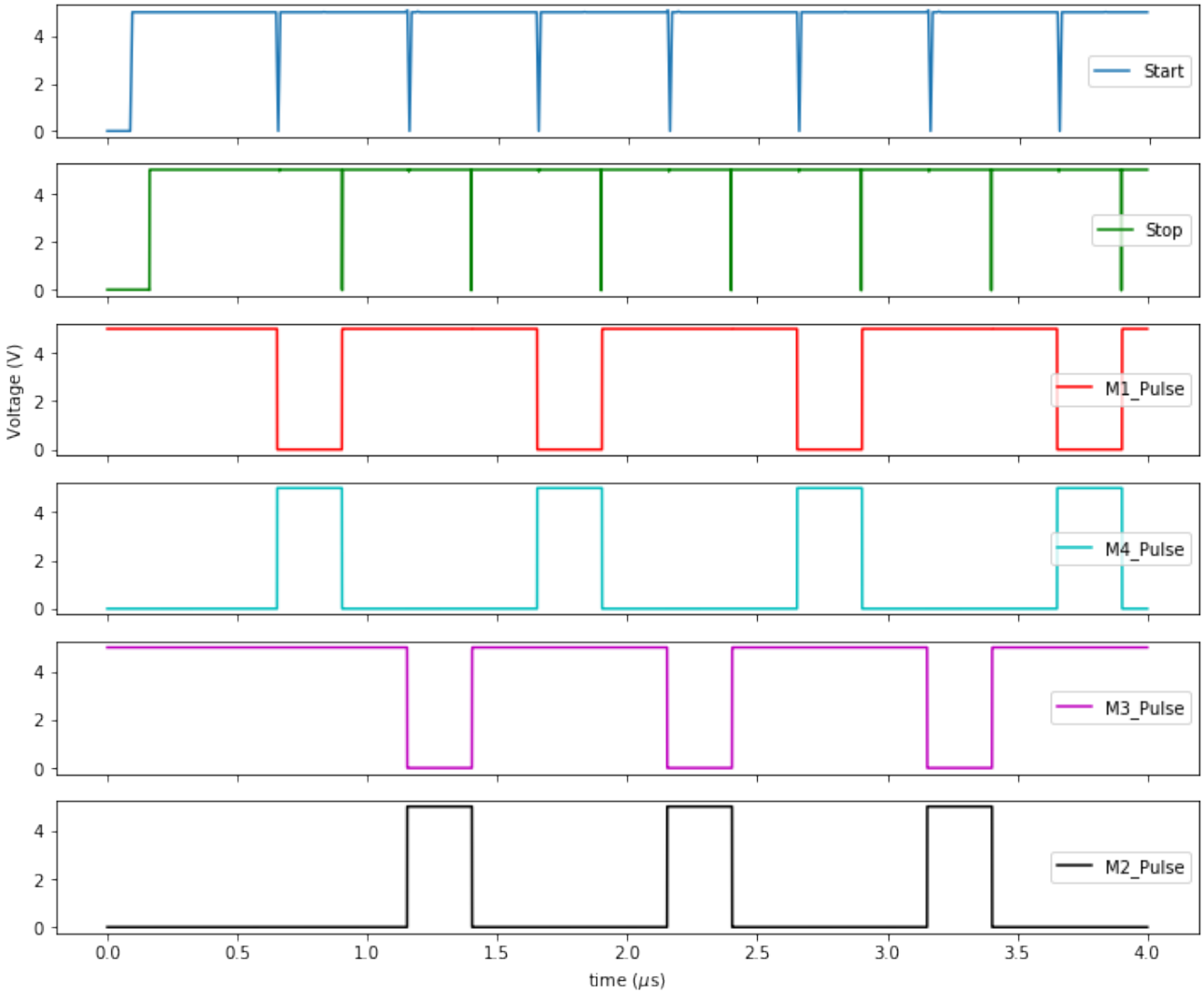

Figure 4.11: Outputs of the Pulse Train Generator

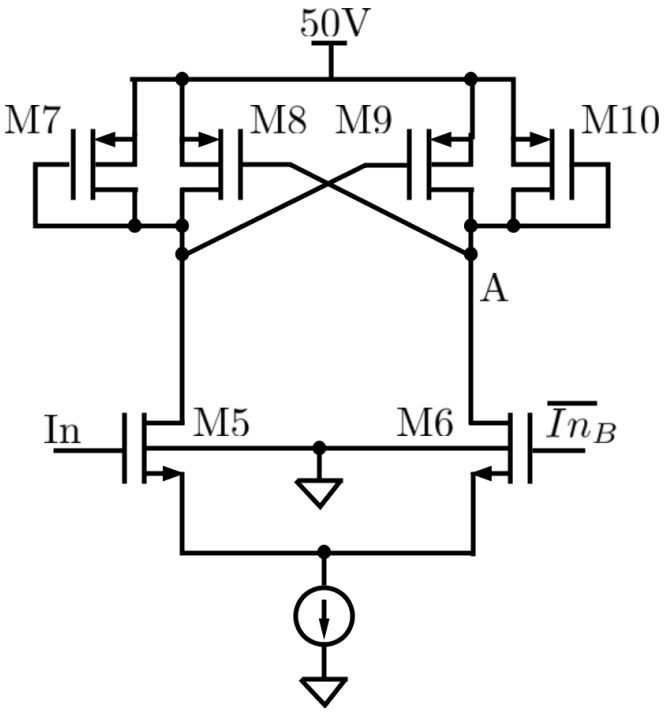

Figure 4.12: Schematic of a conventional level shifter

PMOS directly, the current source must be adjusted, so that the rise time is below 2% of the pulse width. 2% rise time is set to ensure that it does not affect the pulse signal at the output. Higher rise time will reduce the conduction time of the MOSFET switches, and thus the output waveform is not as expected.

The output at point A is connected to the PMOS M1 or M3 from Figure 4.1. Therefore, the total capacitance at this point is:

$$C_A = C_{gate_{M1}} + C_{gate_{M10}} + C_{gate_{M8}} + C_{drain_{M9}} + C_{drain_{M10}} + C_{drain_{M6}}. \tag{4.1}$$

Supposed the total capacitance at A is 14 pF. If the pulse is set at 1 MHz frequency, 25% duty cycle, and 20 V peak-to-peak, its $2\%t_{on}$ rise time is equivalent to:

$$\Delta_{ta} = D \cdot \frac{1}{f} \cdot 2\%t_{on} = 0.25 \cdot \frac{1}{1MHz} \cdot 0.02 = 5ns. \tag{4.2}$$

Its slew rate (SR) will be:

$$SR = \frac{V_{pp}}{\Delta_{tA}} = \frac{20V}{5ns} = 4000V/\mu s. \tag{4.3}$$

In order to achieve such slew rate, the current source must be set at:

$$i_D = SR \cdot C_A = 4000V/\mu s \cdot 14pF = 56mA. \tag{4.4}$$

Since the Vdd is connected to 50 V, the power consumption from this circuit alone is already at 2.8 W, which is a lot higher than the load power. Therefore, this circuit is not designed to drive a large capacitive load. Figure 4.13 shows a level shifter design with an extra voltage supply (30 V), and a couple inverters connected to drive the gate capacitance of the PMOS M1. To reduce the amount of power loss, the current source in this circuit must be minimized, while keeping the rise/fall time of the voltage at point A under 5 ns. A series of inverters is used to drive larger capacitive loads. Since various substrates are biased, a triple-well technology should be exploited. The total capacitance at point A is estimated to be equal to 1.25 pF. Using similar

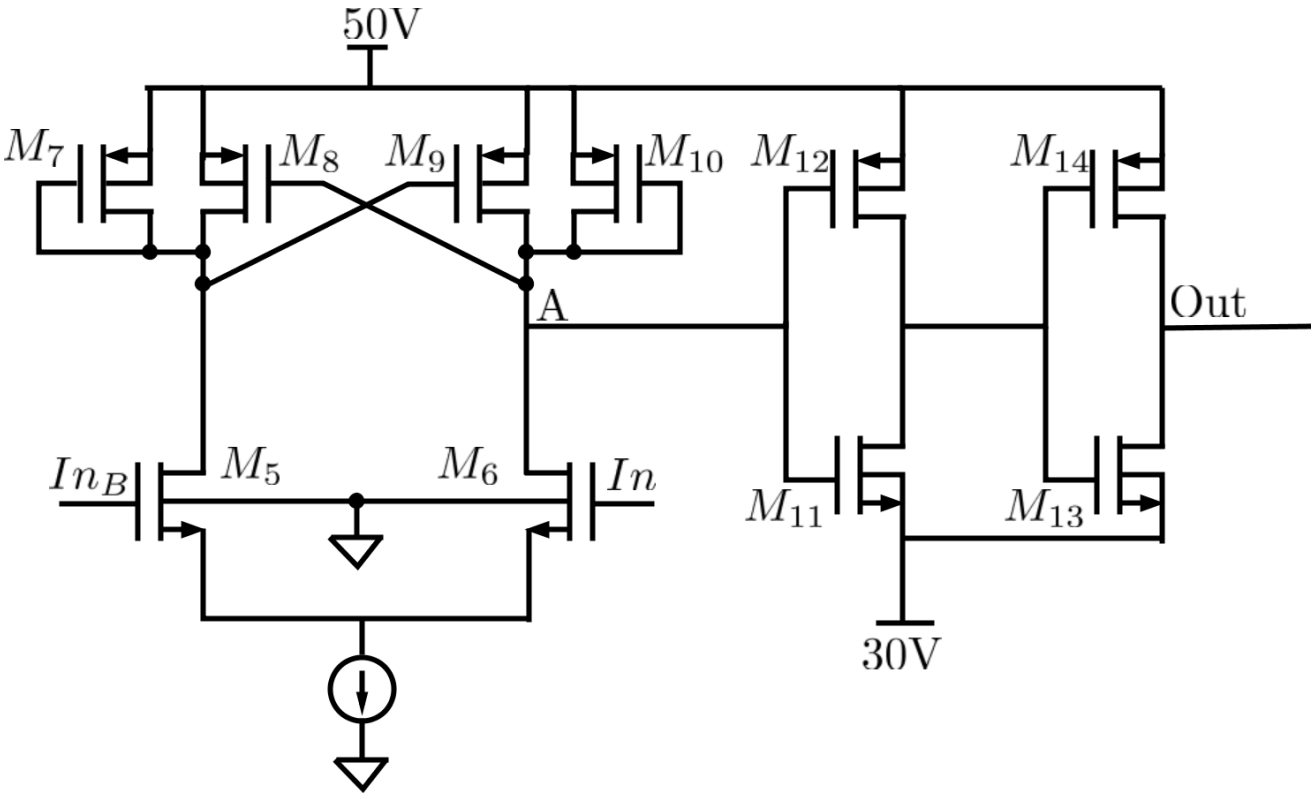

Figure 4.13: Level Shifter used in [3] and [4]

approach, the required current source can be calculated:

$$i_D = -SR \cdot C_A = 4000V/\mu s \cdot 1.25pF = 1.25mA.$$

Since the current source is set at $1.25mA$ and there are 2 of these circuits to drive the PMOS M1 and M3, the total power loss due to these level shifters is found to be:

$$P_{loss} = 2 \cdot 50V \cdot 1.25mA = 125mW. \tag{4.5}$$

Even though the power consumption in this circuit is reduced significantly, there is still not much improvement from [4]. Hence, there is a need for a new design that consume much less power to improve power efficiency.

Level Shifter without current source

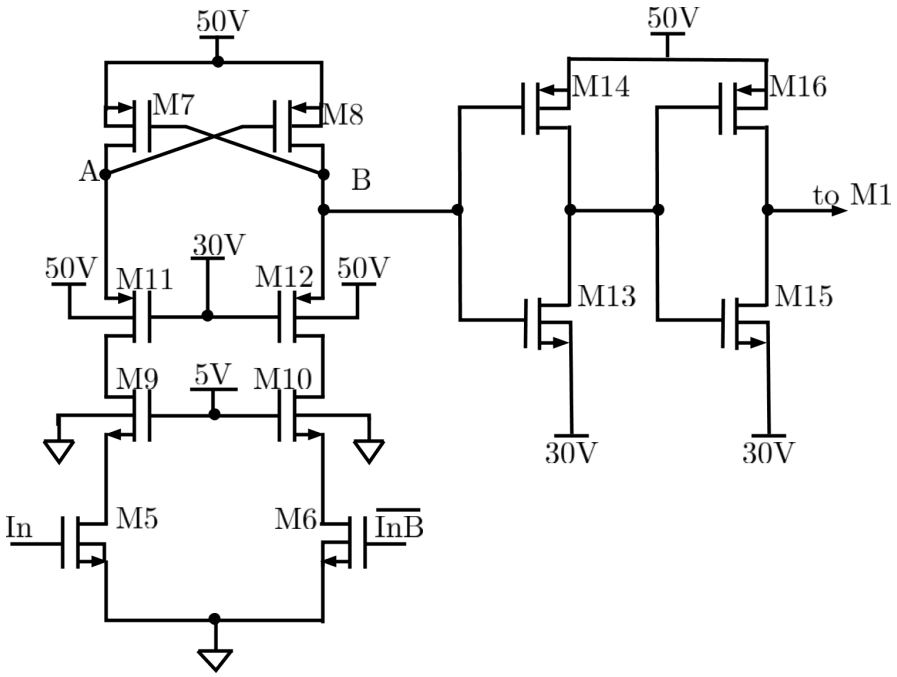

Figure 4.14: Schematic diagram for the 30-50 V level shifter

The level shifter proposed is similar to the negative level shifter design from [28]. The structure of this level shifter is as shown in Figure 4.14, and it is used to drive the PMOS M1 and M3 in Figure 4.1. There are 2 stages in this design. The first stage produces an output voltage swing from 30 V to 50 V, and the second stage is composed of a series of inverters to drive larger capacitive loads. In this design, since M5 and M6 are not exposed to 50V drain-to-source voltage, a low voltage MOSFET can be used (NMOS20H is used, which can sustain 20V across its drain and source). Other transistors in this design are NMOS50H and PMOS50H in this technology, which can sustain 50V from drain to source. The extracted parameters for these devices are shown in Table 7.1.

When the input voltage is 5 V, M6 and M10 are cut off, whereas M5 and M9 are forward biased. At this state, the voltage at the drain of M9 should be 0 V. As a result, transistor M8

and M11 are also forward biased. The gate-to-source voltage at M8 should be equal to 50 V - (30 V + $|V_{tp}|$), which is below the technology break-down voltage. The voltage at the drain of M8 is approximately 50V, so M7 is cut off, but M12 stays ON. Therefore, the voltage at point B should be 50 V.

In the another case, when input voltage is 0 V, M5 and M9 are cut off, whereas M6 and M10 are ON. The voltage at the drain of M10 is 0 V, and causes M7 and M12 to turn ON. As a result, the voltage at point A is 50 V, and turn OFF M8. The voltage at point B would be approximately 30 V+$|V_{tp}|$.

Transistor M9 and M10 are biased at 5 V to protect transistor M5 and M6 by reducing the drain-to-source voltage from 50 V to $50V - V_{tn}$). M11 and M12 are used to reduce the gate-to-source voltage at M7 and M8 from 50 V to 50 V-(30V+$|V_{tp}|$).

During the 50 V to 30 V transition at point B, the voltage at the drain of M10 must be approximately 0 V, which means transistors M6 and M10 must be much bigger than M12, so that most of the voltage drop will be across the drain-to-source of M12. The estimated capacitance at node B is 0.5 pF. For 1 MHz, 25% duty ratio, 20 V peak-to-peak pulse with a rise time Δt_B is set to 2% of the signal period, gives:

$$\Delta t_B = \frac{0.02 \cdot 0.25}{1MHz} = 5ns. \tag{4.6}$$

The on-resistance of M8 must be within:

$$2.2 \cdot R_{ON_{M8}} \cdot 0.5pF < 5ns,$$
$$R_{ON_{M8}} < \tfrac{5ns}{2.2 \cdot 0.5pF}.$$

The on-resistance of a M8 can be estimated by:

$$R_{ON_{M8}} = \left(\frac{L}{W}\right)_{M8} \frac{1 + \theta_{P1}(V_{G_{M8}} - |V_{tp}|) + \theta_{P2}(V_{G_{M8}} - |V_{tp}|)^2}{0.5K'_P(V_{G_{M8}} - |V_{tp}|)}, \tag{4.7}$$

where $\left(\frac{L}{W}\right)$ are the aspect ratios of the MOSFET, $V_{G_{M8}}$ is the gate voltage at M8, which is 20 V, $\theta_P 1$ and $\theta_P 2$ are the first and second order of mobility degradation, K'_P and K'_N are gain factor, and V_{tp} and V_{tn} are the threshold voltage of the PMOS and NMOS respectively. Using the extracted parameters from Appendix B, the aspect ratio of M8 is found to be:

$$\left(\frac{W}{L}\right)_{M6} = \tfrac{10\mu m}{1.4\mu m}.$$

Since the voltage at node B discharges through the gate of M12, its fall time is harder to estimate. One solution is to try different sizes of M12 in the simulation, and obtain the minimum size for M12 to make the fall time within the acceptable range. The final sizes for the first stage of the MOSFET are found to be:

$$\left(\frac{W}{L}\right)_{M7} = \left(\frac{W}{L}\right)_{M8} = \frac{10\mu m}{1.4\mu m}, \tag{4.8}$$

$$\left(\frac{W}{L}\right)_{M11} = \left(\frac{W}{L}\right)_{M12} = \frac{50\mu m}{1.4\mu m}, \tag{4.9}$$

$$\left(\frac{W}{L}\right)_{M5} = \left(\frac{W}{L}\right)_{M6} = \left(\frac{W}{L}\right)_{M9} = \left(\frac{W}{L}\right)_{M10} = \frac{500\mu m}{1\mu m}. \tag{4.10}$$

The analysis for the second stage is very similar to that of M8. The MOSFET M16 and M15 must be large enough to reduce the rise/fall time (t_r) of the signal at the gate of M1 to within 2% of its ON-time. The maximum t_r would be 5 ns as shown in Equation (4.6). The total gate capacitance would be:

$$C_{tot} = C_{Gate_{M1}} + C_{Drain_{M15}} + C_{Drain_{M16}}, \tag{4.11}$$

where $C_{Gate_{M1}}$ is the gate capacitance of M1 and C_{Drain} is the drain capacitance of M15 and M16. These capacitances are estimated using the equations found in Appendix C. The gate driving circuit can be simplified to the circuit as shown in Figure 4.15.

The resistor R_{Driver} from Figure 4.15 is the ON resistance from the MOSFET M15 and M16, which can be estimated by:

$$R_{Driver} = \frac{L}{W}\frac{1 + \theta_1(V_G - V_t) + \theta_2(V_G - V_t)}{0.5K'(V_G - Vt)}, \tag{4.12}$$

where W and L are the width and length of the MOSFET, V_G is the gate voltage, V_t is the threshold voltage, θ_1 and θ_2 are the first and second order of mobility degradation. The width and length for M15 and M16 are set so that their ON resistance (R_{Driver}) are equal to each other, so the output signal will have the same rise and fall time. Assuming the maximum load that the level shifter can drive is $C_{tot} = 50pF$ (estimated gate capacitance of M1 from [4]), the rise-time of the gate driving signal can be estimated as:

$$2.2R_{Driver}50pF < 5ns, \tag{4.13}$$

$$R_{Driver} = \tfrac{5ns}{2.2 \cdot 50pF} < 45.5\Omega.$$

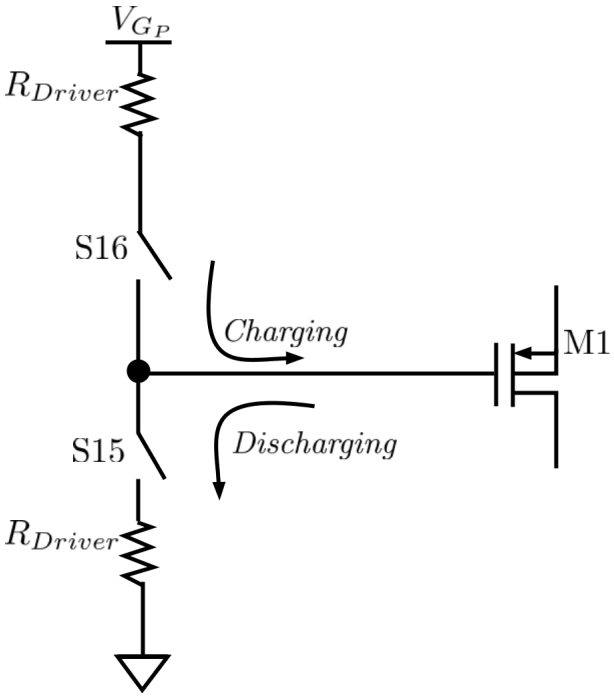

Figure 4.15: Simplified Gate Driving circuit

Using Equation (4.12) and the extracted parameters from Appendix B, the aspect ratio for M15 and M16 can be found as:

$$\left(\frac{W}{L}\right)_{M15} \approx \frac{350\mu m}{1\mu m}, \tag{4.14}$$

$$\left(\frac{W}{L}\right)_{M16} \approx \frac{820\mu m}{1.4\mu m}. \tag{4.15}$$

Similarly, the aspect ratio of M13 and M14 can be obtained by first estimating the total capacitance connected at the drain of the MOSFETs. Then, the on-resistance of M13 and M14 must be equal, and satisfies the rise/fall time requirement. Using the similar approach with the system of Equations (4.11), (4.12), and (4.13), the aspect ratios for M13 and M14 are:

$$\left(\frac{W}{L}\right)_{M13} \approx \frac{25\mu m}{1\mu m}, \tag{4.16}$$

$$\left(\frac{W}{L}\right)_{M14} \approx \frac{60\mu m}{1\mu m}. \tag{4.17}$$

The output waveform of the 30-50V level shifter is shown in Figure 4.16. Figure 4.17 shows the zoomed-in view of the output waveform to measure the total delay time. For this circuit, the

delay time (t_d) is approximately 6.5 ns, while the power consumption is 9.4 mW at 1 MHz under no-load condition.

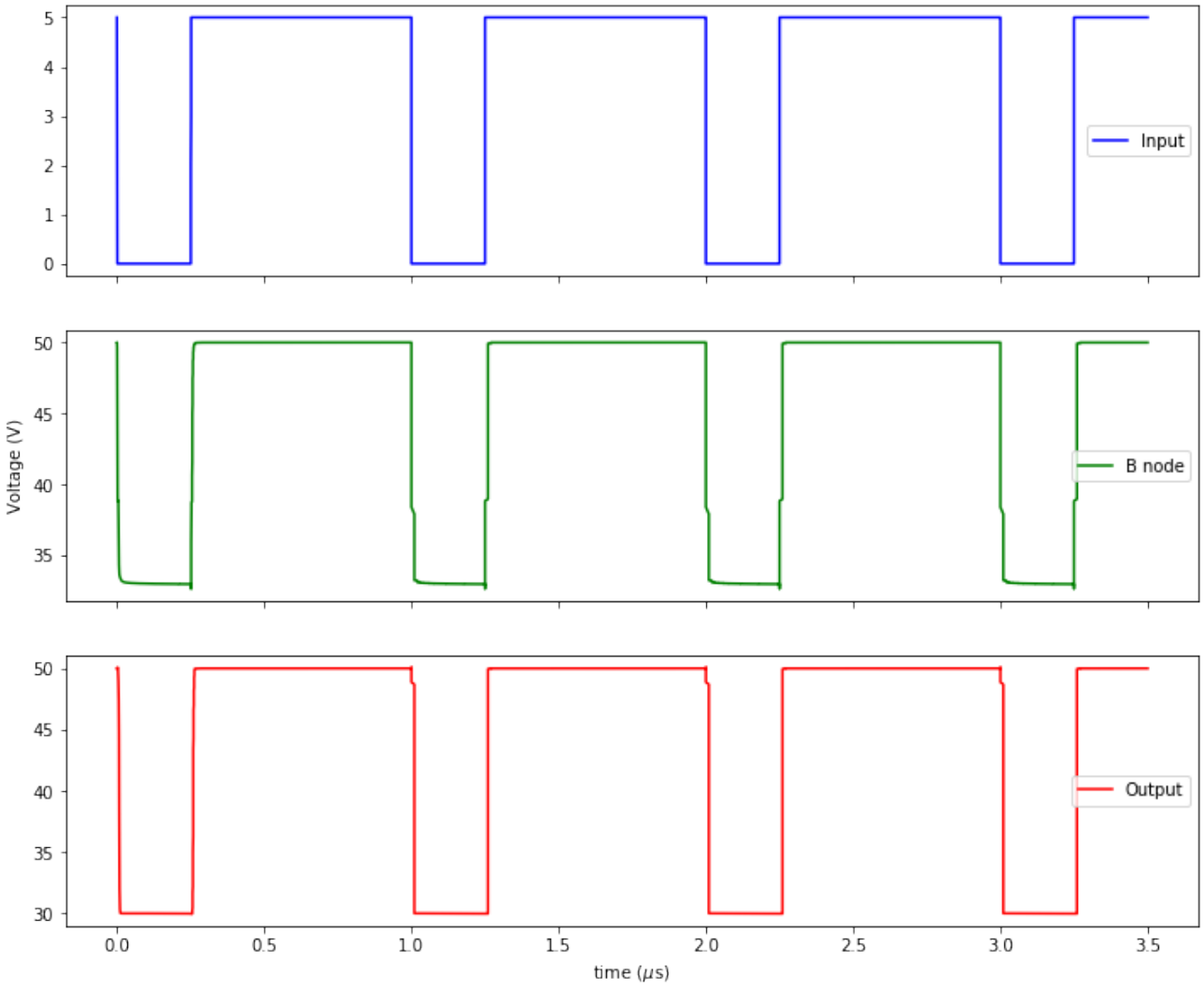

Figure 4.16: Simulated results of the proposed Level Shifter

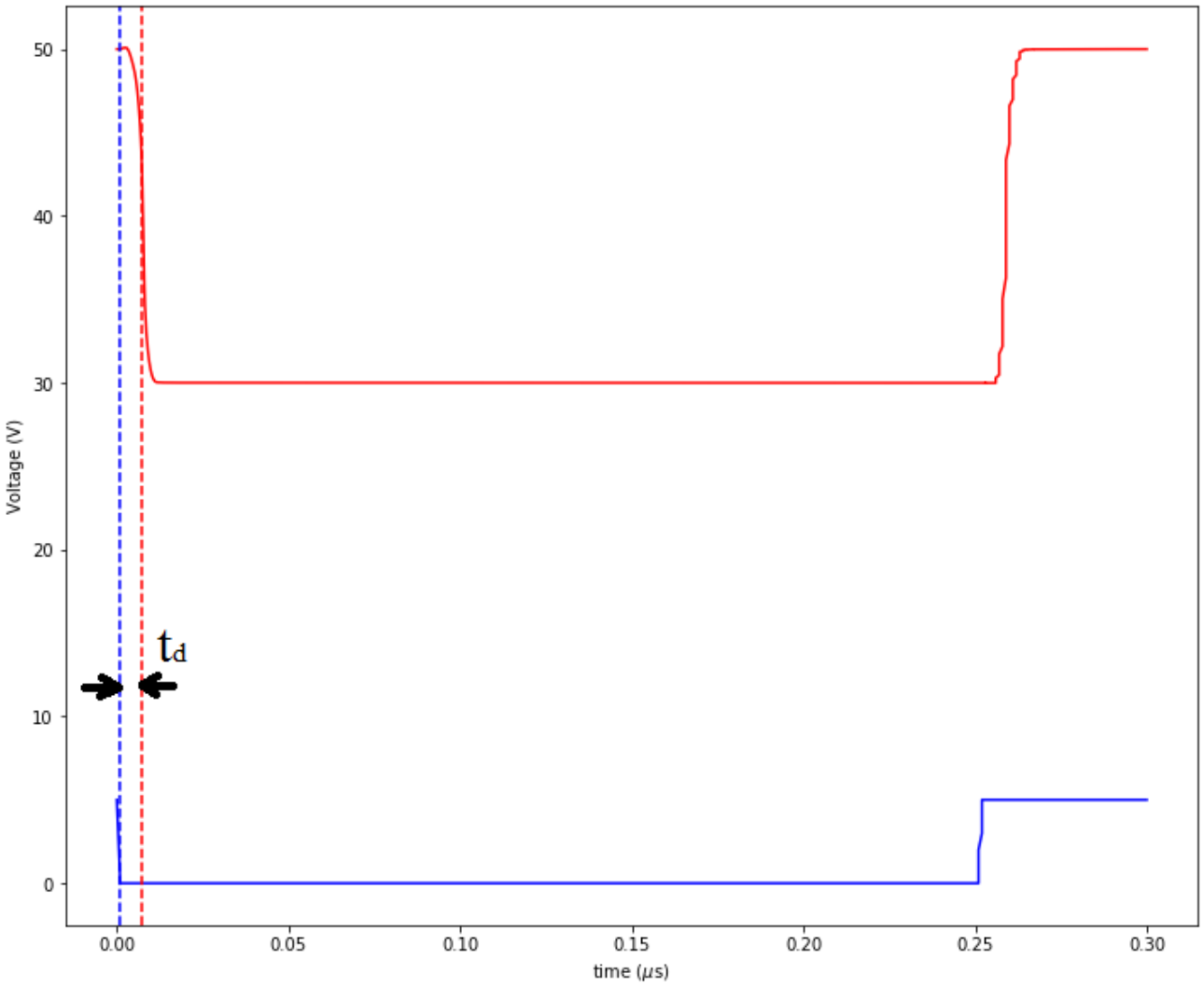

Figure 4.17: Close up view of the level shifter output waveform

4.5 20V Level Shifter

Figure 4.18 shows the 20 V level shifter for the NMOS. The design analysis is similar to that of the 30-50 V level shifter. However, since the NMOS typically has a lower gate capacitance than that of the PMOS, M21 and M22 can be much smaller than M15 and M16. Assuming the maximum gate capacitance at M2 is about 20 pF, the aspect ratios for M21 and M22 are:

$$\left(\frac{W}{L}\right)_{M22} = \frac{140\mu m}{1\mu m}, and \left(\frac{W}{L}\right)_{M28} = \frac{330\mu m}{1.4\mu m}. \tag{4.18}$$

Then, the aspect ratios for M17, M18, M19 and M20 can be found as follows:

$$\left(\frac{W}{L}\right)_{17} = \left(\frac{W}{L}\right)_{18} = \frac{220\mu m}{1\mu m}, \tag{4.19}$$

$$\left(\frac{W}{L}\right)_{19} = \left(\frac{W}{L}\right)_{20} = \frac{10\mu m}{1.4\mu m}. \tag{4.20}$$

Notice the 2 NMOS M17 and M18 are driven by 5V pulse, so their width-to-length ratios must be high to reduce the on-resistance, and also the signal fall time at point A.

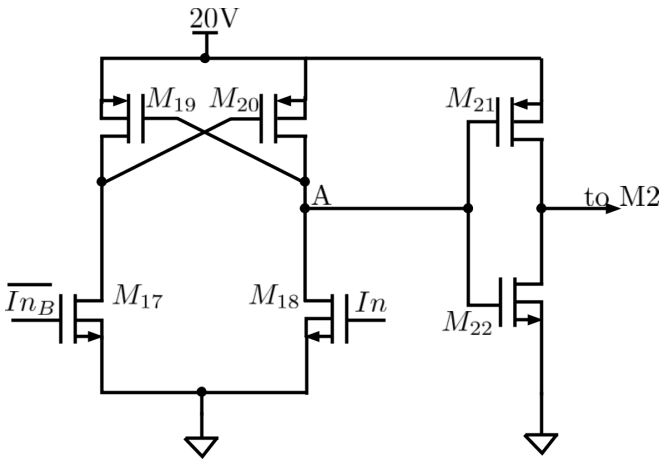

Figure 4.18: 20V Level Shifter design

4.6 Switch Design Methodology

4.6.1 Introduction

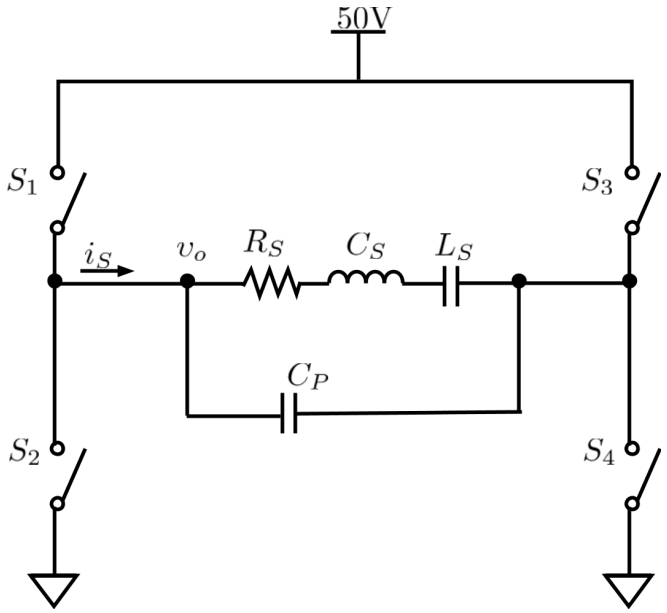

Figure 4.19: Simplified class DE amplifier in full bridge configuration

This chapter discusses the methodology in finding the optimum MOSFET sizes for class DE amplifier. Without the fullbridge class DE amplifier connected, the fixed power losses from the digital circuit, delay systems, and the level shifters is 41 mW. Both of the class DE amplifier designs [3] and [4] did not focus on optimizing the MOSFET sizes. The wider the MOSFET, the less ON-resistance, which would reduce the conduction loss. On the other hand, as the MOSFET gets wider, its gate capacitance also increases. Power losses in integrated circuit can cause heating problems, which affect the sustainability of the system. Therefore, in order to achieve the maximum power efficiency, the switching sizes must be optimum for the transducers. With the proposed system as shown in Figure 4.1, the simplified circuit is shown in Figure 4.19. With the current technology, PMOS50H is used for S1 and S3, whereas NMOS50H is used for S2 and S4, to allow 50V drain-to-source, and 20V gate-to-source nominal voltages. The voltage supply is 50V, which is right at the drain-to-source nominal voltage of the MOSFET, but it is needed to increase the output power.

The three main losses that are caused by the switched MOSFET amplifiers are:

- Switching loss

- Conduction loss
- Gate power loss

Among those three losses listed above, switching loss can be avoided by making sure the amplifier operating in ideal class DE condition. From Equation (3.24), switching loss is depended on the total parallel capacitance C_P, which includes the switch capacitance C_{SW}. However, this optimization technique ensures that the switch capacitance only contributes to a small fraction of C_P. Therefore, this switching loss will be affected mostly by driving method instead instead of the switch sizes. In ideal class DE condition, the main sources of power losses are the conduction loss from switch resistance and the power dissipated in the gate driver circuit.

4.6.2 Equation Formulation

Since switching loss will not be considered in this methodology, Equation (3.10) becomes:

$$I_P = \frac{2\omega C_P V}{1 - cos\phi}. \tag{4.21}$$

Here the switch resistance will be replaced by the unit resistance (R_u) of a MOSFET finger. Recall the switch resistance can be estimated by:

$$R_u = \frac{1 + \theta_1(V_G - V_t) + \theta_2(V_G - V_t)^2}{0.5K' \frac{nWu}{Lu_{eff}}(V_G - V_t)}, \tag{4.22}$$

where R_u is the unit resistance, W_u and L_u are the unit width and length of a single finger MOSFET. The switching resistance, R_{SW} can be reduced by stacking multiple MOSFET fingers in parallel, and thus equals to:

$$R_{SW} = \frac{2Ru}{n} = 2\frac{1 + \theta_1(V_G - V_{TH}) + \theta_2(V_G - V_{TH})^2}{n0.5K_N \frac{W_N}{L_N}}, \tag{4.23}$$

where n is the number of fingers of the MOSFET stacked in parallel. To simplify the calculation later on, the unit resistance of NMOS is set equal to that of the PMOS. Therefore, the unit width of the PMOS can be approximated by:

$$W_{Pu} = W_{Nu}\frac{1 + \theta_{P1}(V_{GP} - |V_{tp}|) + \theta_{P2}(V_{GP} - |V_{tp}|)^2}{1 + \theta_{N1}(V_{GN} - V_{tn}) + \theta_{N2}(V_{GN} - V_{tn})^2} \cdot \frac{K'_N L_{Pu}(V_{GN} - V_{tn})}{K'_P L_{Nu}(V_{GP} - |V_{tp}|)}. \tag{4.24}$$

The unit width and length for PMOS and NMOS are shown in Table 4.1. Since the full-bridge configuration is used, the equation for k factor (3.19) should be consider:

$$k = \frac{4R_u\omega C_P(1 - cos(\pi - \phi))}{n(1 - cos\phi)(\pi - \phi)}. \tag{4.25}$$

Table 4.1: Unit sizes for NMOS (M2 and M4) and PMOS (M1 and M3)

	NMOS	PMOS
W_u/L_u	50μm/1μm	126μm/1.4μm

Thus, the estimated load power would be:

$$P_L = \frac{1}{2} R_S \left(\frac{2\omega C_P V}{(1+k)(1-cos(\phi))} \right)^2. \tag{4.26}$$

Following a reasoning similar to the one used to derive Equation (3.24), the power loss due to the gate capacitance of one MOSFET would be:

$$P_{gate_{cap}} = f C_{gate} V_G^2, \tag{4.27}$$

where C_{gate} is the total capacitance at the gate of the MOSFET, and V_G is the gate voltage. Since all MOSFET in Figure 4.19 are driven by 20 V_{pp} pulse, V_G is equal to 20V. The total gate capacitance is already approximated with Equation (4.11). The total gate power loss is thus:

$$P_G = 2nfC_{G_N} V_G^2 + 2nfC_{G_P} V_G^2 + 41mW, \tag{4.28}$$

where $C_{G_N} = 0.223$ pF and $C_{G_P} = 0.2342$ pF are the unit gate capacitance (1 finger) with the current technology of NMOS and PMOS respectively, and 41 mW is the fixed power loss from driving circuit under no-load condition at 1 MHz. This power loss is frequency dependent. However, because the target operating frequency is close to 1 MHz, the difference can be negligible.

Design Steps

To generalize the amplifier design steps, the following assumptions must be made:

- All assumptions used for the theory analysis from Chapter 3.
- Transducer's approximated values of Rs and resonant frequencies are known.
- All transducers are operating in ideal class DE operation.
- Duty cycle is near 25%.

The design steps for this methodology are as follows:

1. Approximate the operating frequency for the target transducers. This step is doable, since the optimum mechanical frequency of a transducer is dependent on its material and thickness.

2. Set D = 0.25 as an average duty cycle. Since the transducer is assumed to operate in ideal class DE operation. Then, C_P can be solved for a given value of Rs using Equation (3.13). Since D is fixed at 0.25, Equations (4.25), (4.26) and (3.22) become:

$$k = \frac{8R_u\omega C_P}{n\pi}, \tag{4.29}$$

$$P_L = \frac{1}{2}R_S\left(\frac{2\omega C_P V}{1+k}\right)^2, \tag{4.30}$$

$$P_{RSW} = \frac{1}{n}\frac{Ru}{R_S}P_L. \tag{4.31}$$

3. Sweep the number of fingers between 1 to the maximum allowable die area. For each value of n, compute the power efficiency using (4.32).

$$\eta = \frac{P_L}{P_L + P_{RSW} + P_{Gate}}. \tag{4.32}$$

4. Plot η vs. n, and select the number of fingers that fits the design's criteria.

4.6.3 Case Study

Using the above design steps, the optimum number of fingers for the 2 transducer arrays used in sections 3.3 and 3.4 can be decided as follow:

1. The operating frequency for these 2 transducers can be approximated between 1000kHz and 1100kHz. The average frequency of 1050kHz is chosen for this step

2. The load resistance will be the average R_S of the entire array. The resistances for the transducer array from Tables 3.1 and 3.6 are 583 Ω and 41.8 Ω, respectively.

Case I - Small Transducer Array from section 3.3

For the transducer array used in 3.3, the average R_S is found to be 583 Ω. Follow the design steps with the supply voltage connected to 50 V as shown in Figure 4.19, the power efficiency

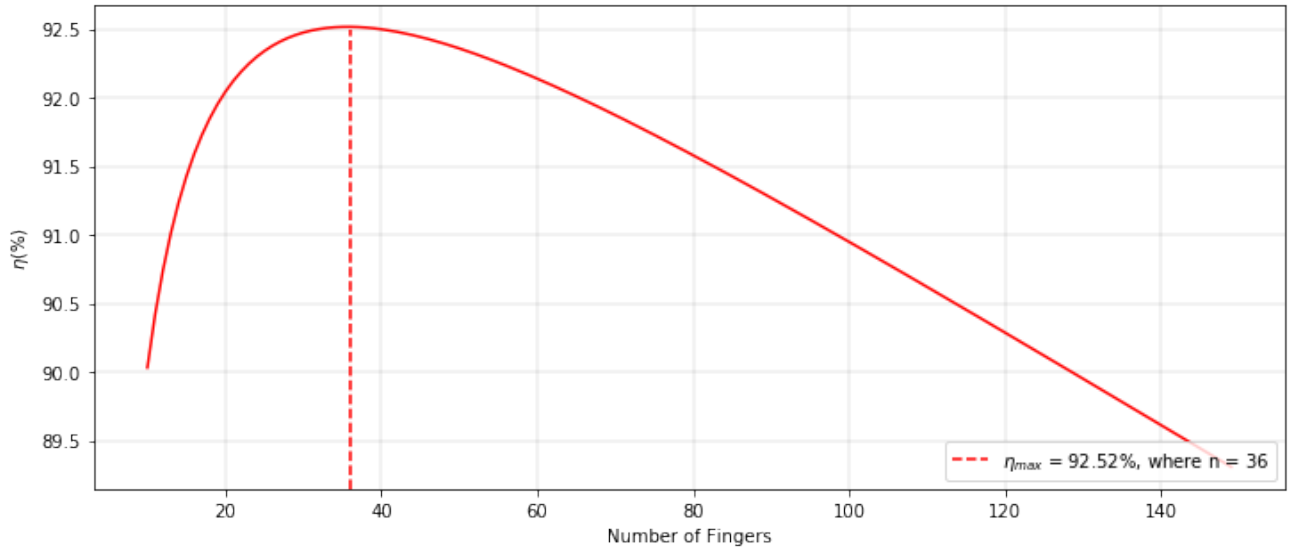

Figure 4.20: Power efficiency vs number of fingers for transducer array used in section 3.3

vs. number of fingers can be observed in Figure 4.20. This plot shows that the maximum power efficiency is at 92.5% when 36 fingers are used.

Another factor that needs to be considered is the total switch capacitance C_{SW}. Since the full-bridge configuration is used, C_{SW} is reduced by half. This switch capacitance will be added to the total parallel capacitance (C_P) at the load, and may prevent the amplifier from operating in ideal class DE condition. P_S will increase, and thus the power efficiency will be reduced. Figure 4.21 shows the switching capacitance as a function of the number of fingers used. For this design, since the switch capacitance is so small, even compared to the stray capacitance from the circuit, this factor can be neglected.

Case II - Large Transducer Array from section 3.4

For the transducer array used in section 3.4, the average R_S is found to be 41.8 Ω. With the load resistance a lot smaller than the previous design, the number of fingers is expected to be much bigger. Figure 4.22 shows the power efficiency vs. the number of fingers required. The maximum power efficiency can be achieved is 97% when n = 480. However, the power efficiency can reach 96% at n = 233, which means half of the die area can be saved at the cost of only 1% in power efficiency. Figure 4.23 shows the switch capacitance at different MOSFET sizes. To

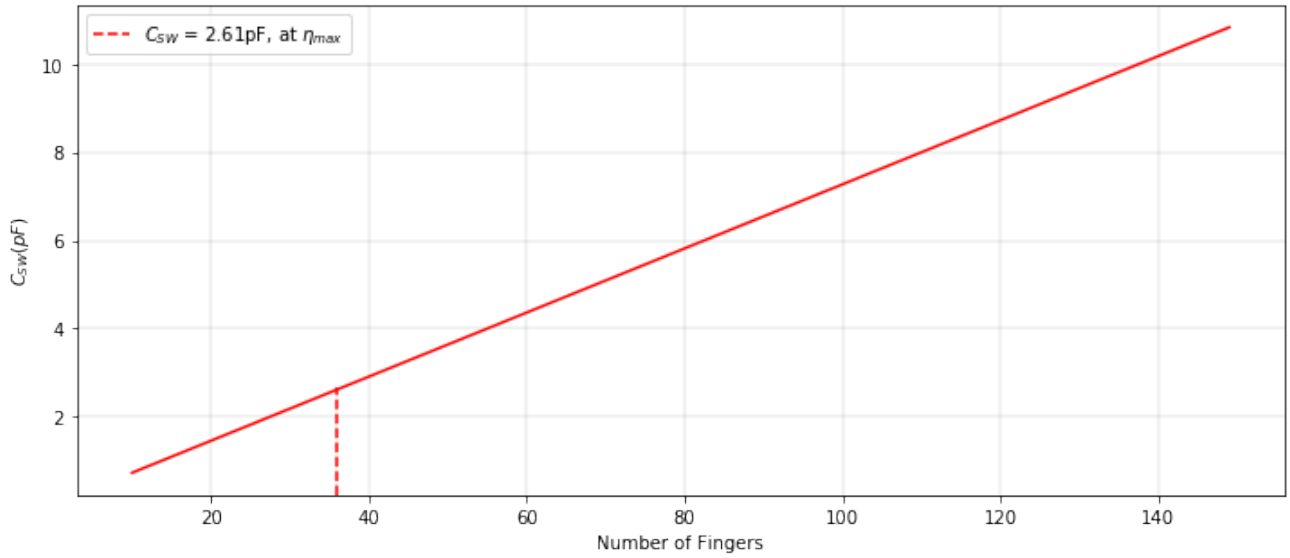

Figure 4.21: Switch capacitance vs number of fingers for transducer array used in section 3.3

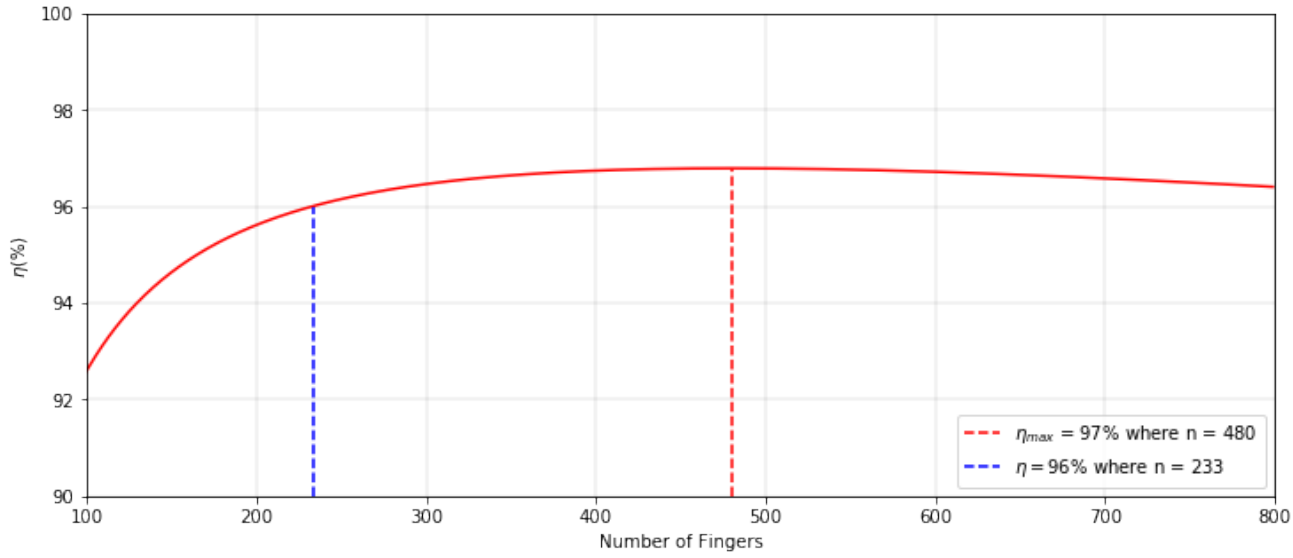

Figure 4.22: Power efficiency vs number of fingers for transducer array used in section 3.3

achieve the maximum-possible power efficiency, C_{SW} is increased more than 2 times compared to when the power efficiency is set at 96%. As a result, the MOSFET sizes for this design are set at 233 fingers.

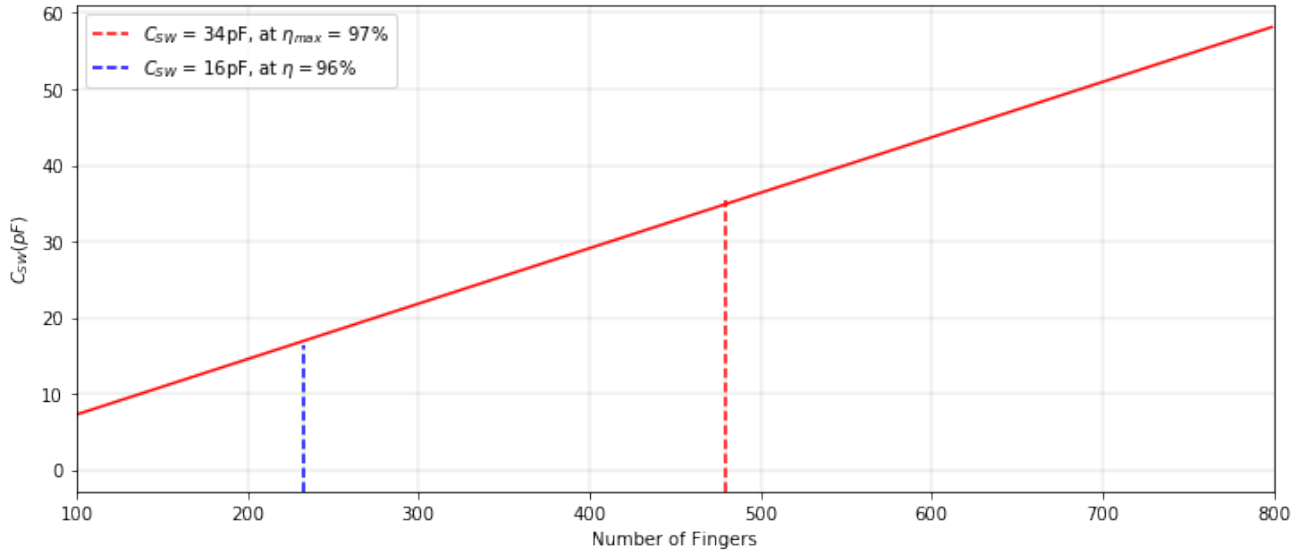

Figure 4.23: Switch capacitance vs number of fingers for transducer array used in section 3.4

Case III - Design for both sets of transducer array

Another situation for this case study is to design the driver for both of the transducers array used in section 3.3 and 3.4. The number of fingers in this case is chosen to be in between 36 and 233 from the previous 2 designs, which is 135. Figure 4.24 shows how the designs from 3 cases would work with different load resistance. The design from Case I suffers from the low load resistance, as its power efficiency drops down below 80%. Case II and Case III offer a wider range of R_S selection, as their power efficient are always kept above 80% in ideal class DE operation. However, switch capacitance is main drawback of Case II design when it used for higher R_S. Since higher R_S usually requires less C_P to operate in ideal class DE operation, the high value of C_{SW} from the design in Case II is unsuitable the transducer array used in Case I. The most important factor is the amount of power loss from the driving circuit. Figure 4.25 shows the power loss in all 3 cases. At lower load resistance, the power loss are quite high, and may require a heat sink to prevent any damage to the chip.

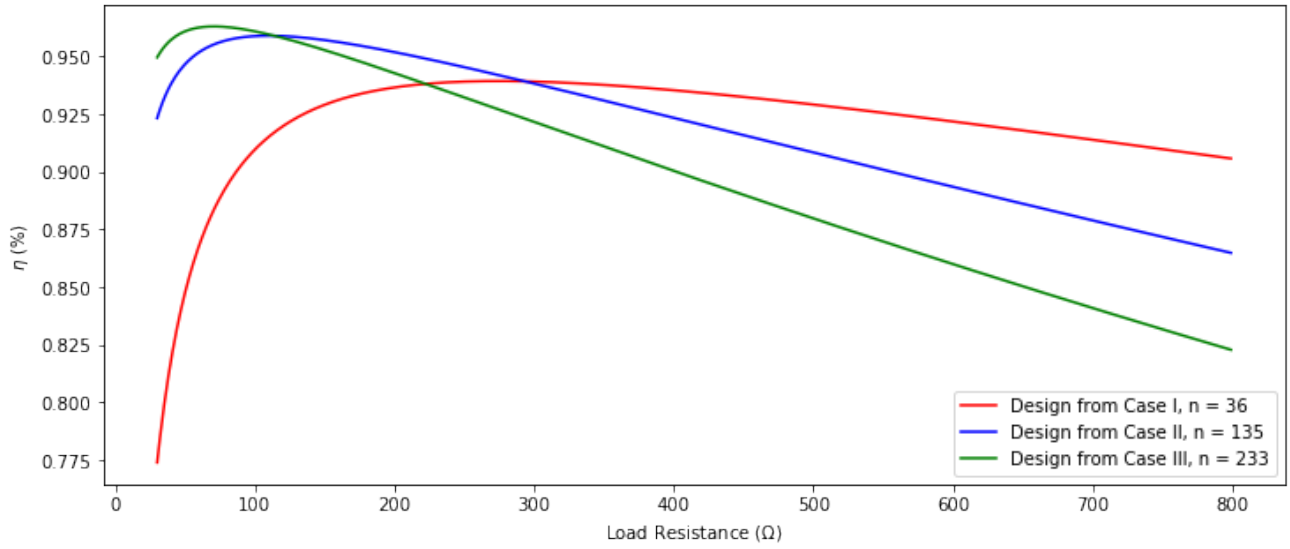

Figure 4.24: Power efficiency vs load resistance

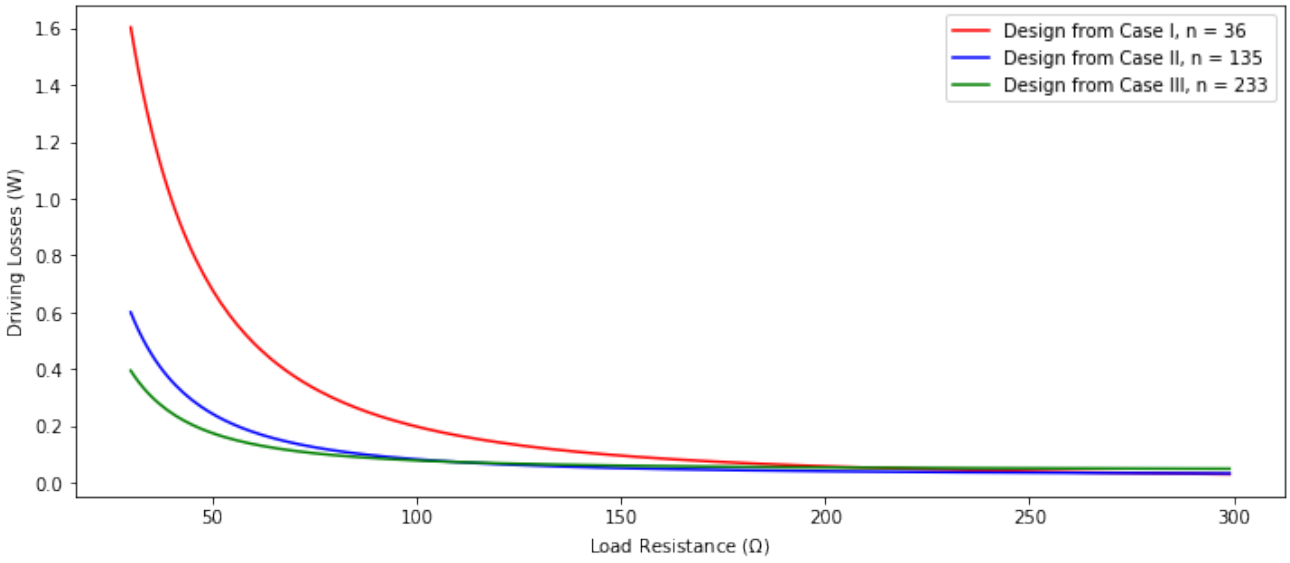

Figure 4.25: Power losses from all 3 cases

4.7 Driver Performance in an array

4.7.1 New driver vs. old design using the same voltage supply

Expected Results

Although there several drivers for piezoelectric transducers that can achieve more than 90% power efficiency, they all require external matching networks containing inductors as shown in Table 2.2. These matching network circuits woud interfere with the MRI-guidance system, so they cannot be used within the bore. Other proposed designs do not require inductors, but efficiency is not one of the main consideration in these designs, and thus they tend to achieve lower efficiencies. As a result, this work will be compared with the design from [4] which implements class DE amplifier to achieve high efficiency without a matching network. Firstly, the performance of the new driver will be tested at the same voltage (20 V) to compare with the design in [4]. Since the design from [4] is specifically for a smaller R_S transducer array, its switch resistance is low, and can be neglected in the calculation. As a result the conduction loss and other effect caused by R_{SW} are assumed to be 0. However, for this new design, the MOSFET sizes are much smaller, so the switch resistance will play an important role in power losses, and cannot be neglected. Also, the switching capacitance from [4] is found to be 10 pF. By measuring the total capacitance experimentally, C_{ext} is found to be 15 pF from the probe and stray capacitance. Since these external capacitance are unavoidable, the calculation from this work will use the same C_{ext} as shown in Figure 4.27. Table 4.2 shows the expected results from both designs to see the difference.

Notice the new design is used at different frequency than the old design because of the change in output capacitance. Figure 4.26 shows the power efficiency vs operating frequency. At $f =$ 1064 kHz, the overall efficiency is at its maximum. Using the same voltage supply, the new driver shows some improvement compared to the old design. The average power efficiency is increased from 47.7% to 78.8%. Also, the average load power is increased from 194 mW to 336 mW. The most important improvement is the reduction in total power loss. Since one of the main objectives in this research is to reduce the power loss to prevent heating problem. The average power loss is reduced from 220 mW to 89 mW.

Table 4.2: Expected result for each transducer using the driving method from section 3.3

	Previous design at f = 1069 kHz						This design at f = 1064 kHz					
Transducer	1	2	3	4	5	6	1	2	3	4	5	6
$D(\%)$	22	22	30	29	27	19	35	25	35	31	33	32
δ	0.72	0.30	0.77	0.86	0.57	0.37	0.99	0.07	1.05	0.52	0.89	0.32
P_L (mW)	146	151	265	200	290	112	404	187	353	248	403	420
P_S (mW)	27	5	29	29	20	7	47	0	48	10	45	5
P_G (mW)	200	200	200	200	200	200	55	55	55	55	55	55
P_{RSW} (mW)	0	0	0	0	0	0	10	4	7	4	10	13
$\eta(\%)$	42.7	43.8	55.3	49.2	58.2	37.1	79	76	76	78	79	85

Simulation Results

The simulation is set up as shown in Figure 4.27. The voltage supply V_{HV1} and V_{HV2} at set at 0 V and 20 V, respectively for this case study. The output voltage is the difference between υ_1 and υ_2

$$Output\_Voltage = \upsilon_1 - \upsilon_2. \tag{4.33}$$

The transient current is taken where the ammeter in Figure 4.27 is located. With this setup, the load current can be calculated as:

$$P_L = average(Output\_Voltage * i_6). \tag{4.34}$$

The conduction and switching losses are the difference between the total power from the (50V voltage source times the current i_5) and P_L:

$$P_{RSW} + P_S = average(V_{HV2} * i_5) - P_L. \tag{4.35}$$

The power loss from the gate driver is the sum of power taken from the 5 V, 30 V and 5O V sources that connect to the level shifters and the pulse train generator.

$$P_G = average(V_{HV2} * i_4) + average(V_{HV1} * i_3) + average(20 * i_2) + average(5 * i_1). \tag{4.36}$$

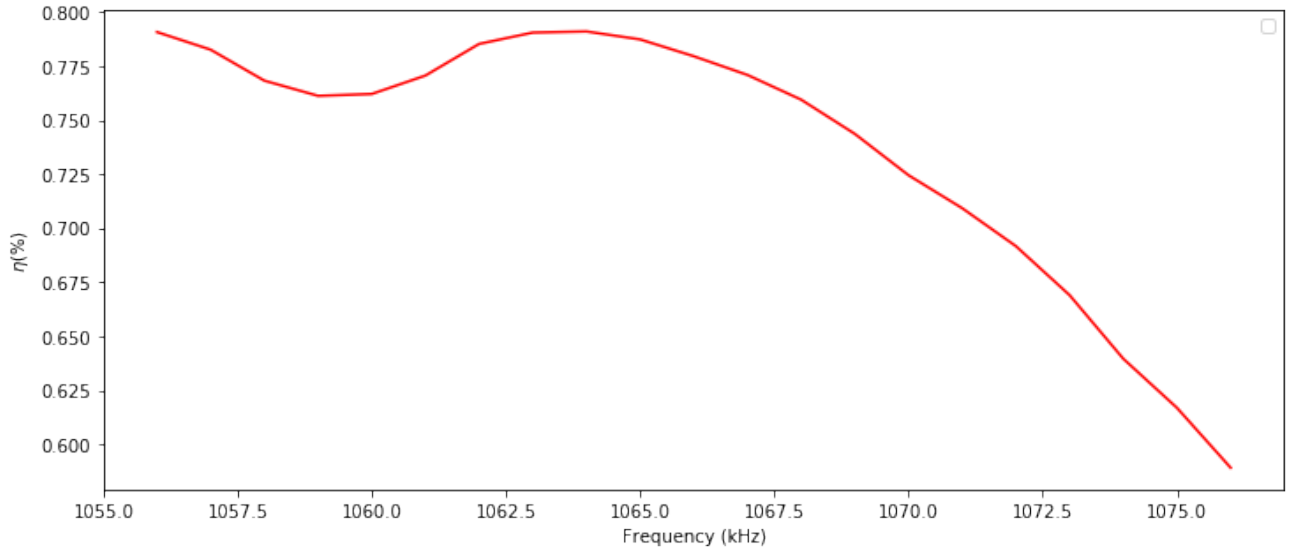

Figure 4.26: η vs. frequency when the power supply is connected to 20 V

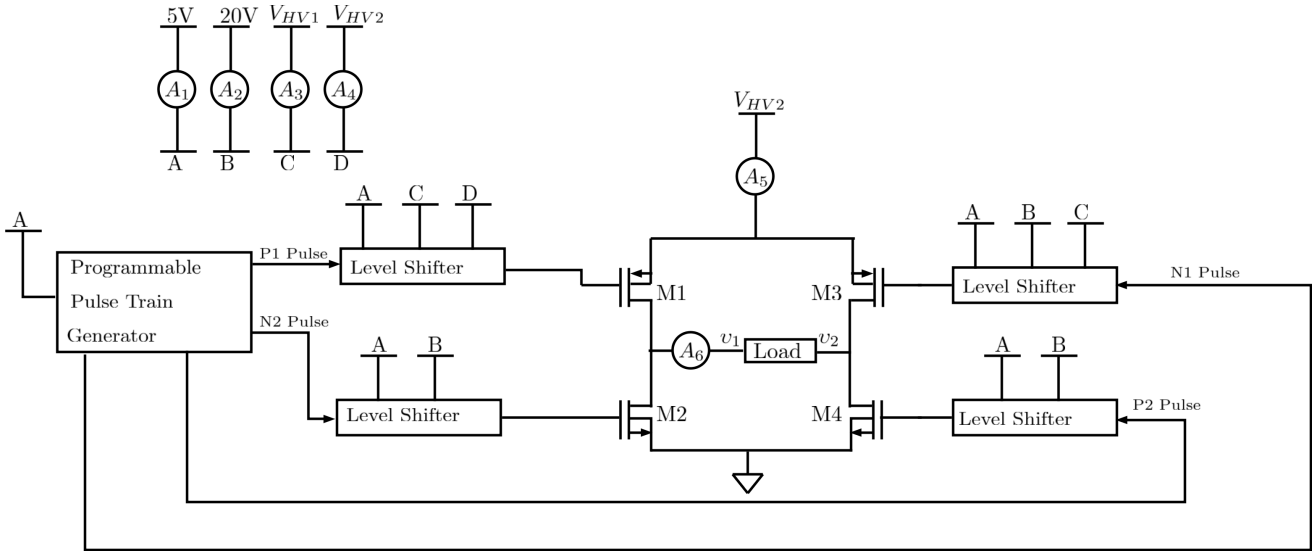

Figure 4.27: Simulation setup

To find the switching loss in the simulation results, a python code is used, to calculate the average power at the instance when the switch is turned ON, t_S (between the green line as shown in Figure 4.28). Assuming the waveforms are symmetric, the switching loss can be extracted using the equation:

$$P_S = 2 * average((20 - v_o) * i_s * t_S * f), \tag{4.37}$$

where v_o and i_s are the output voltage and current during the time interval t_S (the red and blue line in Figure 4.28 respectively). The the conduction loss (P_{RSW}) can be found by subtracting Equation (4.35) by (4.37).

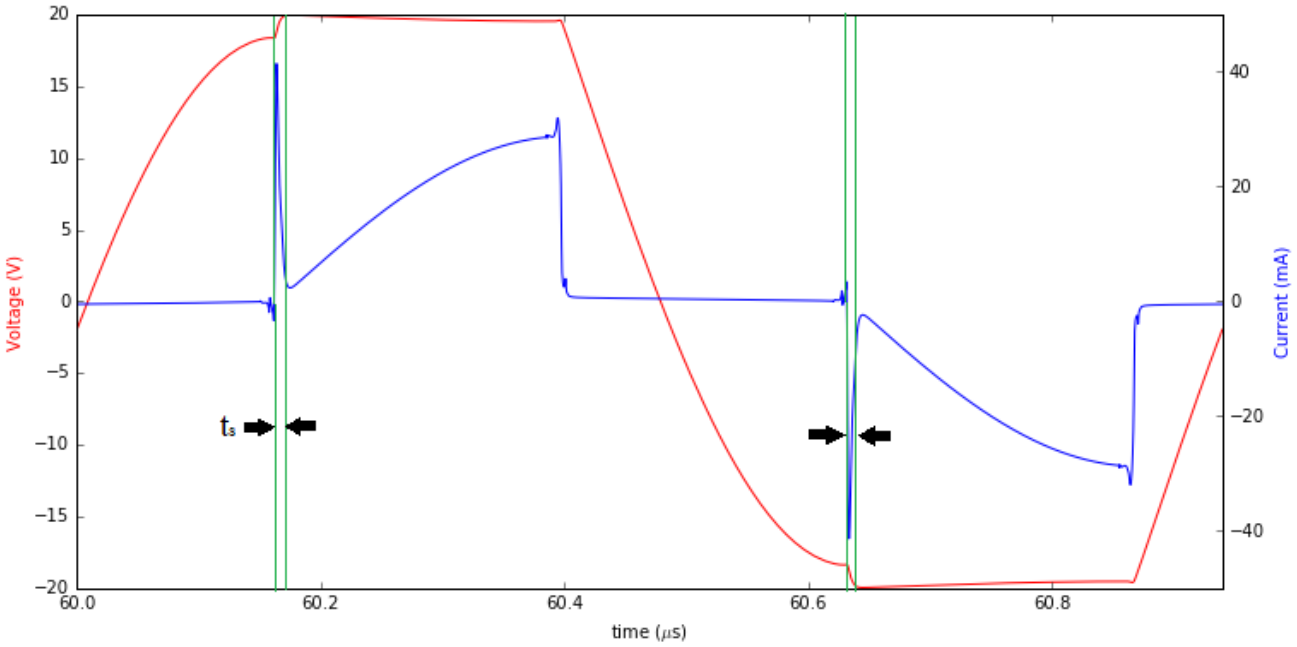

Figure 4.28: Extracting switching loss from simulation, red line is v_o, and blue line is i_s

The simulation results are very close to the calculations as shown in Table 4.3.

Table 4.3: Simulated results for each transducer using the driving method from section 3.3

	Calculation						Simulation					
Transducer	1	2	3	4	5	6	1	2	3	4	5	6
$D(\%)$	35	25	35	31	33	32	35	25	35	31	33	32
δ	0.99	0.07	1.05	0.52	0.89	0.32	0.95	0.08	1.04	0.51	0.88	0.34
P_L (mW)	404	187	353	248	403	420	388	185	348	241	398	397
P_S (mW)	47	0	48	10	45	5	40	0	44	9	42	5
P_G (mW)	55	55	55	55	55	55	55	53	55	54	55	54
P_{RSW} (mW)	10	4	7	4	10	13	11	4	10	4	11	12
$\eta(\%)$	79	76	76	78	79	85	78.6	76.4	76.2	78.1	78.7	84.9

4.7.2 Driver Performance with 50V voltage supply

Since the new driver is designed to drive the transducer load at 50 V_{PP}, the average output power is expected to be much higher. Figure 4.29 shows the maximum efficiency can be achieved when $f = 1068$ kHz. Table 4.4 shows the expected results from the new design. The simulated

Table 4.4: Expected results from new design for each transducer using the driving method from section 3.3

Transducer	1	2	3	4	5	6
$D_{opt}(\%)$	29	21	30	26	30	27
P_L (mW)	1655	733	1606	955	2049	1532
δ	0.52	0.10	0.66	0.30	0.67	0.06
P_S (mW)	83	3	119	19	163	1
P_{RSW} (mW)	30	10	27	12	44	37
P_G (mW)	55	55	55	55	55	55
η (%)	90.8	91.5	88.9	91.7	88.7	94.3

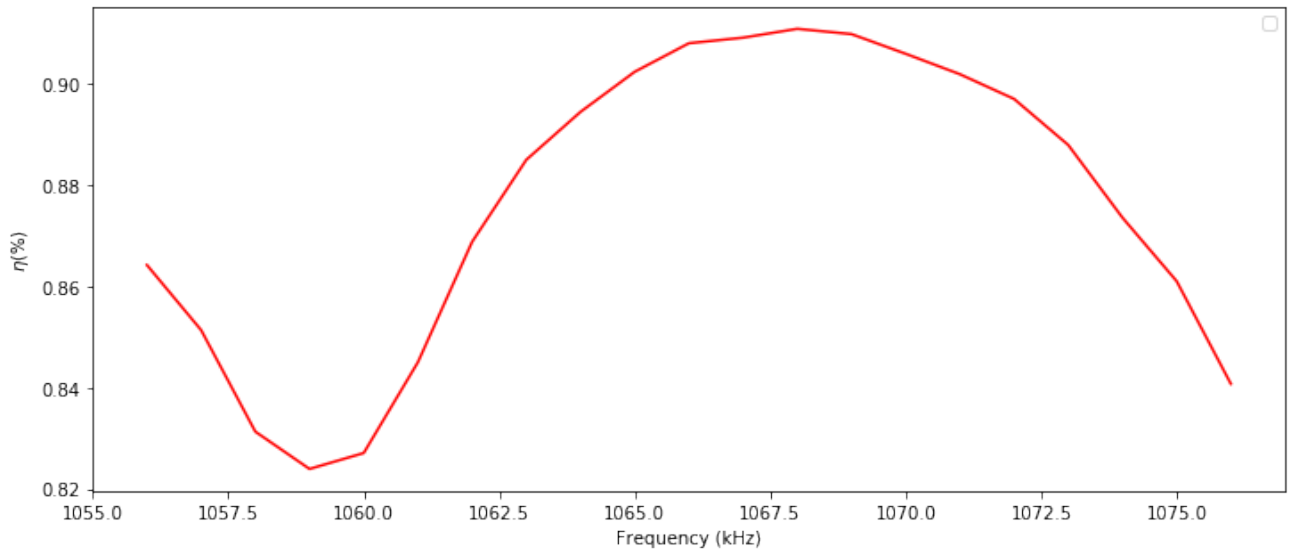

Figure 4.29: η vs. frequency when using 50 V voltage supply

results are shown in Table 4.5. These results are obtained by changing V_{HV1} and V_{HV2} in Figure 4.27 to 30 V and 50 V, respectively. The performance from this new design shows some very promising results:

- The expected load power is increased from 194mW in [4] to 1422 mW. This is because the new driver supports 50 V voltage supply to offer more output power.
- Even with a higher voltage supply, the switching loss (P_S) is even reduced for transducer 2, 4 and 6. This is because of low switch capacitance from this new design, which enables some transducers to operate closer to ideal class DE operation ($\delta \approx 0$).
- Because of the new level shifter design, the gate power loss is reduced by a significant amount, which increases the overall power efficiency.
- The average total power loss is about 144 mW from simulations. This amount of power loss should be safe for the driver to operate without any heating problems.

Table 4.5: Simulated results from new design for each transducer using the driving method from section 3.3

Transducer	1	2	3	4	5	6
$D_{opt}(\%)$	29	21	30	26	30	27
δ	0.53	0.11	0.66	0.30	0.65	0.08
P_L (mW)	1666	712	1597	961	2003	1466
P_S (mW)	82	4	112	19	149	2
P_{RSW} (mW)	36	9	33	13	48	33
P_G (mW)	54	54	54	54	54	54
η (%)	90.7	91.6	88.9	91.8	88.9	94.4

Chapter 5

Conclusions

The main objectives for this thesis have been achieved, as the simulation results show that the new driver design works as expected, and addresses several challenges in designing the integrated amplifier:

1. The average power delivered to the transducer array discussed in section 3.3 has been increased to 1422 mW. This objective is achieved by using a higher voltage supply without exceeding the break-down voltage of the MOSFET model (NMOS50H and PMOS50H) used in this work (50V drain-to-source, and 20V gate-to-source nominal voltages).

2. Improving the power efficiency by reducing the power consumption by the gate driver's circuit to 41 mW under no-load condition.

3. The re-designed digital logic unit allows 360^o phase shift, and 1% duty cycle resolution.

4. Two drive methods are introduced to reduce the switching power loss in suboptimal class DE condition, obtain the optimum drive parameters (frequency and duty cycle) to maximize power efficiency, and equalize load power while driving the entire transducer array.

5. The average total power loss is 144 mW, which is in acceptable range. Through experiments, a driver using the same technology and same chip package can handle 300 mW of power losses without any heating problems.

6. The new proposed method to determine the optimum switching MOSFET sizes can help achieving the best-possible power efficiency.

By using the design and methodology introduced this thesis, the load power is increased significantly compared to [4] while the driving losses is reduced. As a result, the overall power efficiency has increased from 47.7% in [4] to 91% in this work.

5.1 Future Work

There are still a lot more work needed to improve the performance of the ultrasound driver:

1. The electrical characteristic of the ultrasound is sensitive to the surrounding environment. Hence, there is a need for a feedback circuit to constantly measure the output power, and calculate power efficiency. Then, the duty cycle can be adjusted accordingly to keep the power efficiency at maximum.

2. In this design, an external clock signal is still used at a high frequency. At 100 MHz, a 20 cm cable can be considered a transmission line, which can have an effect on the clock signal, and disturb the functionality of the digital circuit.

3. The technology used in this work has a 50 V drain-to-source nominal voltage, which prevents the amplifier to connect to a higher voltage supply, and output more power.

4. The driver must be fabricated and tested in the MRI environment. The experimental results are needed verify the methodology proposed in this thesis.

Chapter 6

Appendix A - Expected and Simulated Results from the new design

6.1 Output Waveform with 20V Supply

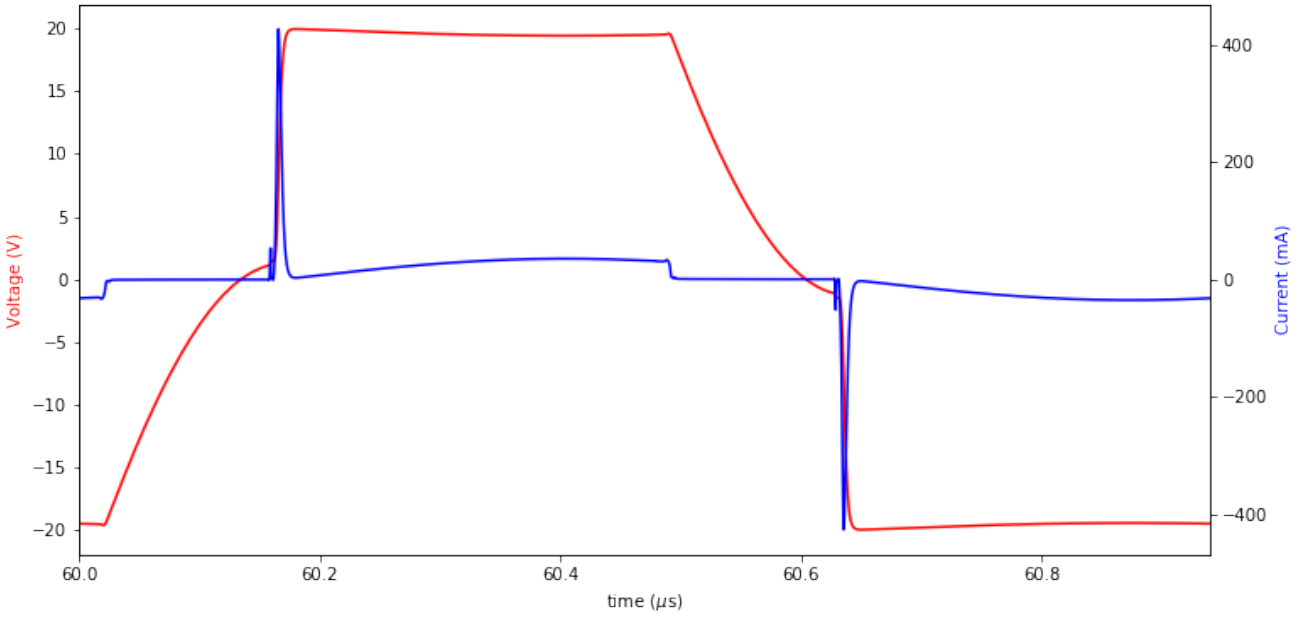

Figure 6.1: Output Voltage and Current of transducer 1

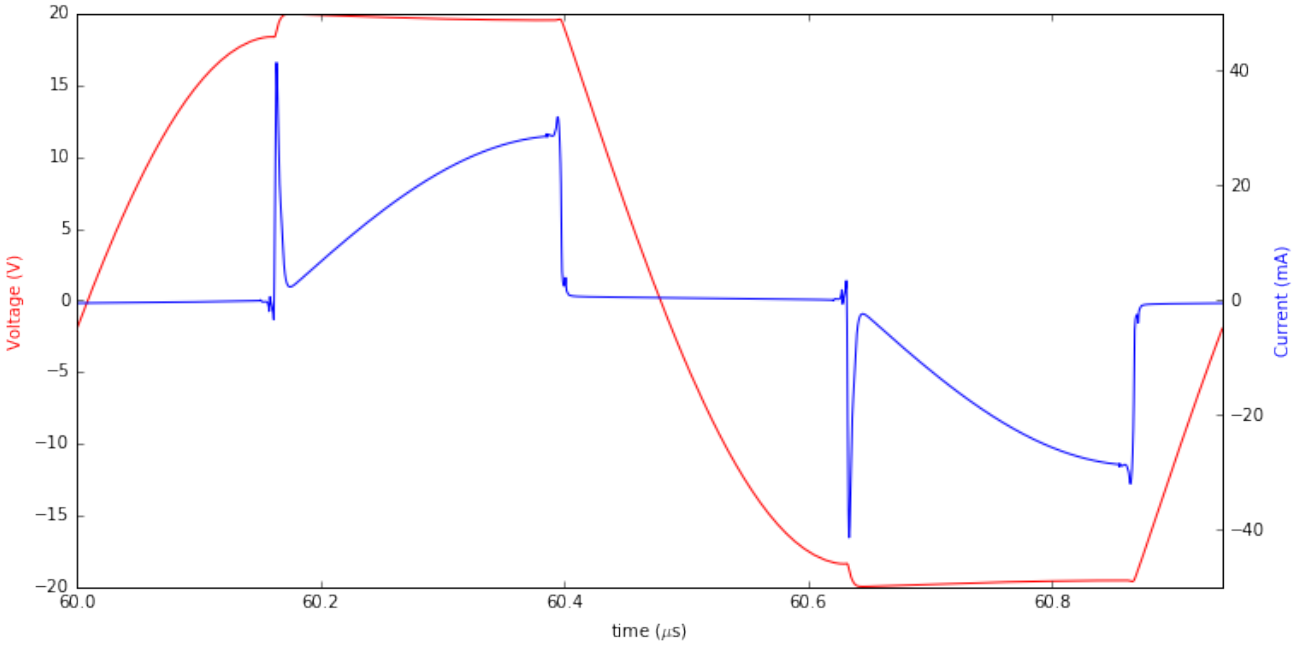

Figure 6.2: Output Voltage and Current of transducer 2

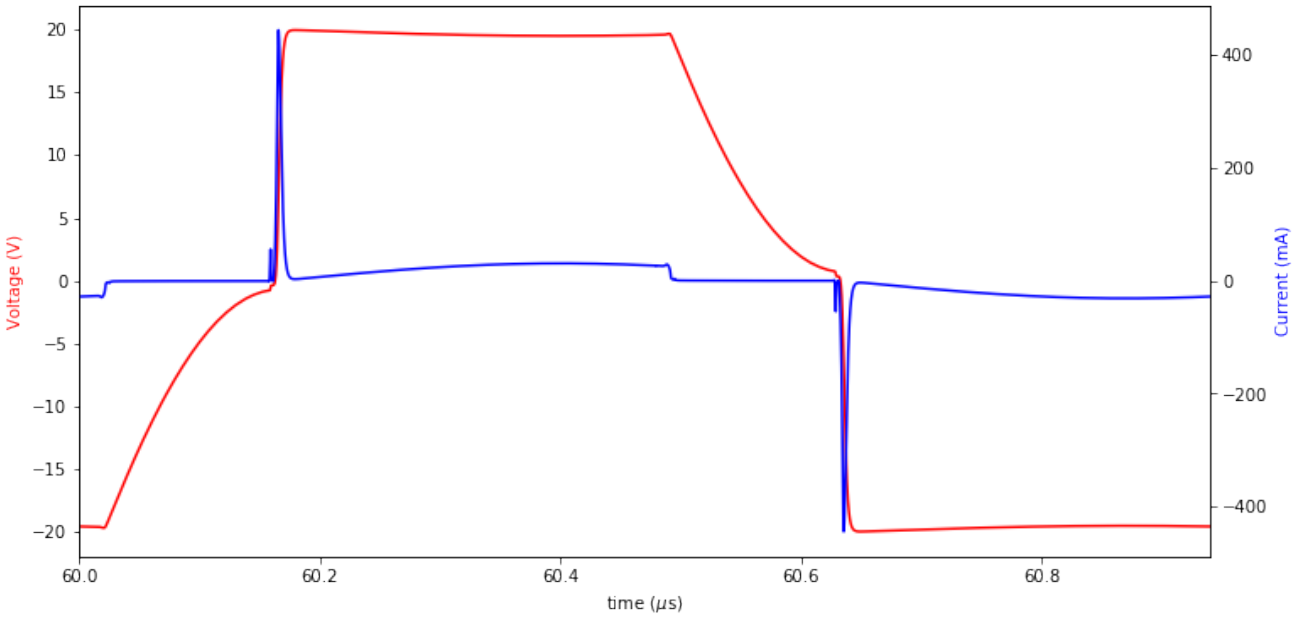

Figure 6.3: Output Voltage and Current of transducer 3

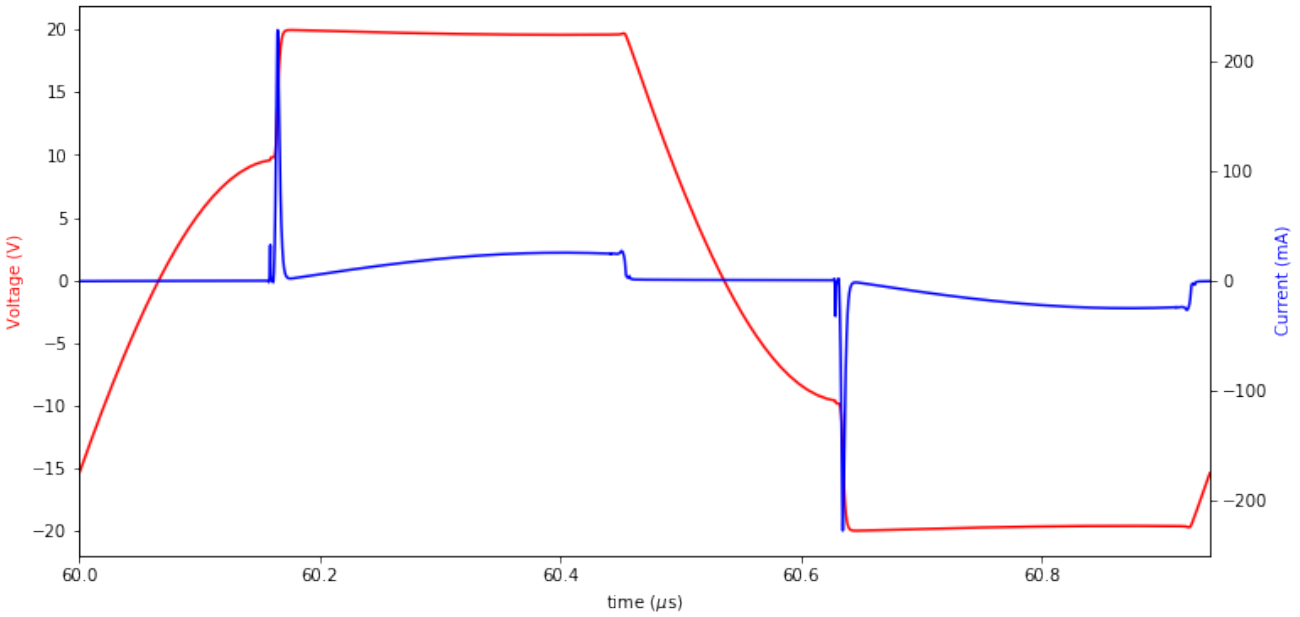

Figure 6.4: Output Voltage and Current of transducer 4

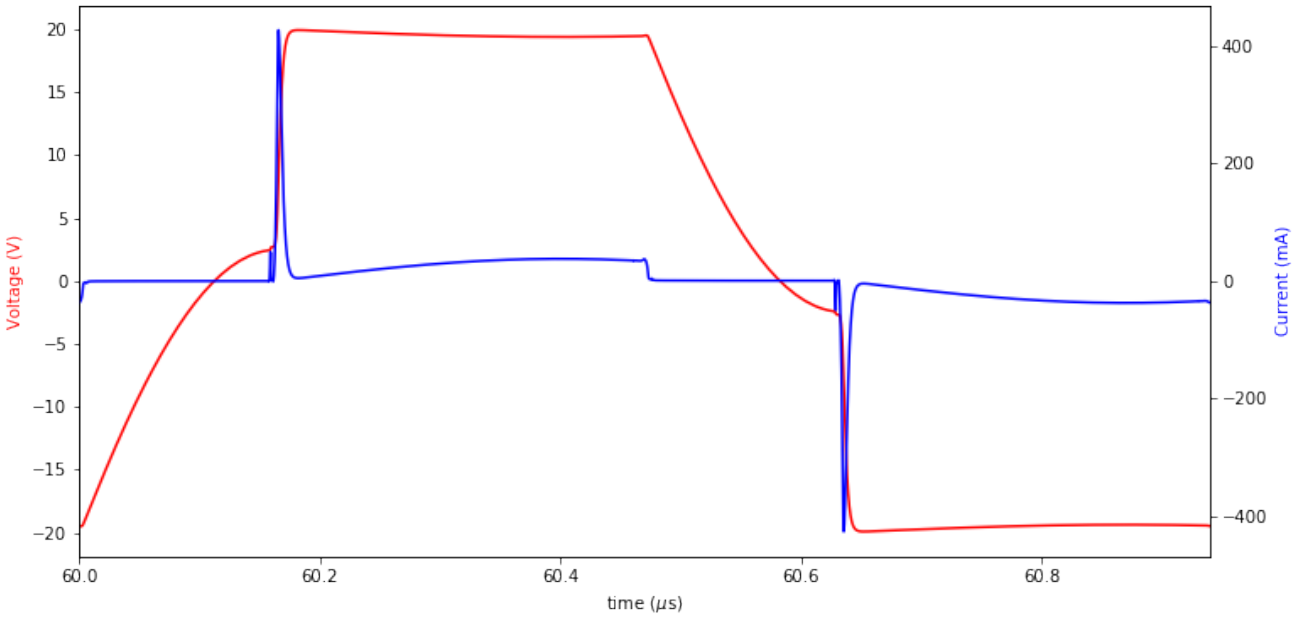

Figure 6.5: Output Voltage and Current of transducer 5

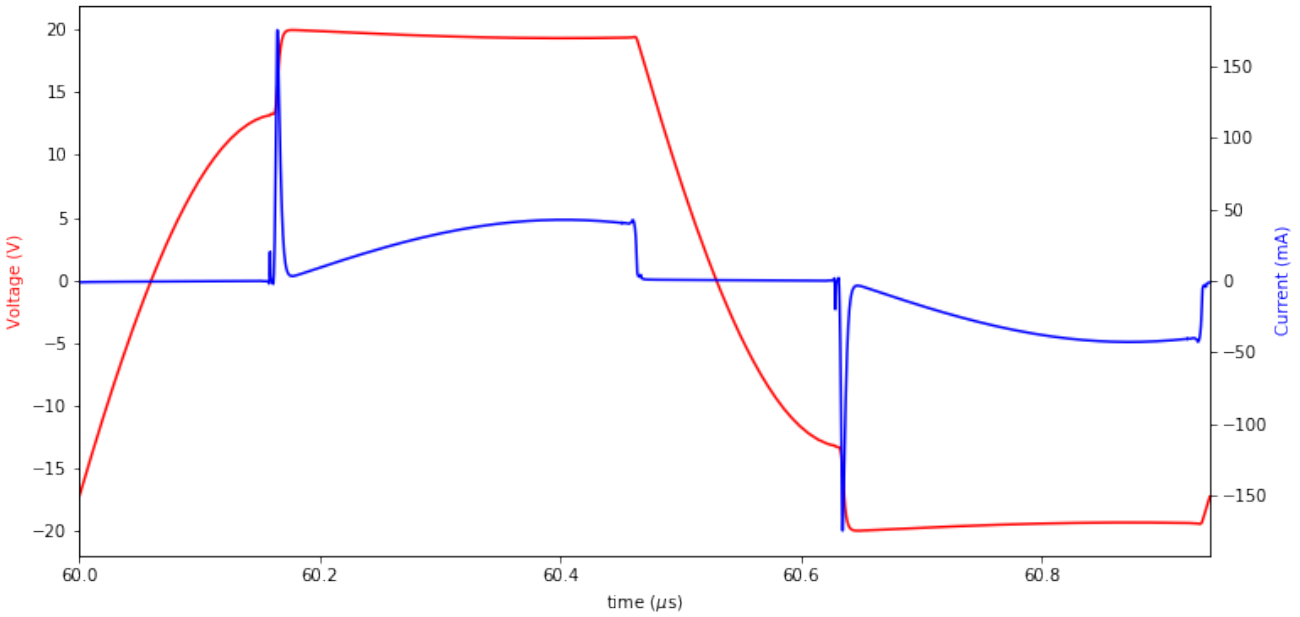

Figure 6.6: Output Voltage and Current of transducer 6

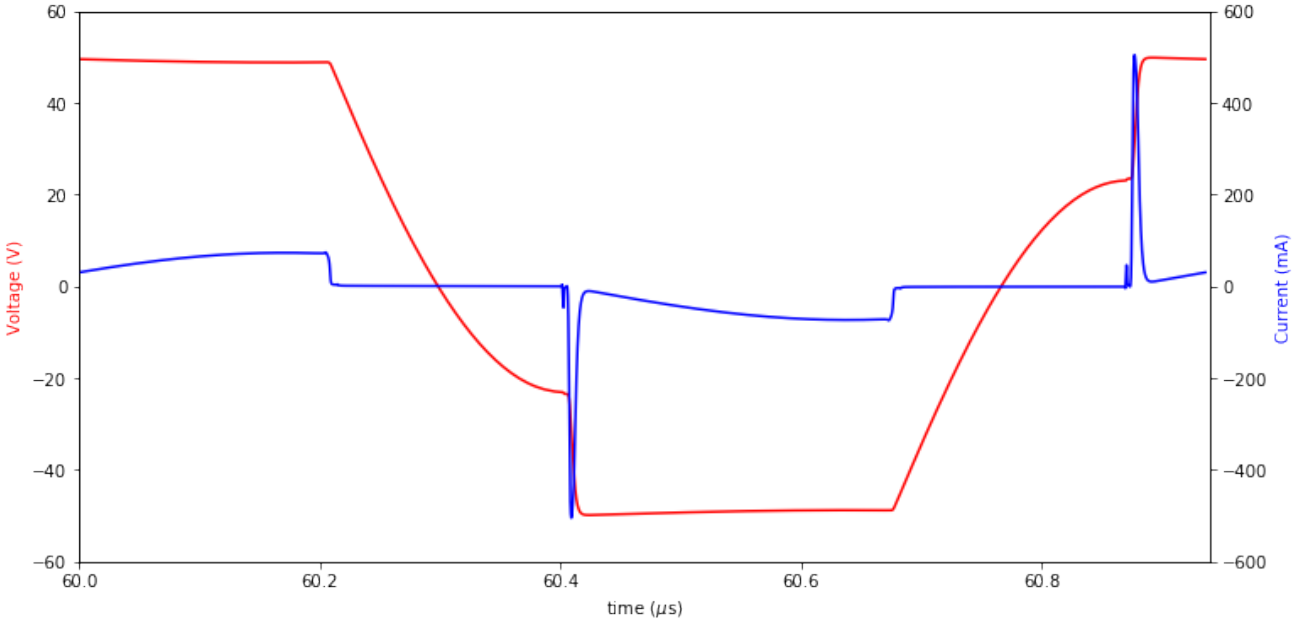

Figure 6.7: Output Voltage and Current of transducer 1

6.2 Output Waveform with 50V Supply

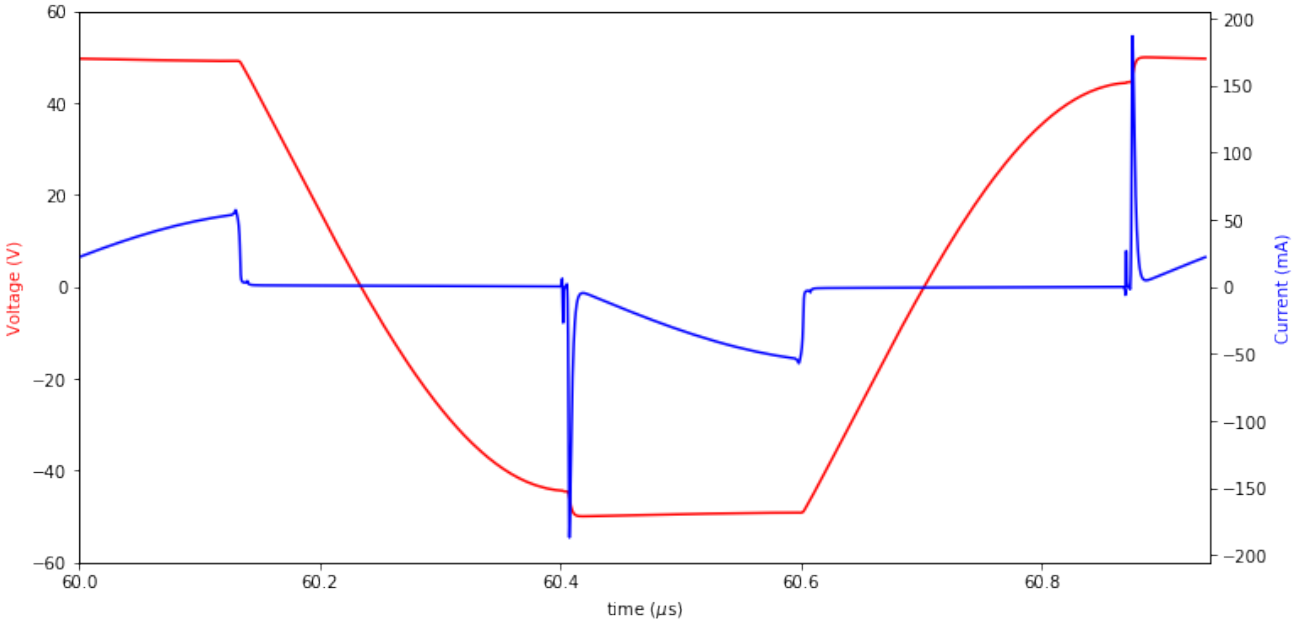

Figure 6.8: Output Voltage and Current of transducer 2

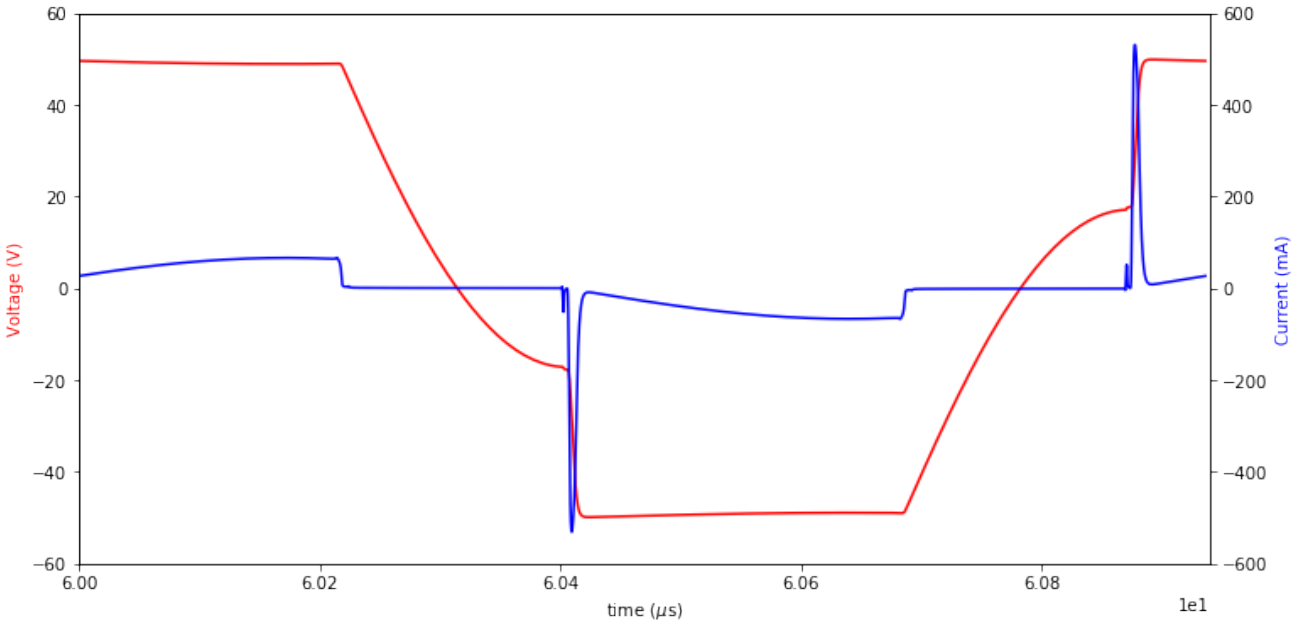

Figure 6.9: Output Voltage and Current of transducer 3

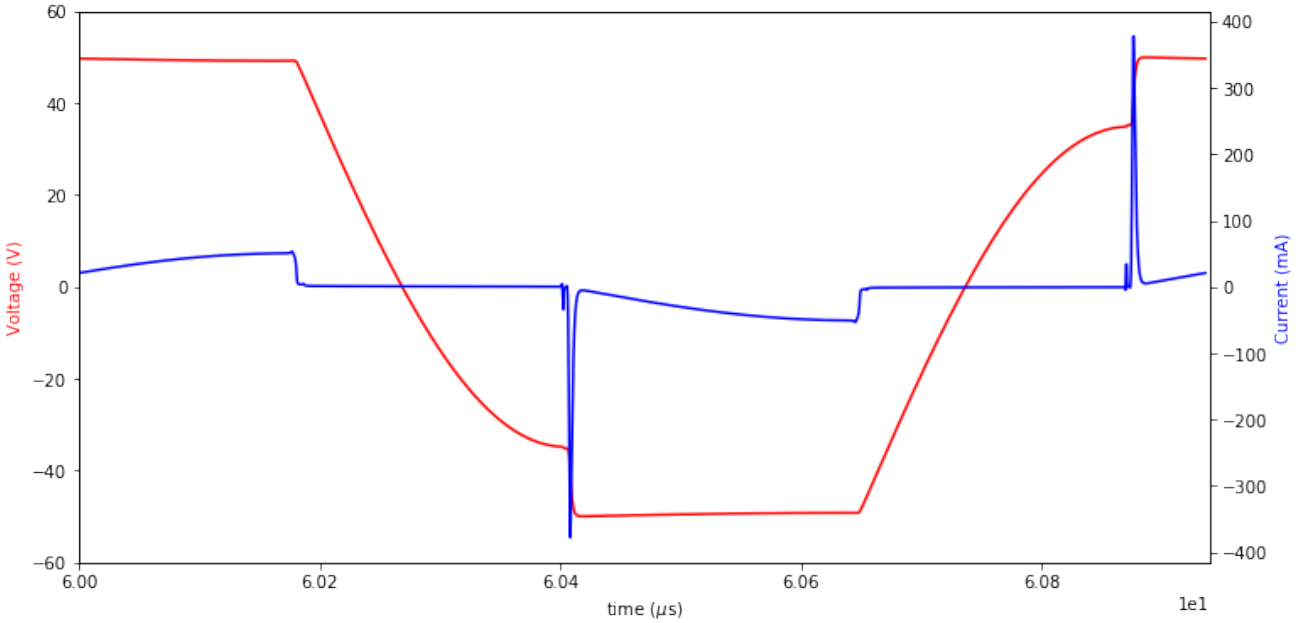

Figure 6.10: Output Voltage and Current of transducer 4

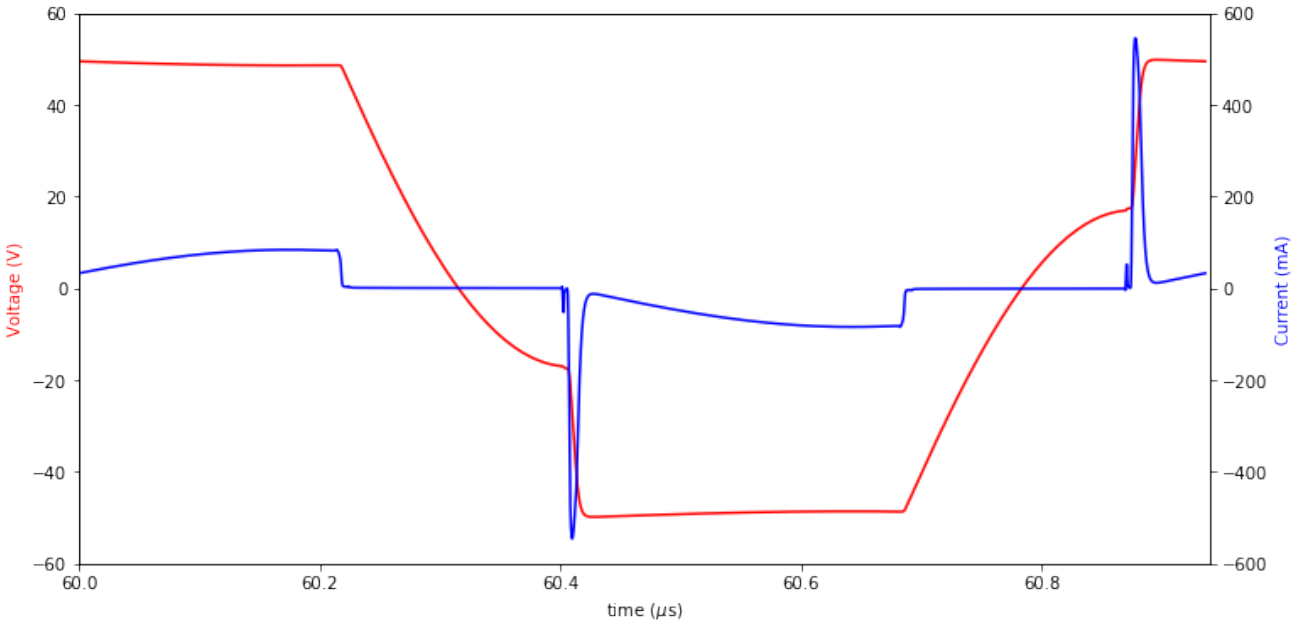

Figure 6.11: Output Voltage and Current of transducer 5

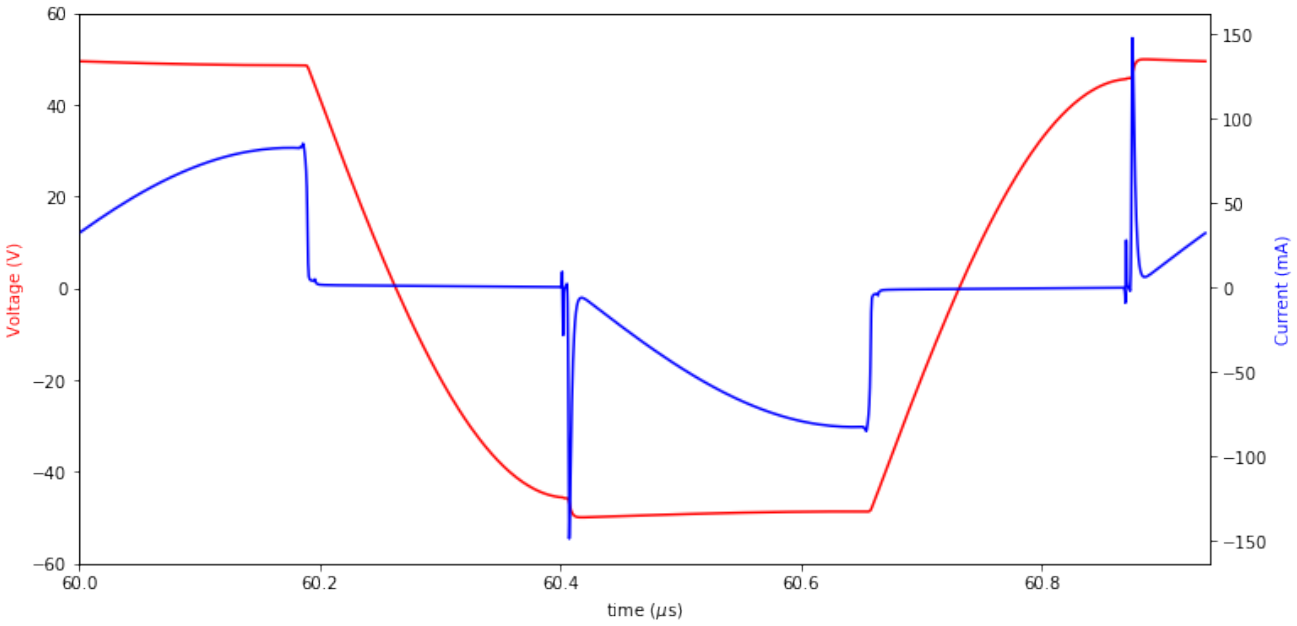

Figure 6.12: Output Voltage and Current of transducer 6

Chapter 7

Appendix B - Parameters Extraction

Threshold Voltage

The extraction method is found from [24]. In order to find the threshold voltage (V_t) and the specific current (I_{SQ}), the circuit is set up as shown in Figure 7.1. The Gate voltage$V_GB_NMOS_1$

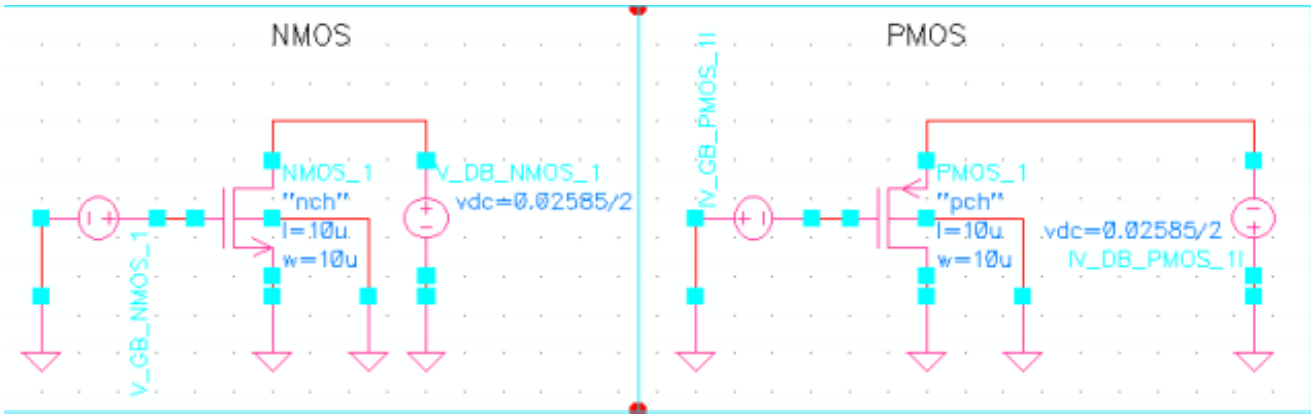

Figure 7.1: I_{SQ} and V_t extraction circuit

and $|V\_GB\_PMOS\_1|$ are swept from 0 to 20V to obtain the drain current I_D vs V_{GB} as shown in Figure 7.2

Then, by obtaining the transconductance-to-drain-current ratio (gm/I_D) curve of the MOSFET, The gate voltage at 53% of gm/ID's maximum value corresponds to the threshold voltage, V_t. as shown in Figure 7.3.

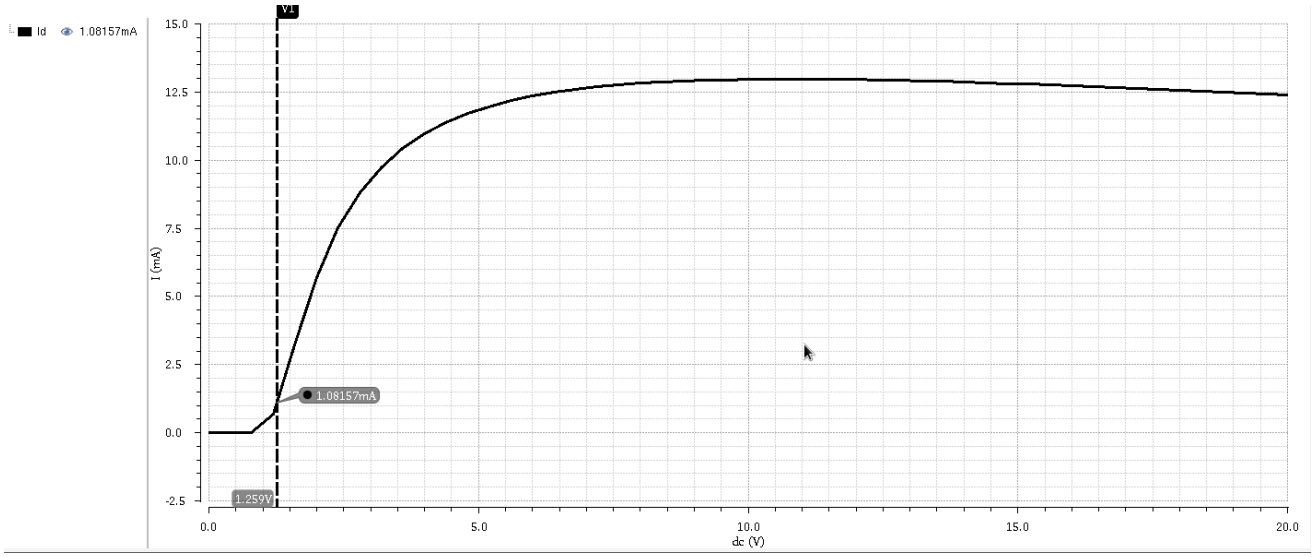

Figure 7.2: $I_D vs V_{GB}$ for NMOS50M

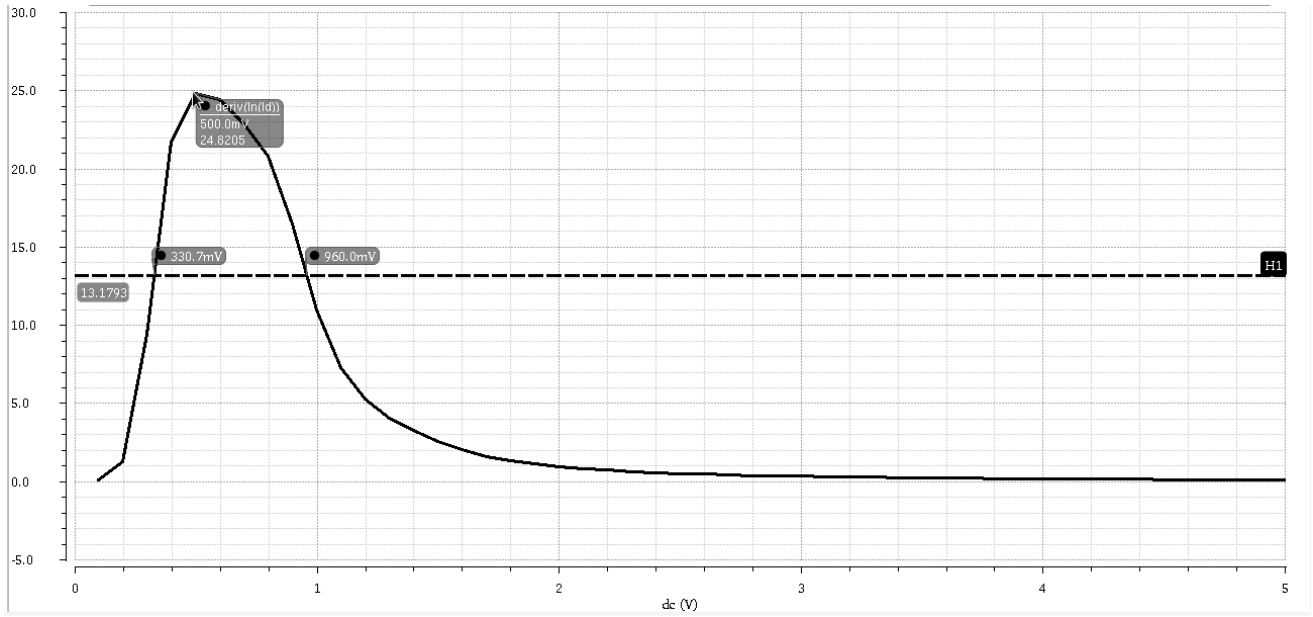

Figure 7.3: Obtaining V_t for NMOS50M

K' and mobility of degradation factors

The MOSFET's drain current can be estimated using the equation:

$$I_D = \frac{K'\frac{W}{L}(V_{GS} - V_t)V_{DS}}{1 + \theta_1(V_{GS} - V_t) + \theta_2(V_{GS} - V_t)^2}. \tag{7.1}$$

The circuits are set up are as shown in Figure 7.4 to find K', θ_1 and θ_2 for the NMOS50M. Assuming the transistor will operate in triode region, V_{DS} is fixed at 0.5V and is much smaller than $(V_{GS} - V_t)$ The transient drain current is taken and is as shown in Figure 7.5 for NMOS.

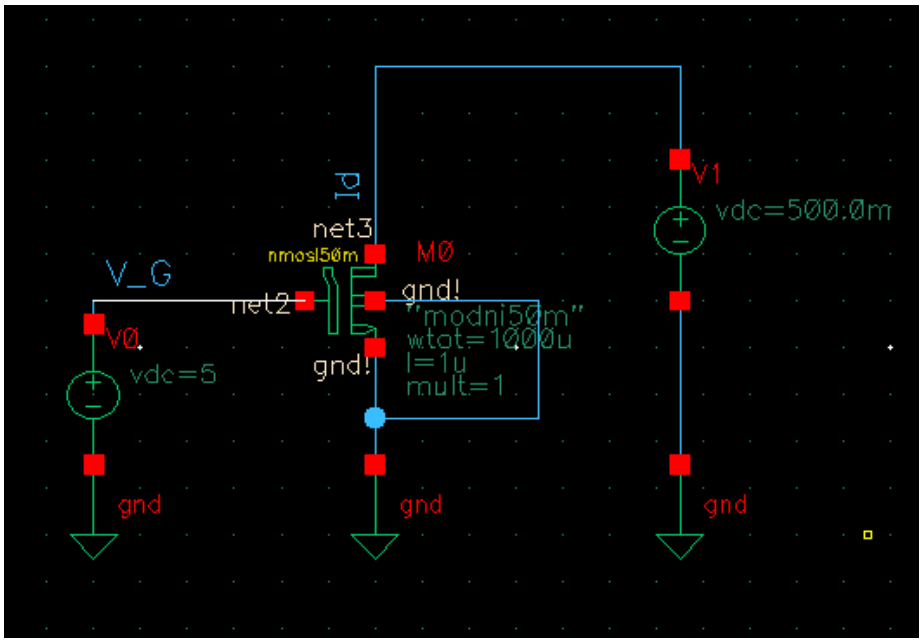

Figure 7.4: Circuit setup to extract parameters for NMOS50M

At the beginning, both θ_1 and θ_2 are assumed to be 0 to find K' using the equation:

$$K' = \frac{I_D}{\frac{W}{L}(V_{GS} - V_t) * 0.5V}. \tag{7.2}$$

By picking a point where there is a linear relationship between I_D and V_{GS}. The line 'I_recreated1' in Figure 7.5 represents the theoretical drain current (I_{Dt}).

$$I_{Dt} = K'\frac{W}{L}(V_{GS} - V_t)V_{DS}. \tag{7.3}$$

Then, θ_2 is still assumed to be 0 to solve for θ_1 using equation:

$$\theta_1 = \left(\frac{I_{Dt}}{I_{Dm}} - 1\right)/(V_{GS} - V_t). \tag{7.4}$$

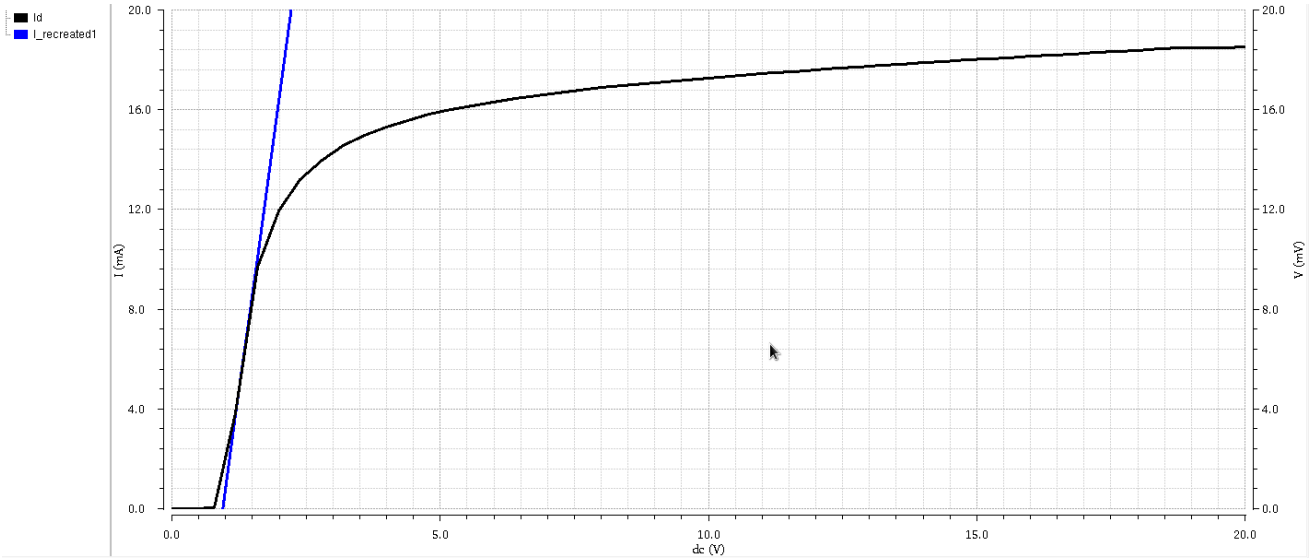

Figure 7.5: measure I_D (black) and recreated I_D (blue) with only K parameter for NMOS50M

By picking a point where the measured I_D is different than the theoretical drain current (I_{Dt}) and using Equation (7.4), θ_1 can be found. Then, by repeating the same process: plot the second theoretical drain current (I_{Dt2}) consider the effect of θ_1, pick a point where the I_{Dt2} is different than the measured I_D and use Equation (7.5) to solve for θ_2:

$$\theta_2 = \left(\frac{I_{Dt}}{I_{Dm}} - 1 - \theta_1 (V_{GS} - V_t) \right) / (V_{GS} - V_t)^2. \tag{7.5}$$

The recreated I_D using the value found is as shown in Figure 7.6. The process of finding K', θ_1 and θ_2 for PMOS is very similar to that of the NMOS. The circuit setup is as shown in Figure 7.7 The recreated drain current curve for PMOS is as shown in Figure 7.8

The extracted parameters are shown in Table 7.1

Table 7.1: Extracted Parameters

MOSFET	V_t (V)	K' ($\frac{\mu A}{V}$)	$\theta_1(V^{-1})$	$\theta_2(mV^{-2})$
NMOS50H	3.22	16.3	0.128	3.885
NMOS50M	0.96	31.402	0.7404	4.3155
PMOS50H	-2.05	-14.11	-0.3492	0
PMOS50M	-1.259	-15.995	-0.4074	-0.0105

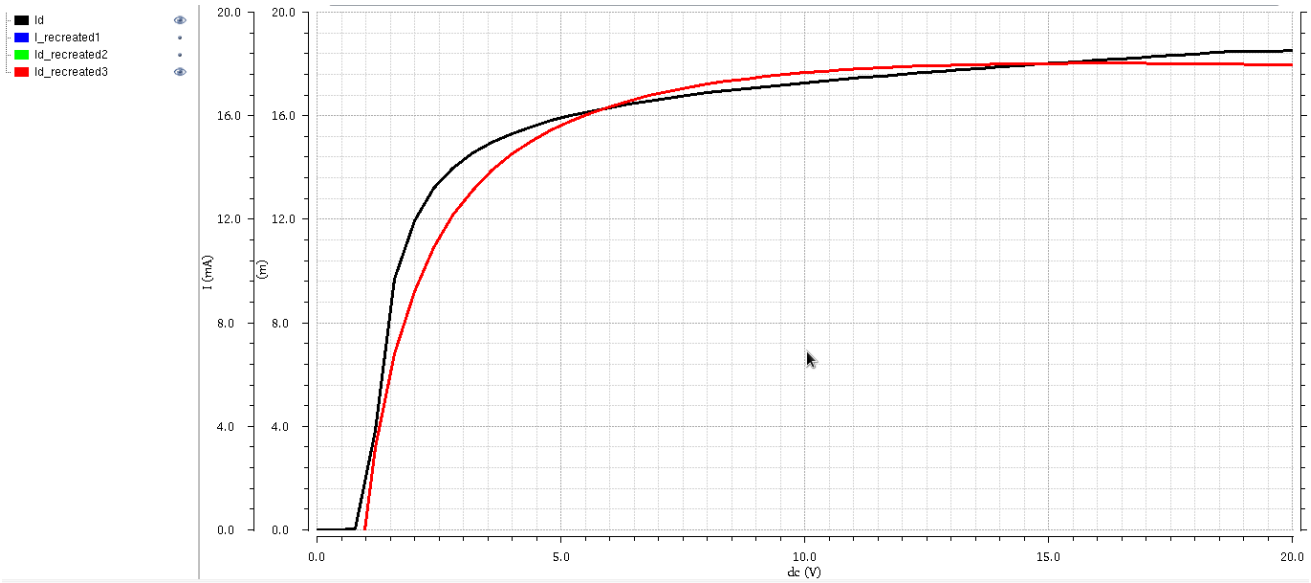

Figure 7.6: Recreated I_D using the extracted parameters (red) and the measure I_D (black)

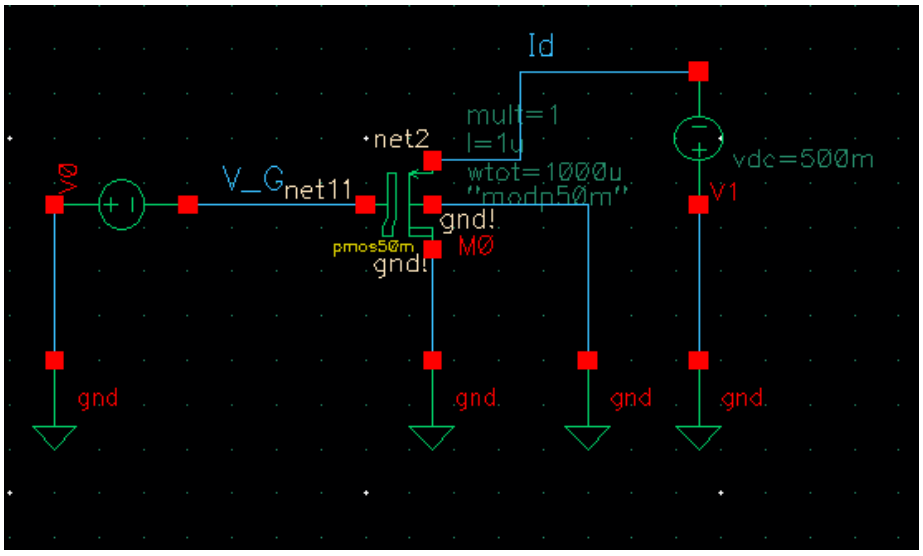

Figure 7.7: Circuit setup to extract parameters for PMOS50M

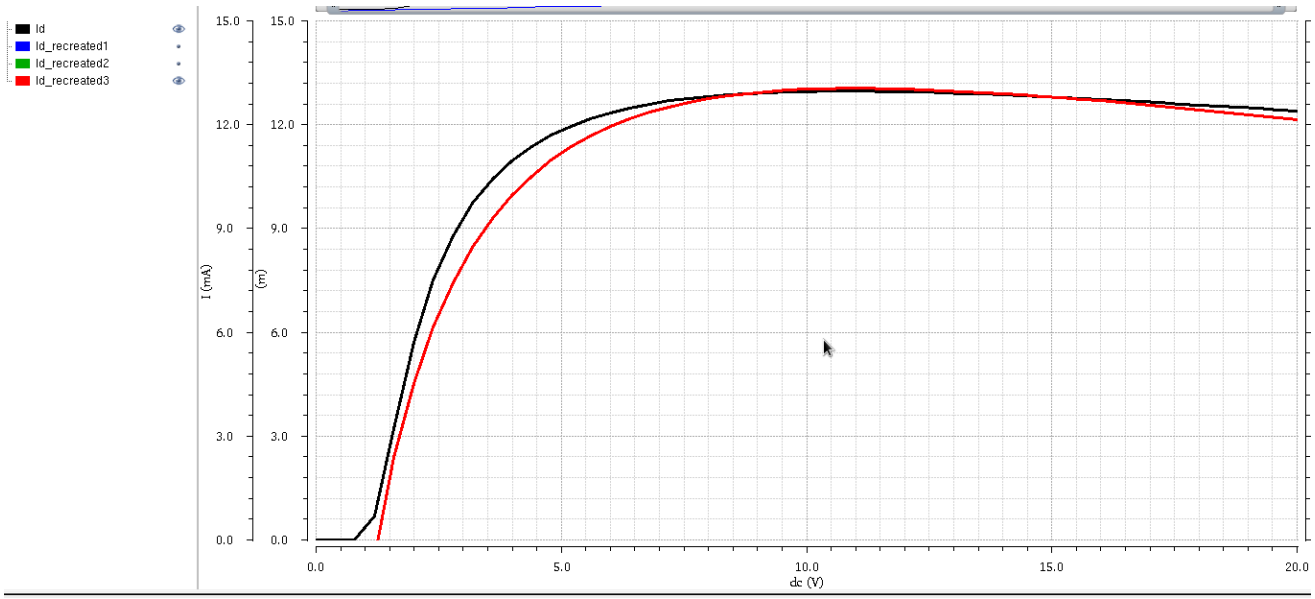

Figure 7.8: Recreated I_D for PMOS using the extracted parameters (red) and the measure I_D (black)

The extracted parameters are mostly used to calculate MOSFET on-resistance in this research. The calculated on-resistance is verified by the simulation as shown in Table 7.2. The setup is as shown in Figure 7.9. NMOS50H is used in this simulation to verify the results.

Table 7.2: Calculated on-resistance and the extracted on-resistance from simulation

MOSFET (NMOS50H) width (μm)	Calculated (Ω)	Simulation (Ω)
50	310.2	312.4
1000	15.5	14.9
5000	3.1	2.9

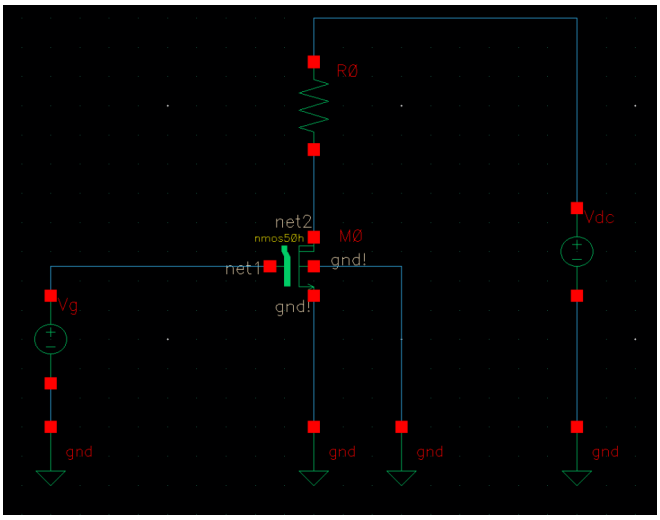

Figure 7.9: Simulation setup to extract the actual MOSFET on-resistance

Chapter 8

Appendix C - MOSFET Capacitance

8.1 Gate Capacitance

The gate capacitance of a MOSFET transistor can be estimated by

$$C_{gate} = W \cdot L \cdot C_{ox}, \tag{8.1}$$

where W and L are the width and length of the MOSFET, and C_{ox} is the gate oxide capacitance. The circuit setup to extract the C_{ox} for MOSFET gate capacitance is as shown in Figure 8.1. The extracted parameters are shown in Table 8.1. The gate voltage is a 0-20V pulse signal. The resistor is set high enough to see the gate voltage charging up. Recall the time constant equation:

$$\tau = RC, \tag{8.2}$$

$$C_{gate} = \frac{\tau}{R}. \tag{8.3}$$

The charging curve of the gate capacitance is plotted in Figure 8.2. τ is the time when V_{gate} charges to 0.632*V_{max}, which is 0.632 * 20V = 12.64V.

8.2 MOSFET Drain Capacitance

$$C_{DS} = WLC_j + 2W_uL_uC_{jsw}. \tag{8.4}$$

Where W and L are the effective width and length of the MOSFET, C_j and C_{jsw} are the junction and sidewall junction respectively. C_j is the junction capacitance, and C_{jsw} is the junction sidewall capacitance. c_j is 0.385mF/$(\mu m)^2$ and 0.22mF/$(\mu m)^2$ for NMOS and PMOS respectively. c_{jsw} is 0 and 0.33nF/μm for NMOS and PMOS used in this technology.

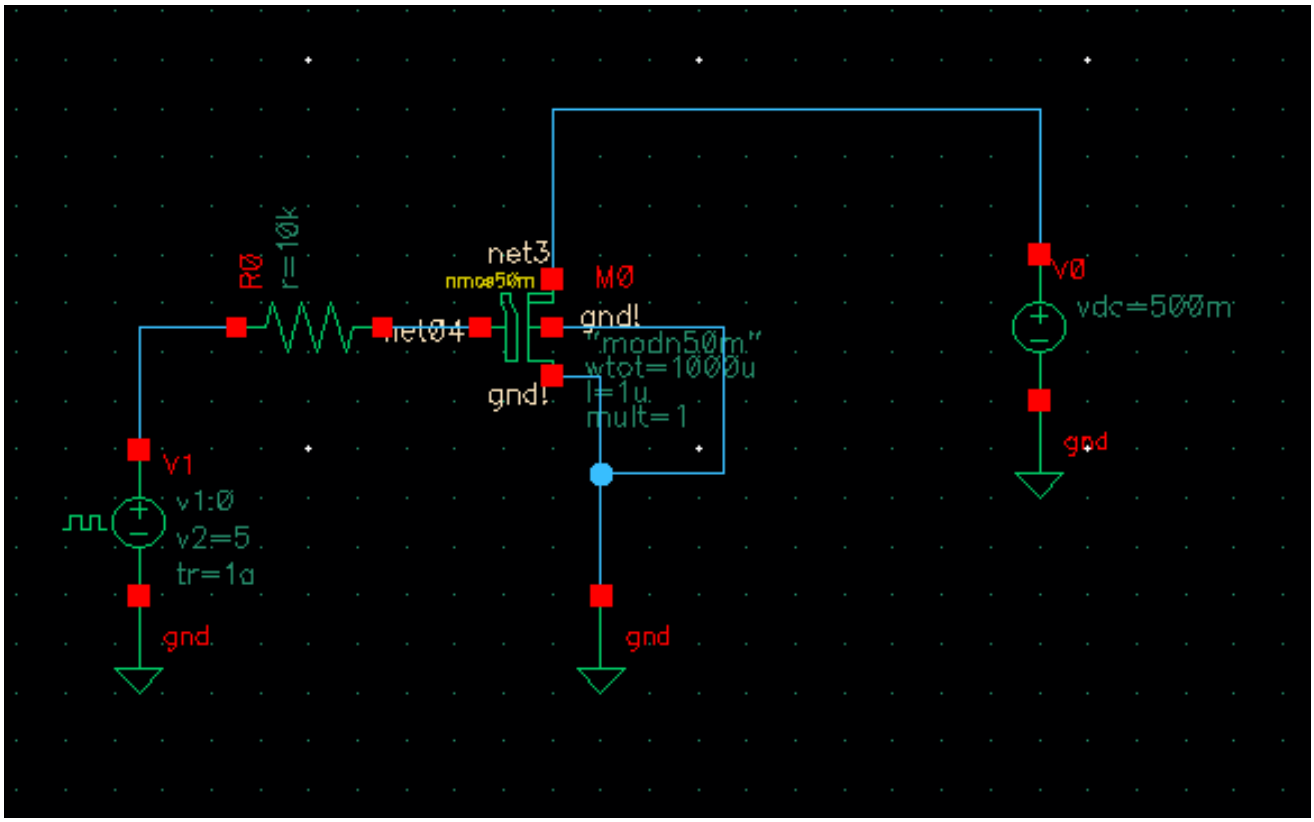

Figure 8.1: Circuit setup to find the gate capacitance

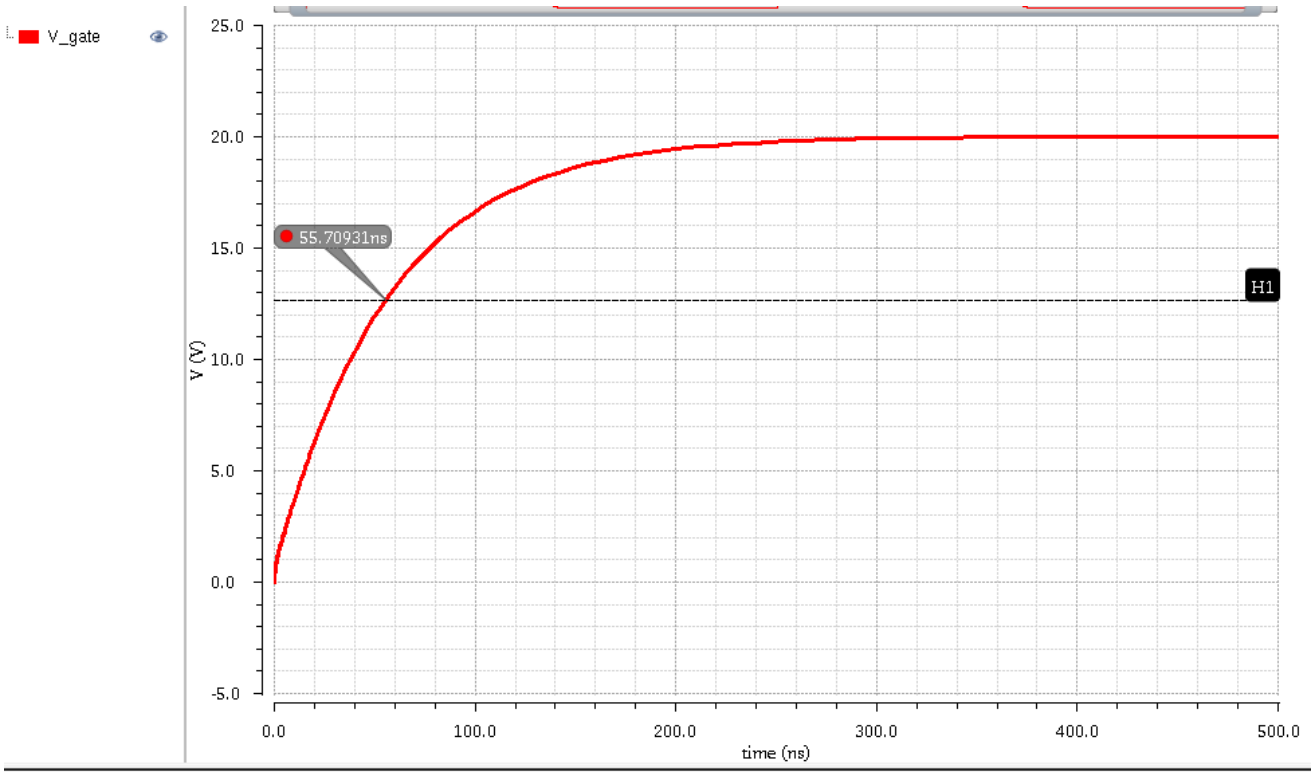

Figure 8.2: Gate capacitance charging curve

Table 8.1: Extracted C_{ox}

MOSFET	$C_{ox}(\frac{fF}{(\mu m)^2})$
NMOS50H	2.23
NMOS50M	5.50
PMOS50H	1.78
PMOS50M	4.65

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